# **Power MOSFET, N-Channel,** Trench<sup>®</sup>, 1.5 V Specified Thin WLCSP

# 20 V, 5.3 A, 39 mΩ

# **General Description**

Designed on advanced 1.5 V PowerTrench<sup>®</sup> process with state of the art "fine pitch" WLCSP packaging process, the FDZ192NZ minimizes both PCB space and r<sub>DS(on)</sub>. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low r<sub>DS(on)</sub>.

## Features

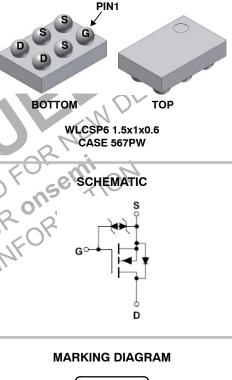
- Max  $r_{DS(on)} = 39 \text{ m}\Omega$  at  $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 2.0 \text{ A}$
- Max  $r_{DS(on)} = 43 \text{ m}\Omega$  at  $V_{GS} = 2.5 \text{ V}$ ,  $I_D = 2.0 \text{ A}$
- Max  $r_{DS(on)} = 49 \text{ m}\Omega$  at  $V_{GS} = 1.8 \text{ V}$ ,  $I_D = 1.0 \text{ A}$
- Max  $r_{DS(on)} = 55 \text{ m}\Omega$  at  $V_{GS} = 1.5 \text{ V}$ ,  $I_D = 1.0 \text{ A}$
- Occupies only 1.5 mm<sup>2</sup> of PCB Area. Less than 50% of the Area of 2 x 2 BGA

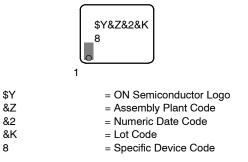
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant , wanagement • Load Switch • Battery Protection • HS REPRESENTATION • REPRESENTA



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# **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

#### **ORDERING INFORMATION**

Part Number	Device Marking	Package	Shipping <sup>†</sup>
FDZ192NZ	8	WLCSP6 1.5x1x0.6 (Pb-Free / Halogen Free)	5000 Units / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

#### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = $25^{\circ}$ C unless otherwise noted)

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain to Source Voltage	20	V
V <sub>GS</sub>	Gate to Source Voltage	±8	V
۱ <sub>D</sub>	Drain Current Continuous, T <sub>A</sub> = 25°C (Note 1a)	5.3	А
	Drain Current Pulsed	15	
PD	Power Dissipation, $T_A = 25^{\circ}C$ (Note 1a)	1.9	N W
	Power Dissipation, $T_A = 25^{\circ}C$ (Note 1b)	0.9	2
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### **THERMAL CHARACTERISTICS**

Symbol	Parameter Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a) 65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b) 133	°C/W
	CHARACTERISTICS (T - 25°C unless otherwise noted)	

# ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
off Charact	eristics	DR. IE'				
$BV_{DSS}$	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu A$ , referenced to 25°C		10		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V			1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 8 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μΑ

**On Characteristics** 

VGS(th)	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \ \mu A$	0.4	0.7	1.0	V
$\Delta V_{GS(th)} \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25°C		-3		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_{D} = 2.0 \text{ A}$		26	39	mΩ
		$V_{GS} = 2.5 \text{ V}, I_{D} = 2.0 \text{ A}$		29	43	
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 1.0 A		33	49	
		V <sub>GS</sub> = 1.5 V, I <sub>D</sub> = 1.0 A		38	55	
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 2.0 \text{ A}, \text{ T}_{J} = 125^{\circ}\text{C}$		31	47	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 \text{ V}, \text{ I}_{D} = 5.3 \text{ A}$		36		s

#### **Dynamic Characteristics**

Ciss	Input Capacitance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	915	1220	pF
Coss	Output Capacitance	$v_{\rm DS} = 10^{-1}$ , $v_{\rm GS} = 0^{-1}$ , $1 = 1^{-1}$ with 2	145	195	pF
Crss	Reverse Transfer Capacitance		100	150	pF

#### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Cor	Test Conditions		Тур	Max	Unit
Switching C	Characteristics						
td(on)	Turn-On Delay Time				6.5	13	ns
t <sub>r</sub>	Rise Time		$V_{DD}$ = 10 V, I <sub>D</sub> = 5.3 A, V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω		4	10	ns
td(off)	Turn-Off Delay Time				50	80	ns
t <sub>f</sub>	Fall Time				20	32	ns
Q <sub>g</sub>	Total Gate Charge	$V_{GS}$ = 0 V to 4.5 V	$V_{DD} = 10 V,$ $I_{D} = 5.3 A$		12	17	nC
Qgs	Gate to Source Charge				1.3		nC
Qgd	Gate to Drain "Miller" Charge				2.3		nC

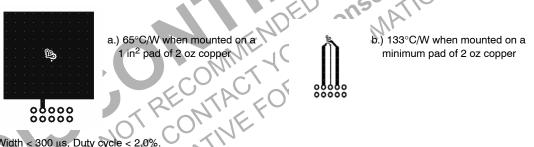
#### **Drain-Source Diode Characteristics**

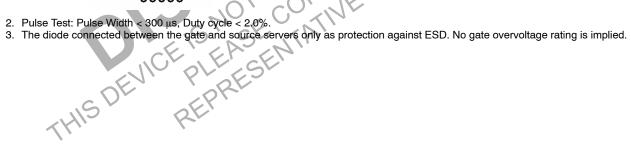
١	V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.1 A (Note 2)	0.6	1.2	V
	trr	Reverse Recovery Time	I <sub>F</sub> = 5.3 A, di/dt = 100 A/us	18	32	ns
(	Qrr	Reverse Recovery Charge		4.6	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

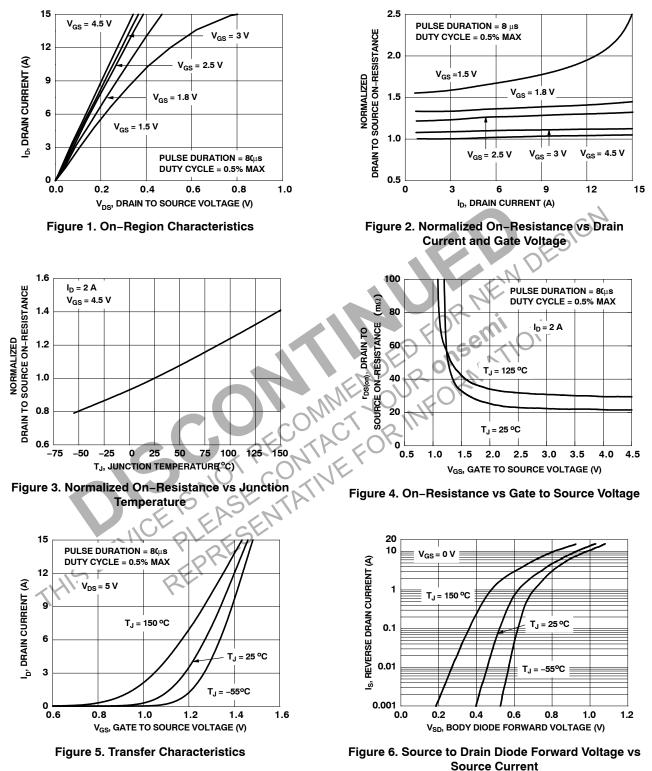
1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.





# **TYPICAL CHARACTERISTICS**

(T<sub>J</sub> = 25°C unless otherwise noted)



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(T<sub>J</sub> = 25°C unless otherwise noted)

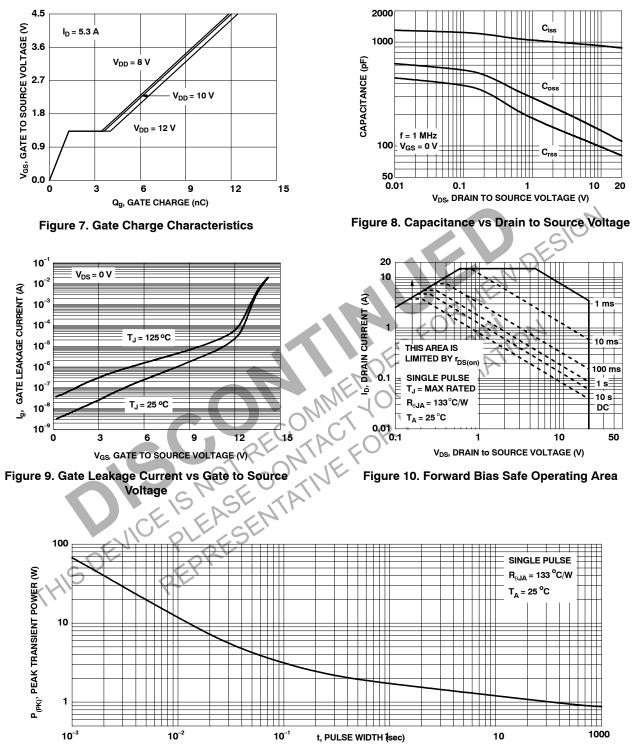
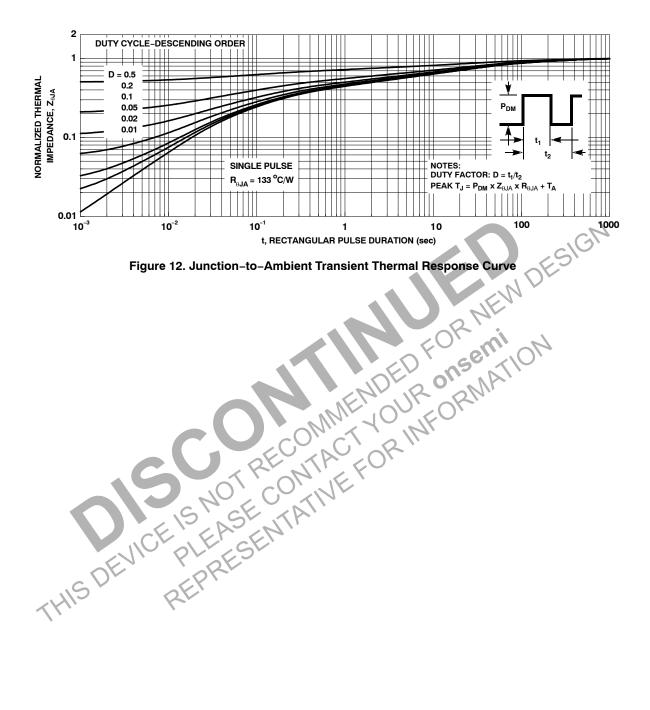


Figure 11. Single Pulse Maximum Power Dissipation

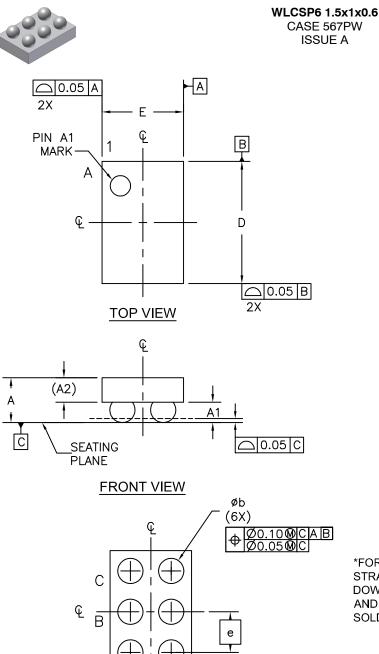
# **TYPICAL CHARACTERISTICS**

(T<sub>J</sub> = 25°C unless otherwise noted)



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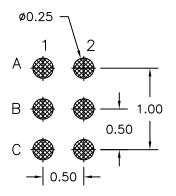
DATE 04 AUG 2021

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REGISTRATION REFERENCE AS OF OCTOBER 2005.
C) DRAWING CONFORMS TO ASME

Y14.5M-2009

DIM	MILLIMETERS				
	MIN.	NOM.	MAX.		
Α	-	-	0.60		
A1	0.22	0.25	0.28		
A2	(	0.30 REF			
b	0.24	0.31	0.39		
D	1.45	1.50	1.55		
E	0.95	1.00	1.05		
е	(	0.50 BSC			



#### LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	WLCSP6 1.5x1x0.6		PAGE 1 OF 1		

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