

# MOSFET – N-Channel POWERTRENCH®

30 V, 8.5 A, 23 mΩ

## FDS8884

### Description

This N-Channel MOSFET has been Designed Specifically to improve the overall efficiency of DC/DC Converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(on)}$  and fast switching speed.

### Features

- Max  $R_{DS(on)}$  = 23 mΩ at  $V_{GS} = 10$  V,  $I_D = 8.5$  A
- Max  $R_{DS(on)}$  = 30 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 7.5$  A
- Low Gate Charge
- 100%  $R_G$  Tested
- These Device is Pb-Free and RoHS Compliant

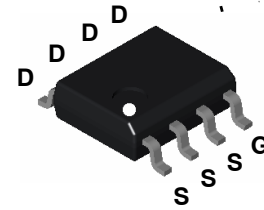
### MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current Continuous (Note 1a) Pulsed	8.5 40	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	32	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	2.5	W
	Derate Above $25^\circ\text{C}$	20	mW/ $^\circ\text{C}$
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	$-55$ to $+150$	$^\circ\text{C}$

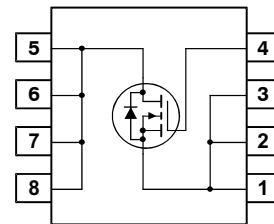
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

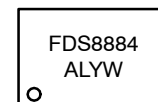
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Case (Note 1)	25	



SOIC8,  
CASE 751EB



### MARKING DIAGRAM



FDS8884 = Specific Device Code  
A = Assembly Location  
L = Lot Traceability Code  
YW = Date Code (Year and Week)

### ORDERING INFORMATION

Device	Package	Shipping†
FDS8884	SO-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

**ELECTRICAL CHARACTERISTICS**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	23	–	mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}$ $V_{GS} = 0\ \text{V}$ , $T_J = 125^\circ\text{C}$	–	–	1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$	–	–	$\pm 100$	nA

**On Characteristics (Note 3)**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 380\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	–4.9	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Drain to Source On-Resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 8.5\ \text{A}$	–	19	23	m $\Omega$
		$V_{GS} = 4.5\ \text{V}$ , $I_D = 7.5\ \text{A}$	–	23	30	
		$V_{GS} = 10\ \text{V}$ , $I_D = 8.5\ \text{A}$ , $T_J = 125^\circ\text{C}$	–	26	32	

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	–	475	635	pF
$C_{oss}$	Output Capacitance		–	100	135	pF
$C_{rss}$	Reverse Transfer Capacitance		–	65	100	pF
$R_g$	Gate Resistance	$f = 1\ \text{MHz}$	–	0.9	1.6	$\Omega$

**Switching Characteristics (Note 3)**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\ \text{V}$ , $I_D = 8.5\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_{GS} = 32\ \Omega$	–	5	10	ns
$t_r$	Rise Time		–	9	18	ns
$t_{d(off)}$	Turn-Off Delay Time		–	42	68	ns
$t_f$	Fall Time		–	21	34	ns
$Q_g$	Total Gate Charge	$V_{DS} = 15\ \text{V}$ , $V_{GS} = 10\ \text{V}$ , $I_D = 8.5\ \text{A}$	–	9.2	13	nC
$Q_g$	Total Gate Charge	$V_{DS} = 15\ \text{V}$ , $V_{GS} = 5\ \text{V}$ , $I_D = 8.5\ \text{A}$	–	5.0	7	nC
$Q_{gs}$	Gate to Source Gate Charge		–	1.5	–	nC
$Q_{gd}$	Gate to Drain Charge		–	2.0	–	nC

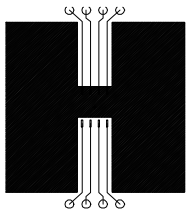
**Drain-Source Diode Characteristics and Maximum Ratings**

$V_{SD}$	Source to Drain Diode Forward Voltage	$I_{SD} = 8.5\ \text{A}$	–	0.9	1.25	V
		$I_{SD} = 2.1\ \text{A}$	–	0.8	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_F = 8.5\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$	–	–	33	ns
$Q_{rr}$	Reverse Recovery Charge		–	–	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

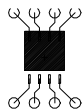
**NOTES:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

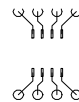


Scale 1 : 1 on letter size paper

a). 50  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b). 105  $^\circ\text{C}/\text{W}$  when mounted on a 0.4 in<sup>2</sup> pad of 2 oz copper.



c). 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad

- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\ \text{mH}$ ,  $I_{AS} = 8\ \text{A}$ ,  $V_{DD} = 27\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .
- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## TYPICAL CHARACTERISTICS

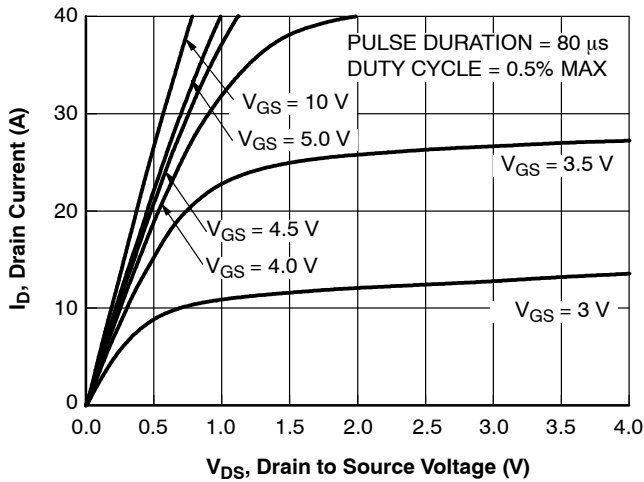
(T<sub>J</sub> = 25 °C unless otherwise noted)

Figure 1. On-Region Characteristics

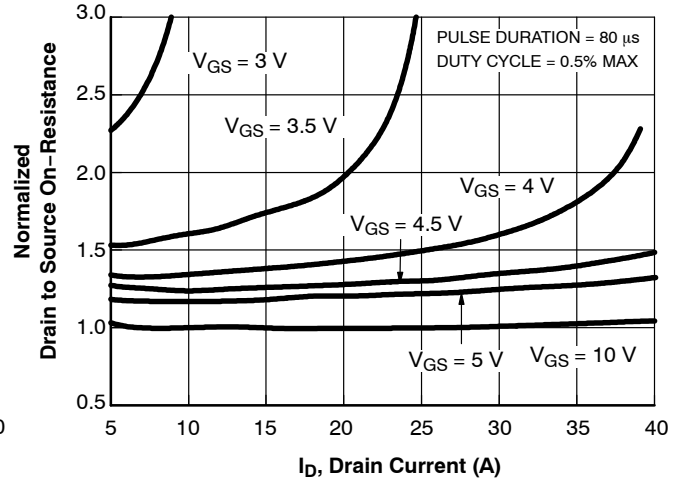


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

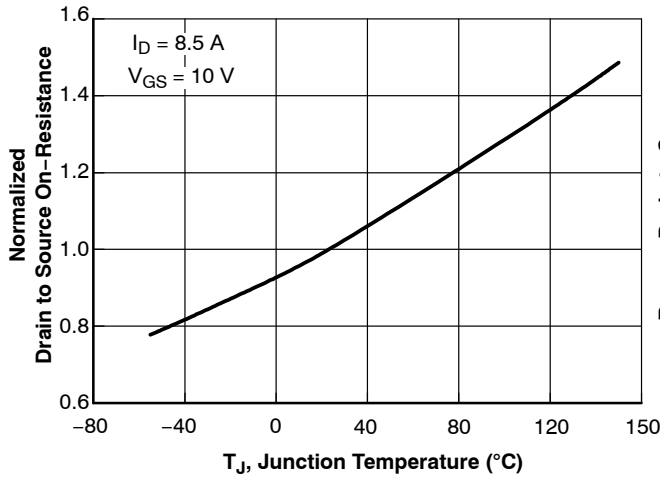


Figure 3. Normalized On-Resistance vs. Junction Temperature

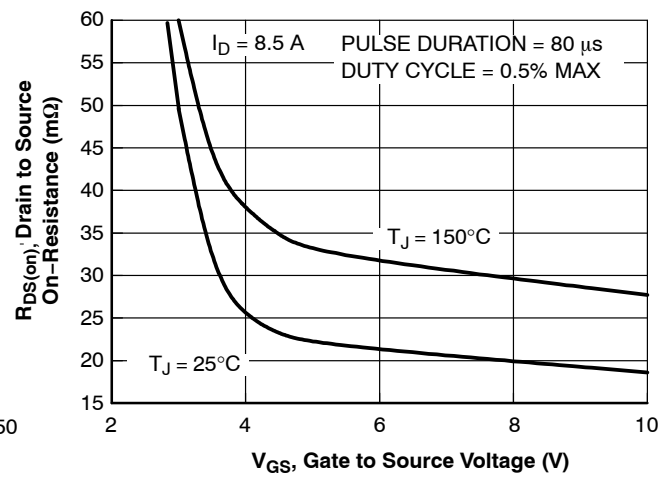


Figure 4. On-Resistance vs. Gate to Source Voltage

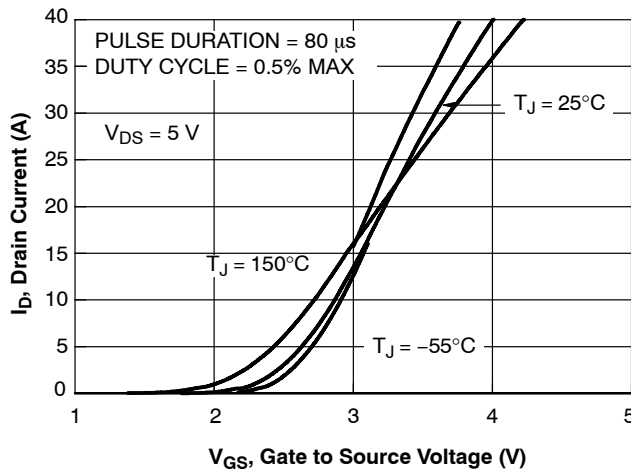


Figure 5. Transfer Characteristics

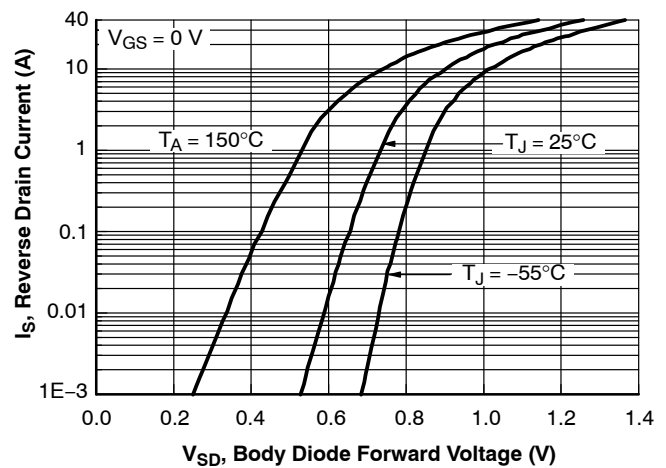


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

## TYPICAL CHARACTERISTICS

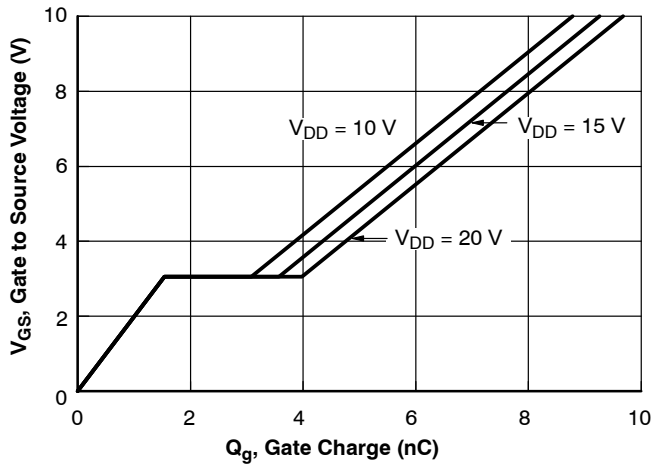
(T<sub>J</sub> = 25 °C unless otherwise noted) (CONTINUED)

Figure 7. Gate Charge Characteristics

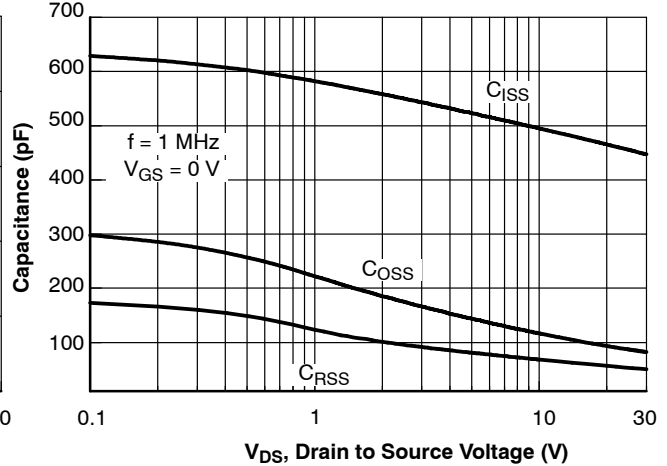


Figure 8. Capacitance vs Drain to Source Voltage

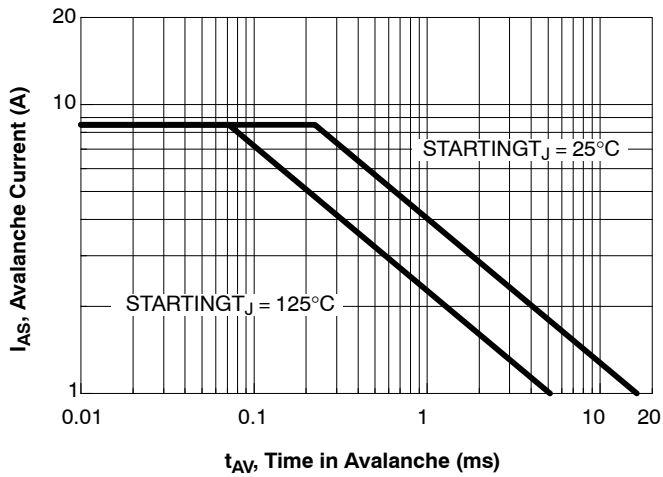


Figure 9. Unclamped Inductive Switching Capability

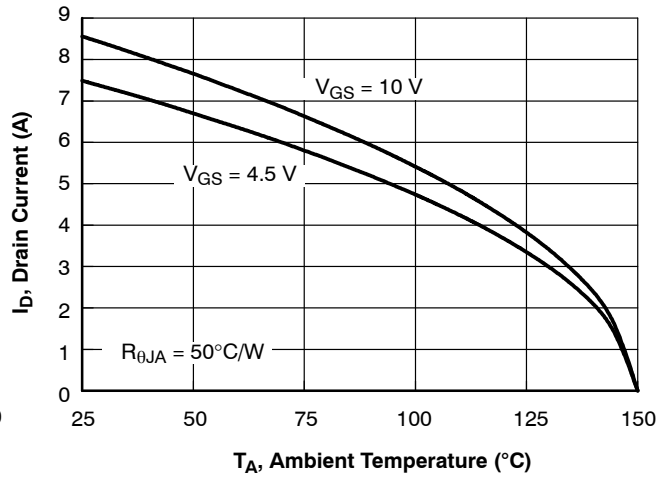


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

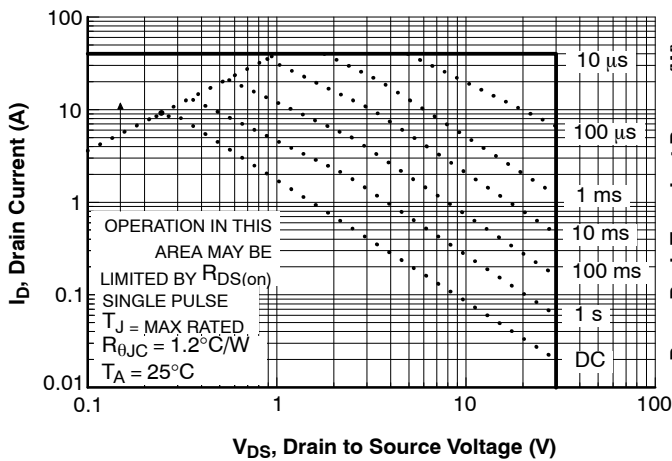


Figure 11. Forward Bias Safe Operating Area

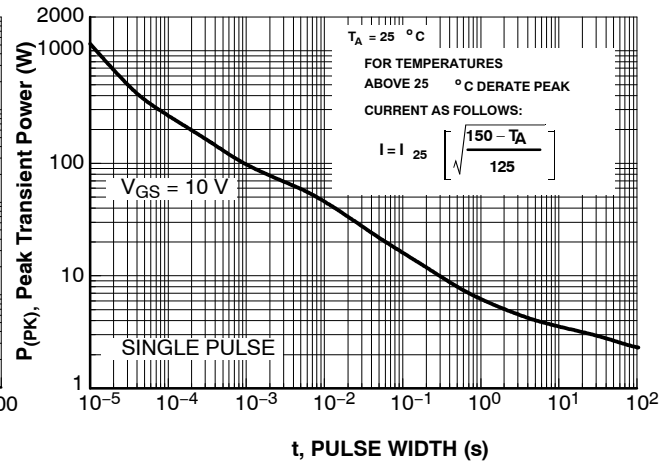
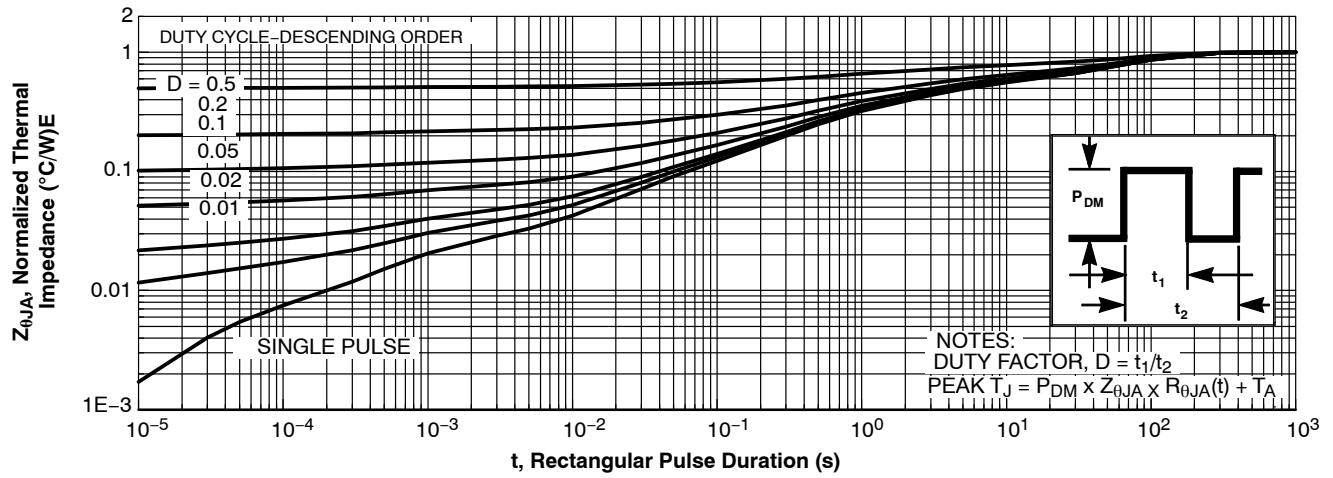


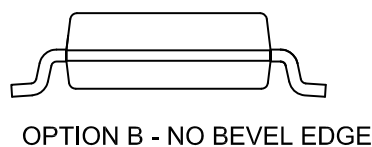
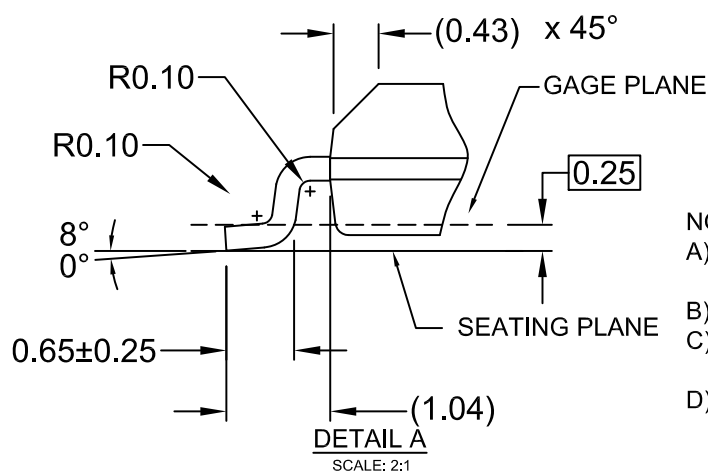
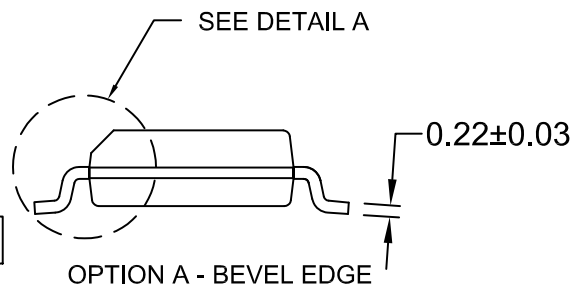
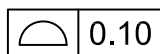
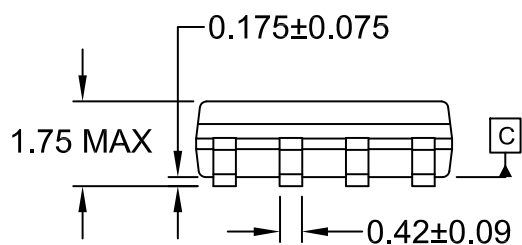
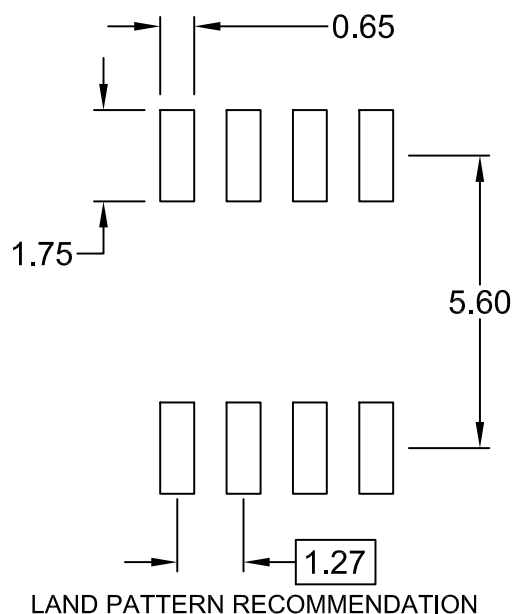
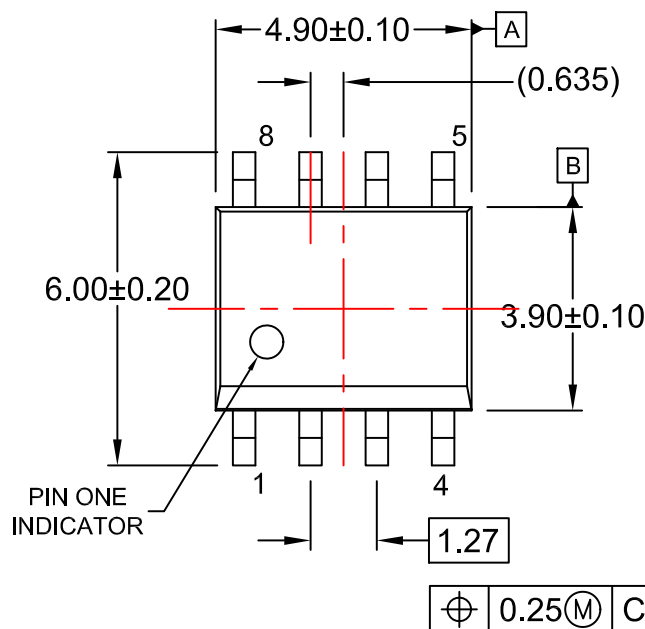
Figure 12. Single Pulse Maximum Power Dissipation

## TYPICAL CHARACTERISTICS

(T<sub>J</sub> = 25 °C unless otherwise noted) (CONTINUED)

**SOIC8**  
CASE 751EB  
ISSUE A

DATE 24 AUG 2017



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.  
B) ALL DIMENSIONS ARE IN MILLIMETERS.  
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.  
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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