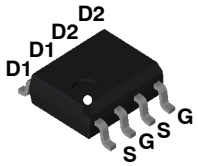
# MOSFET – N-Channel, POWERTRENCH®

## 30 V, 18.5 A, 4.5 mΩ

# FDS8813NZ




SOIC8
CASE 751EB

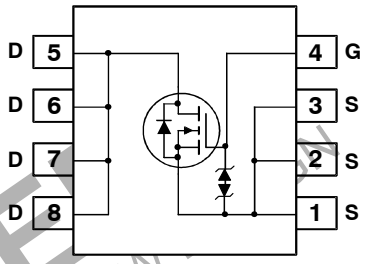
### Description

This N−Channel MOSFET is Produced using **onsemi**'s Advanced POWERTRENCH Process that has been especially tailored to minimize the on−state resistance.

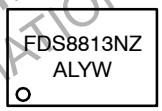
This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Features

- Max $R_{DS(on)}$ = 4.5 mΩ at $V_{GS}$ = 10 V, $I_D$ = 18.5 A
- Max $R_{DS(on)}$ = 6.0 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 16 A
- HBM ESD Protection Level of 5.6 kV Typical (note 3)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- These Device is Pb−Free and RoHS Compliant




### MARKING DIAGRAM




FDS8813NZ = Specific Device Code
A = Assembly Location
L = Lot Traceability Code
YW = Date Code (Year and Week)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDS8813NZ | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### MOSFET MAXIMUM RATINGS $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current−Continuous<br>−Pulsed | 18.5<br>74 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 4) | 337 | mJ |
| $P_D$ | Power Dissipation (Note 1a) | 2.5 | W |
| | Power Dissipation (Note 1b) | 1.0 | |
| $T_J$, $T_{stg}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Note 1) | 25 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 50 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1b) | 125 | |

**ELECTRICAL CHARACTERISTICS** $T_J$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 30 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | – | 20 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±10 | nA |
| **On Characteristics (Note 3)** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1 | 1.8 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | – | −6 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain to Source On−Resistance | $V_{GS}$ = 10 V, $I_D$ = 18.5 A | – | 3.8 | 4.5 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 16 A | – | 4.7 | 6.0 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 18.5 A, $T_J$ = 125°C | – | 5.1 | 6.6 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 18.5 A | – | 74 | – | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 3115 | 4145 | pF |
| $C_{oss}$ | Output Capacitance | | – | 580 | 775 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 345 | 520 | pF |
| $R_g$ | Gate Resistance | f = 1 MHz | 0.1 | 1.8 | 5.6 | Ω |
| **Switching Characteristics (Note 3)** | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 18.5 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 13 | 24 | ns |
| $t_r$ | Rise Time | | – | 8 | 16 | ns |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 39 | 63 | ns |
| $t_f$ | Fall Time | | – | 7 | 14 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V, to 10 V, $V_{DD}$ = 15 V, $I_D$ = 18.5 A | – | 55 | 76 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V, to 5 V, $V_{DD}$ = 15 V, $I_D$ = 18.5 A | – | 28 | 40 | nC |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 15 V, $I_D$ = 18.5 A | – | 9 | – | nC |
| $Q_{gd}$ | Gate to Drain Charge “Miller” Charge | | – | 10 | – | nC |
| **Drain−Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | – | 0.7 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 18.5 A, di/dt = 100 A/μs | – | 32 | 47 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 27 | 41 | nC |



Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to− ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user’s board design.

a) 50 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.

b) 125 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. The Diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
4. Starting $T_J$ = 25°C, L = 3 mH, $I_{AS}$ = 15 A, $V_{DD}$ = 30 V, $V_{GS}$ =10 V.

## TYPICAL CHARACTERISTICS

($T_J$ = 25 °C unless otherwise noted)

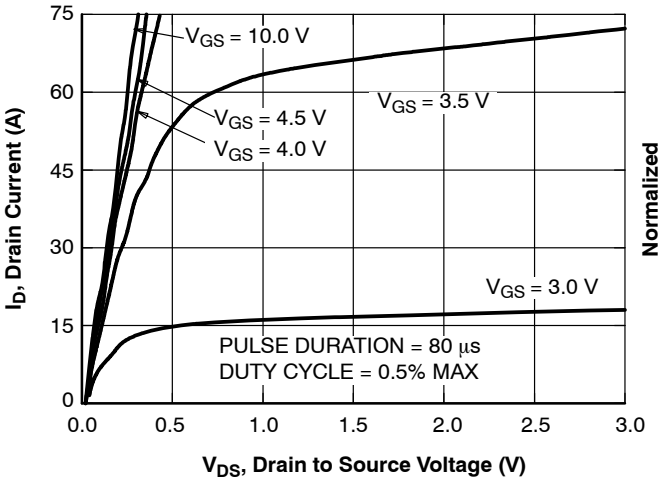



Figure 1. On−Region Characteristics

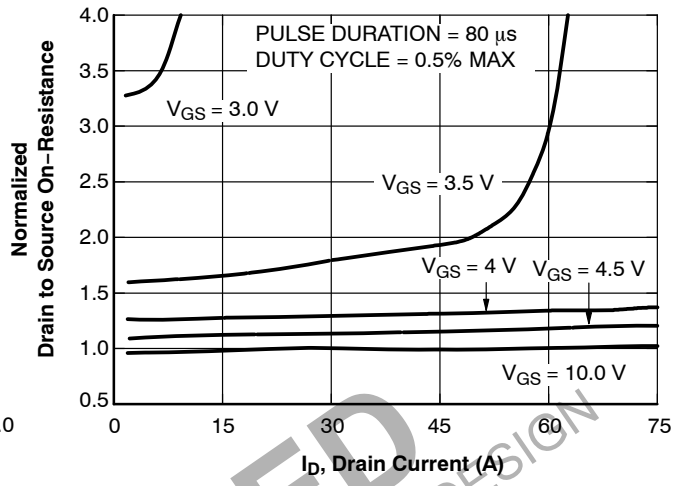



Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

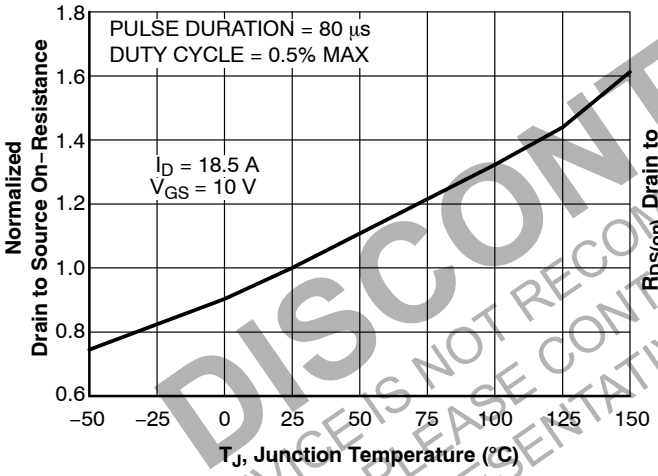



Figure 3. Normalized On−Resistance vs Junction Temperature

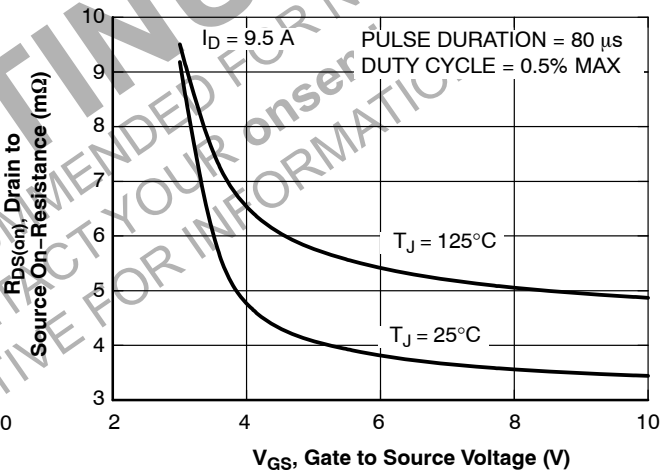



Figure 4. On−Resistance vs Gate to Source Voltage

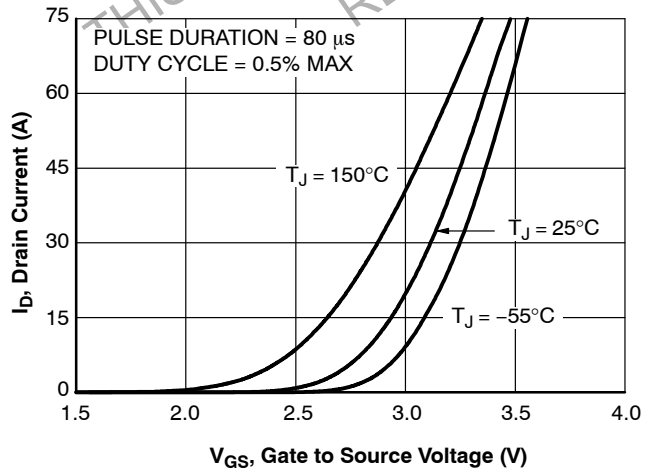



Figure 5. Transfer Characteristics

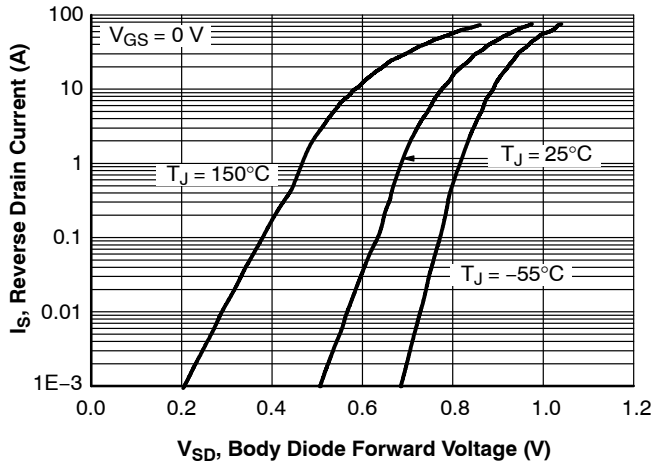



Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## TYPICAL CHARACTERISTICS (CONTINUED)

($T_J$ = 25 °C unless otherwise noted)

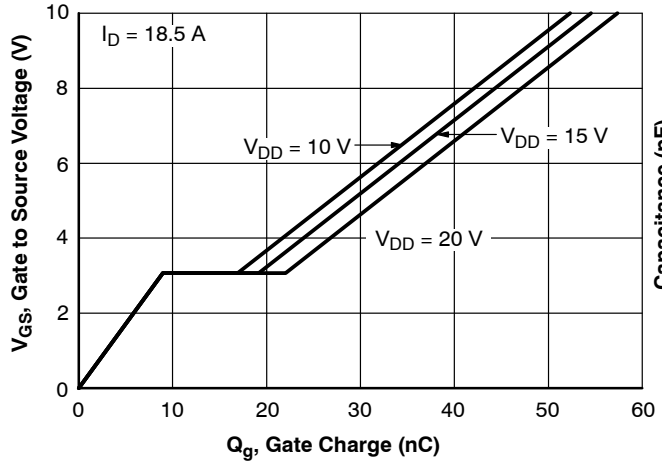



**Figure 7. Gate Charge Characteristics**

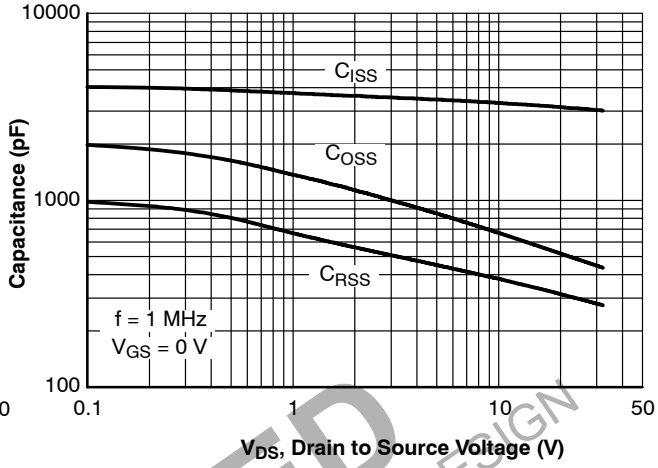



**Figure 8. Capacitance vs Drain to Source Voltage**

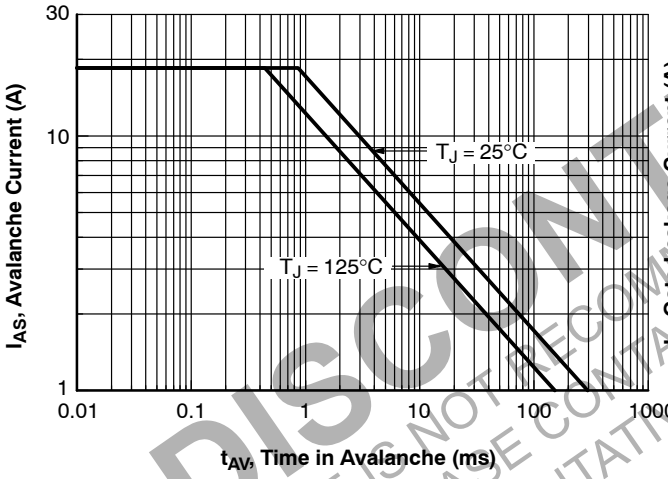



**Figure 9. Unclamped Inductive Switching Capability**

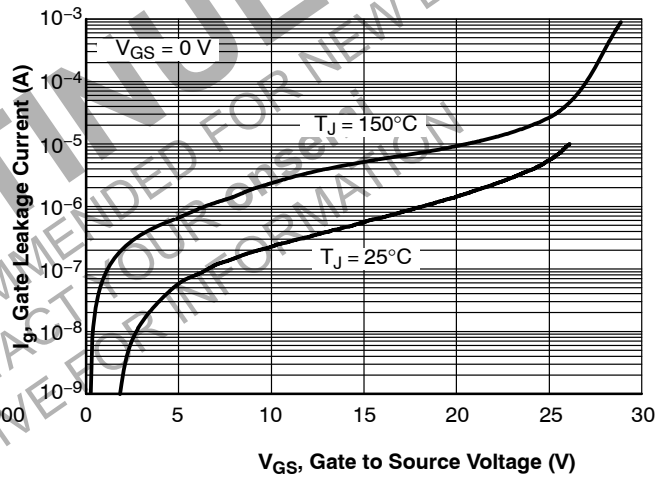



**Figure 10. Gate Leakage Current vs Gate to Source Voltage**

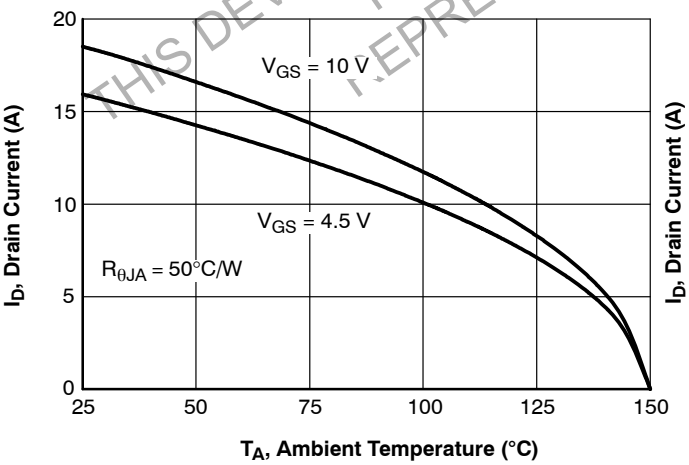



**Figure 11. Maximum Continuous Drain Current vs Ambient Temperature**

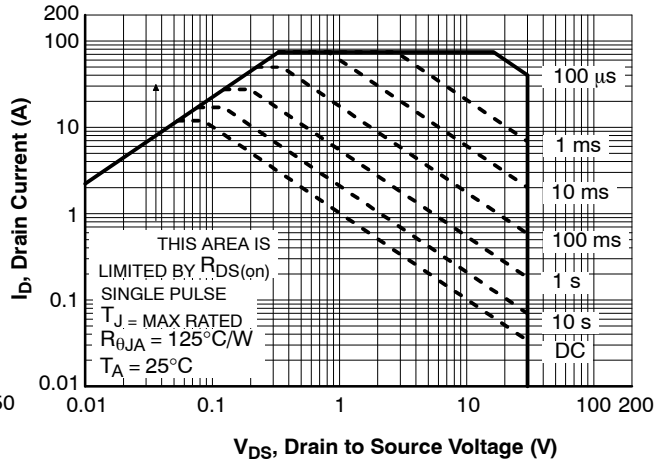



**Figure 12. Forward Bias Safe Operating Area**

## TYPICAL CHARACTERISTICS (CONTINUED)

($T_J$ = 25 °C unless otherwise noted)

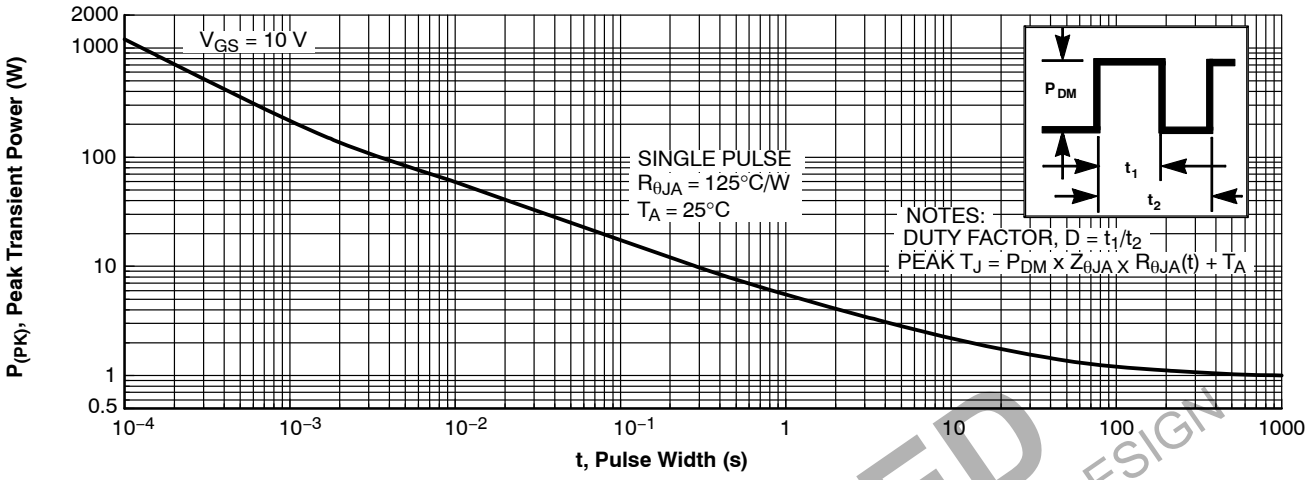



**Figure 13. Single Pulse Maximum Power Dissipation**

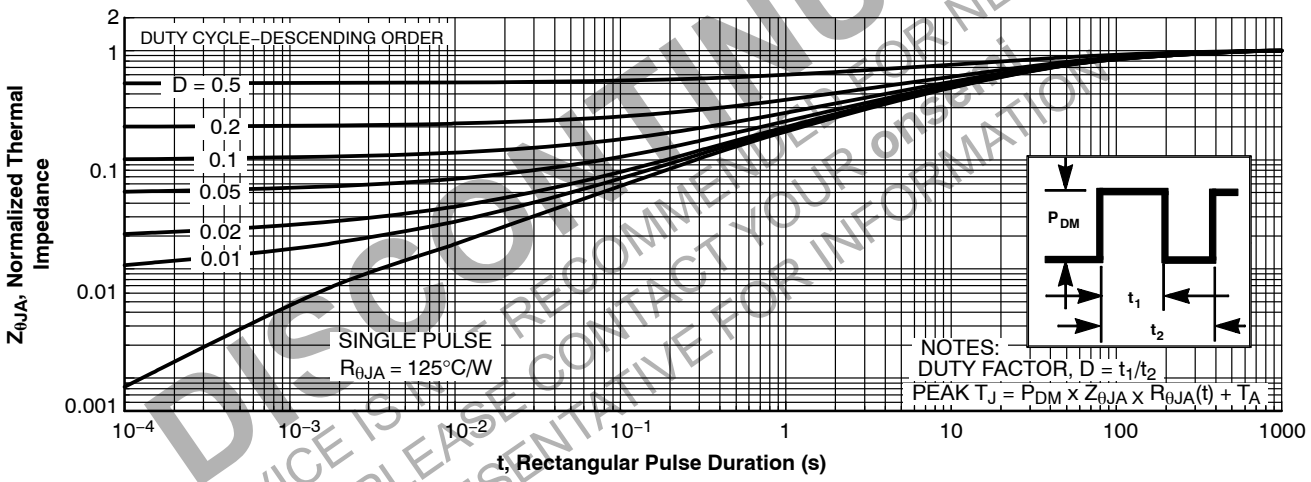



**Figure 14. Junction–to–Ambient Transient Thermal Response Curve**

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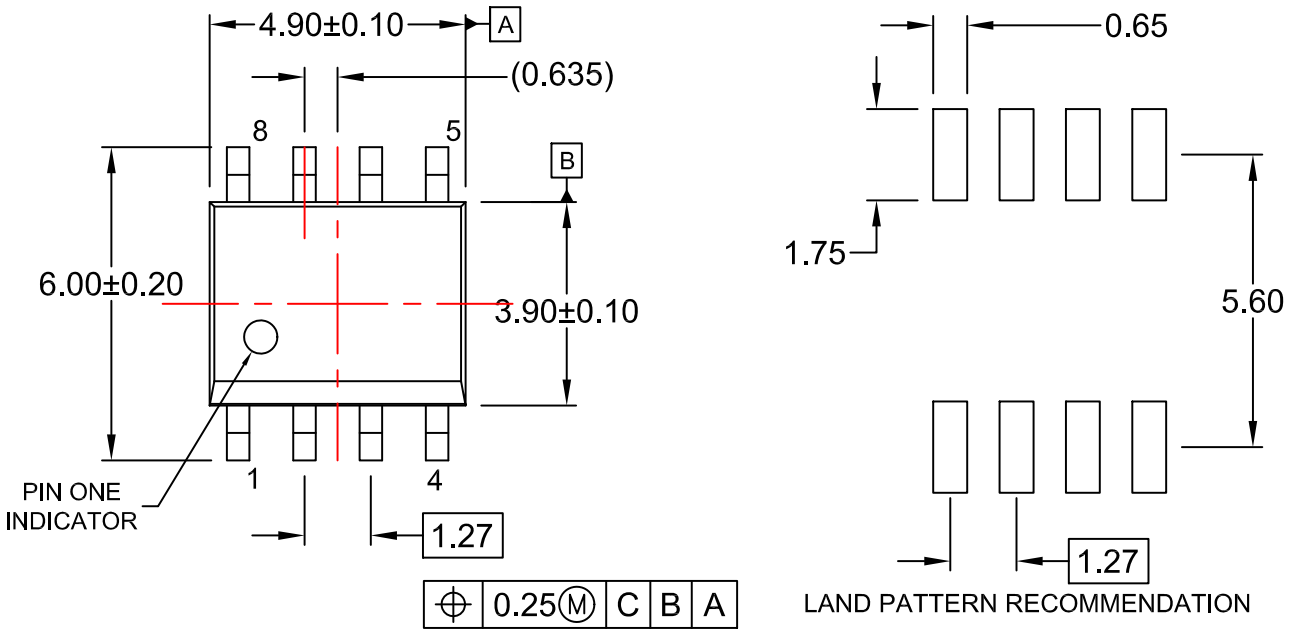
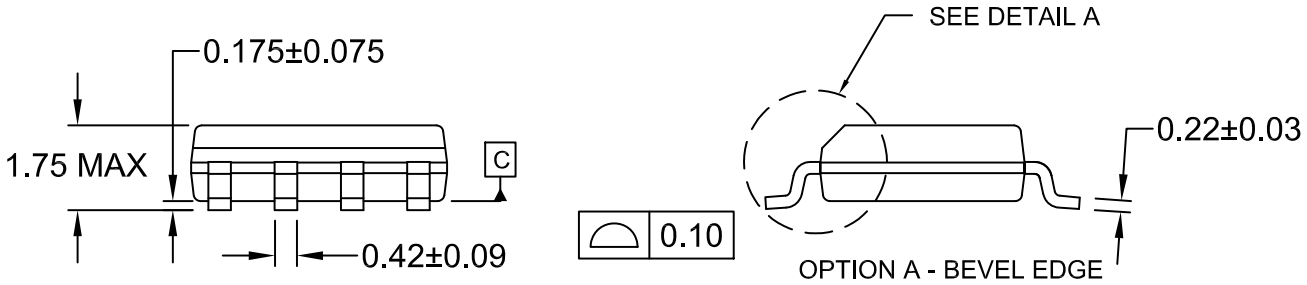
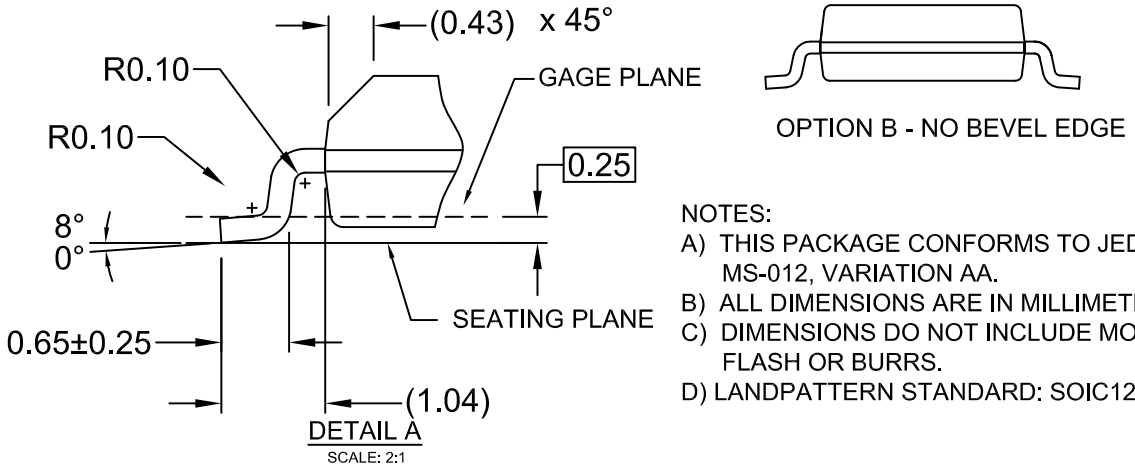
ISSUE A

DATE 24 AUG 2017




NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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