MOSFET – N-Channel, POWERTRENCH®

60 V, 77 A, 4.1 mΩ

FDPF041N06BL1-F154

ON Semiconductor®

www.onsemi.com

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
60 V	4.1 mΩ @ 10 V	77 A

Description

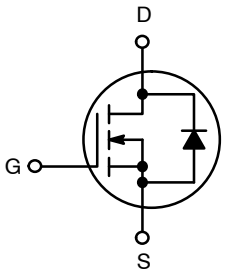
This N−Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that has been tailored to minimize the on−state resistance while maintaining superior switching performance.

Features

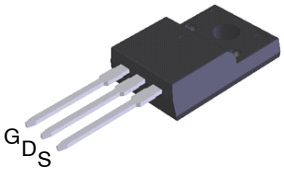
- $R_{DS(on)}$ = 3.5 mΩ (Typ.)@ V_{GS} = 10 V, I_D = 77 A
- Low FOM $R_{DS(on)}$*Q_G
- Low Reverse Recovery Charge, Q_{rr}
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System

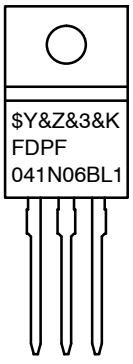


MOSFET



TO−220F Ultra Narrow Lead
CASE 221BN

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDPF041N06BL1	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		60	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	− Continuous (T_C = 25°C, Silicon Limited)	77	A
		− Continuous (T_C = 100°C, Silicon Limited)	55	
I_{DM}	Drain Current	− Pulsed (Note 1)	308	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		365	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	44.1	W
		− Derate Above 25°C	0.29	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8″ from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 3 mH, I_{AS} = 15,6 A, starting T_J = 25°C.
3. $I_{SD} \le$ 100 A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Quantity
FDPF041N06BL1−F154	FDPF041N06BL1	TO−220F (Pb−Free)	50 Units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	60	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.03	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	–	4	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 77 A	–	3.5	4.1	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 77 A	–	125	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	–	4280	5690	pF
C_{oss}	Output Capacitance		–	1050	1400	pF
C_{rss}	Reverse Transfer Capacitance		–	23	–	pF
$C_{oss(er)}$	Energy Related Output Capacitance	V_{DS} = 30 V, V_{GS} = 0 V	–	1787	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 30 V, I_D = 100 A, V_{GS} = 10 V (Note 4)	–	53	69	nC
Q_{gs}	Gate to Source Gate Charge		–	23	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	8	–	nC
$V_{plateau}$	Gate Plateau Voltage		–	5.7	–	V
Q_{sync}	Total Gate Charge Sync.	V_{DS} = 0 V, I_D = 50 A	–	48.6	–	nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V	–	63.8	–	nC
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 100 A, V_{GS} = 10 V, R_{GEN} = 4.7 Ω (Note 4)	–	29	68	ns
t_r	Turn-On Rise Time		–	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		–	38	86	ns
t_f	Turn-Off Fall Time		–	11	32	ns
ESR	Equivalent Series Resistance (G−S)	f = 1 MHz	–	0,8	–	Ω
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	77	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	308	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 77 A	–	–	1.25	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 100 A, dI_F/dt = 100 A/μs	–	65	–	ns
Q_{rr}	Reverse Recovery Charge		–	63	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

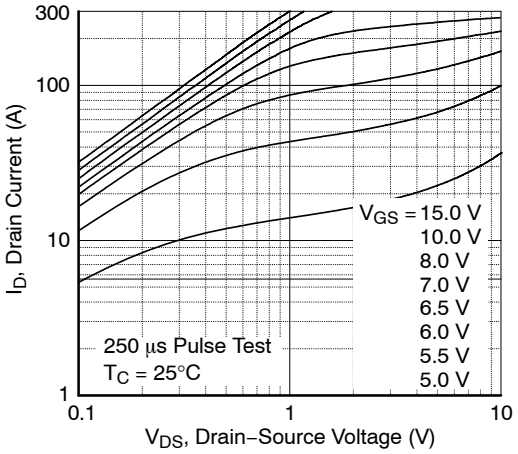


Figure 1. On−Region Characteristics

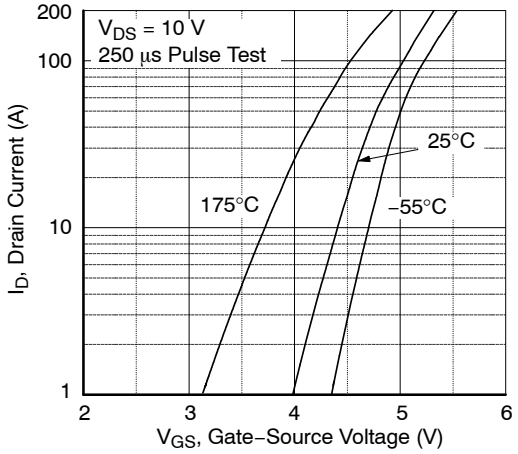


Figure 2. Transfer Characteristics

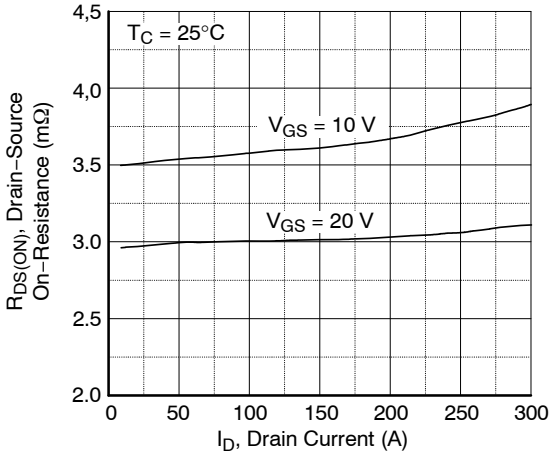


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

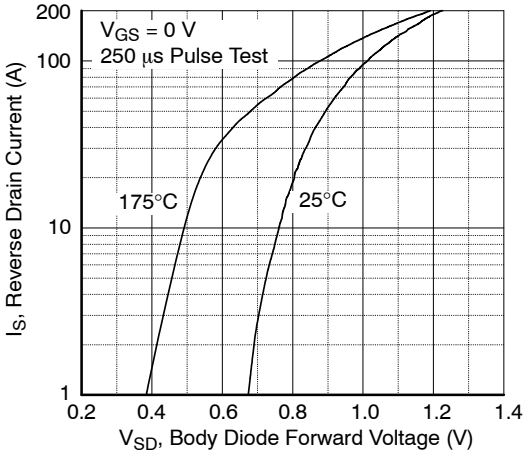


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

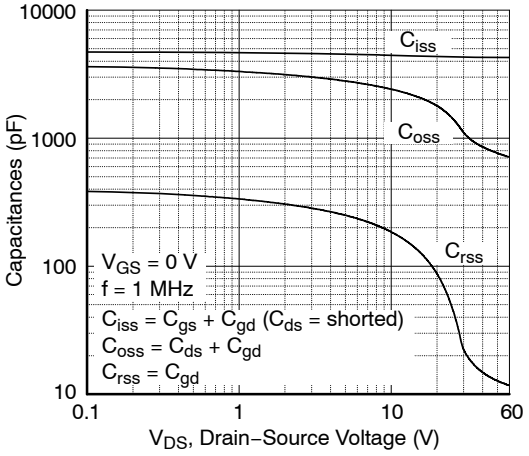


Figure 5. Capacitance Characteristics

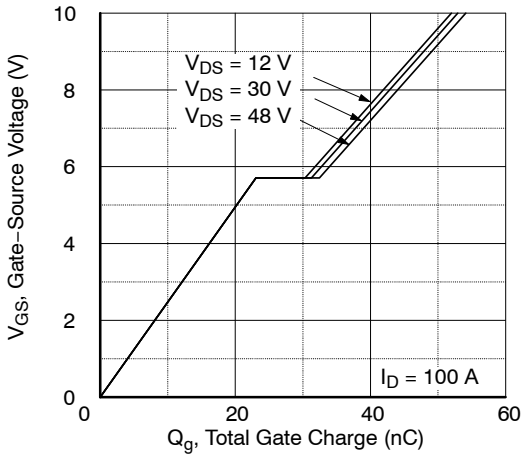


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

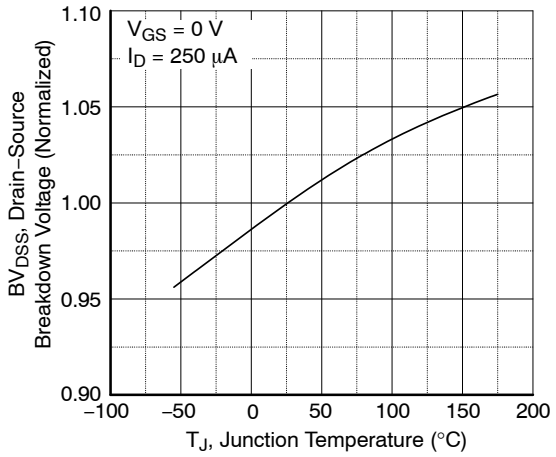


Figure 7. Breakdown Voltage Variation vs. Temperature

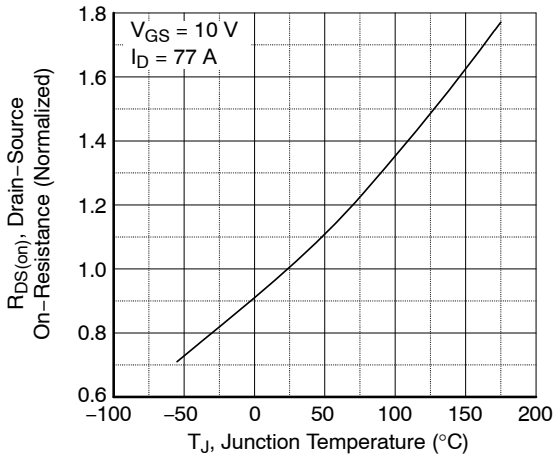


Figure 8. On−Resistance Variation vs. Temperature

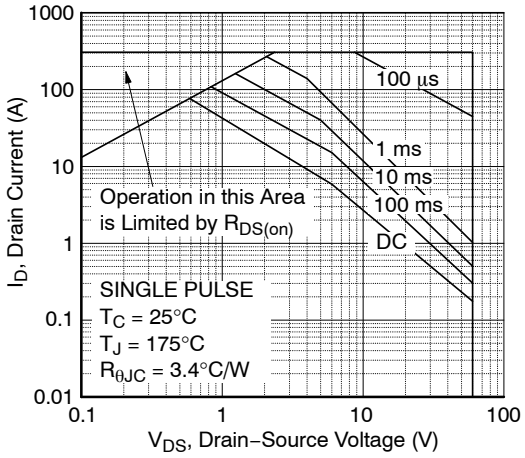


Figure 9. Maximum Safe Operating Area vs. Case Temperature

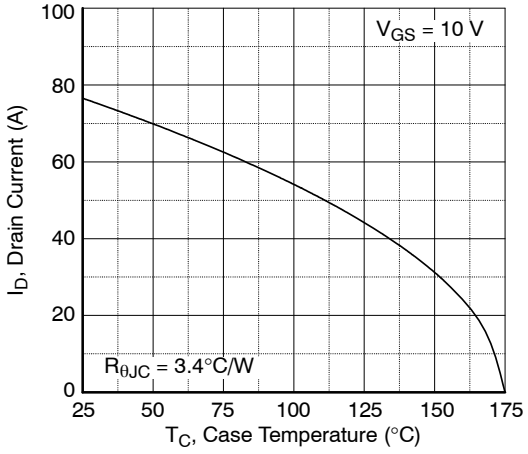


Figure 10. Maximum Drain Current

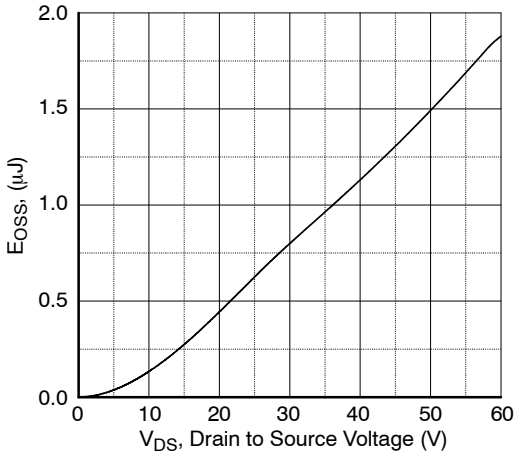


Figure 11. E_{OSS} vs. Drain to Source Voltage

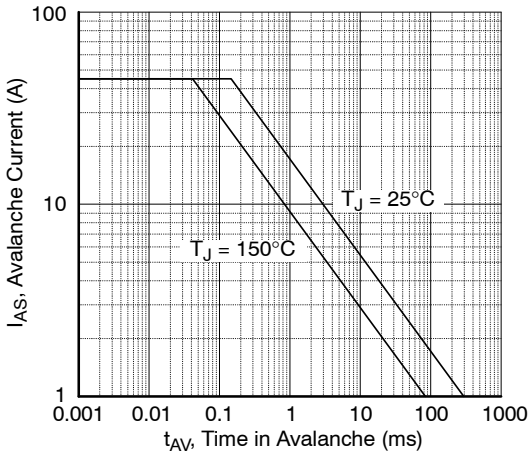


Figure 12. Unclamped Inductive Switching Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

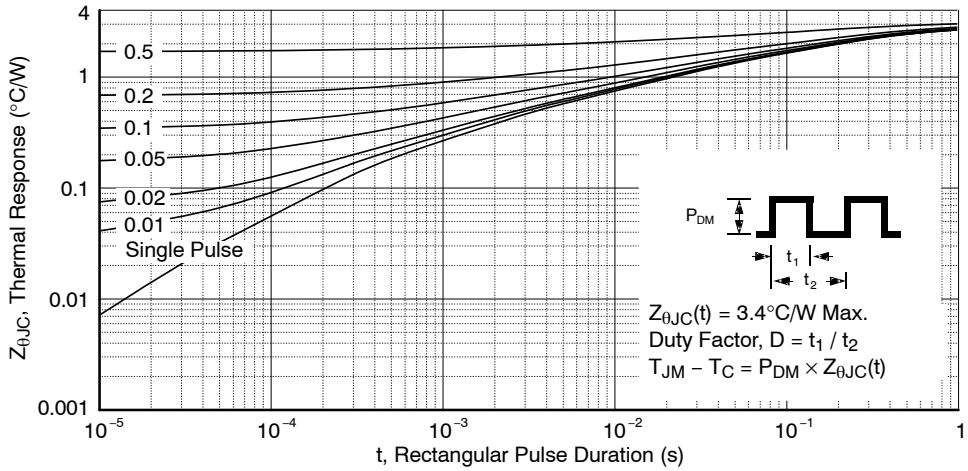


Figure 13. Transient Thermal Response Curve

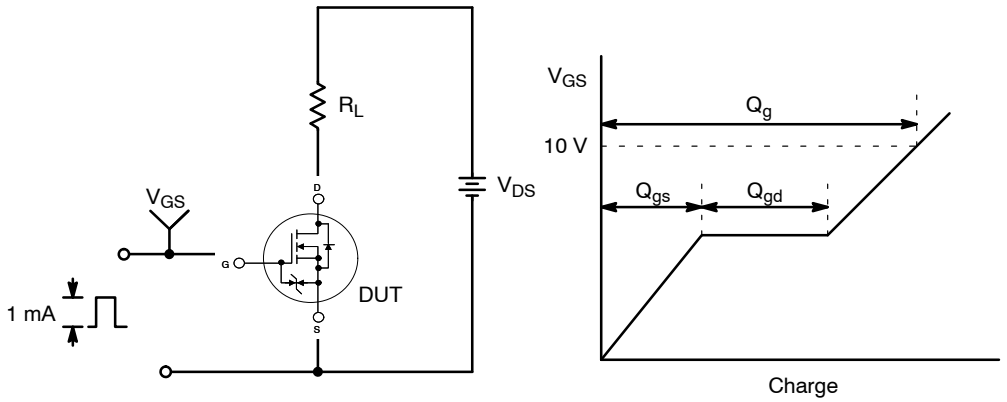


Figure 14. Gate Charge Test Circuit & Waveform

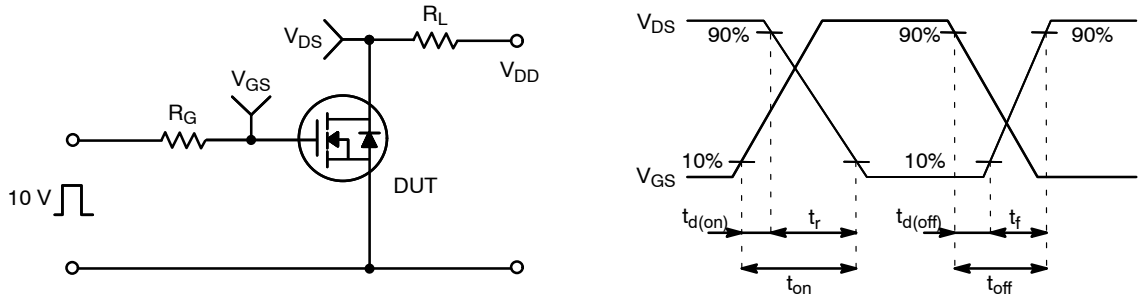


Figure 15. Resistive Switching Test Circuit & Waveforms

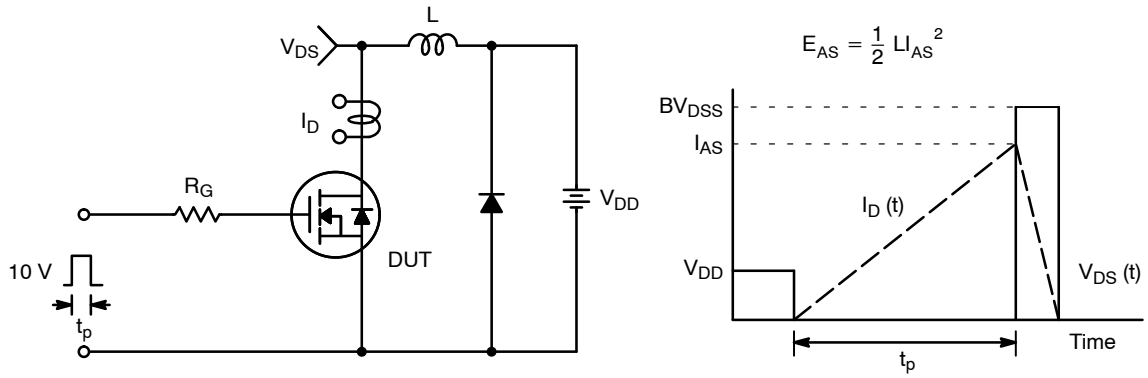


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

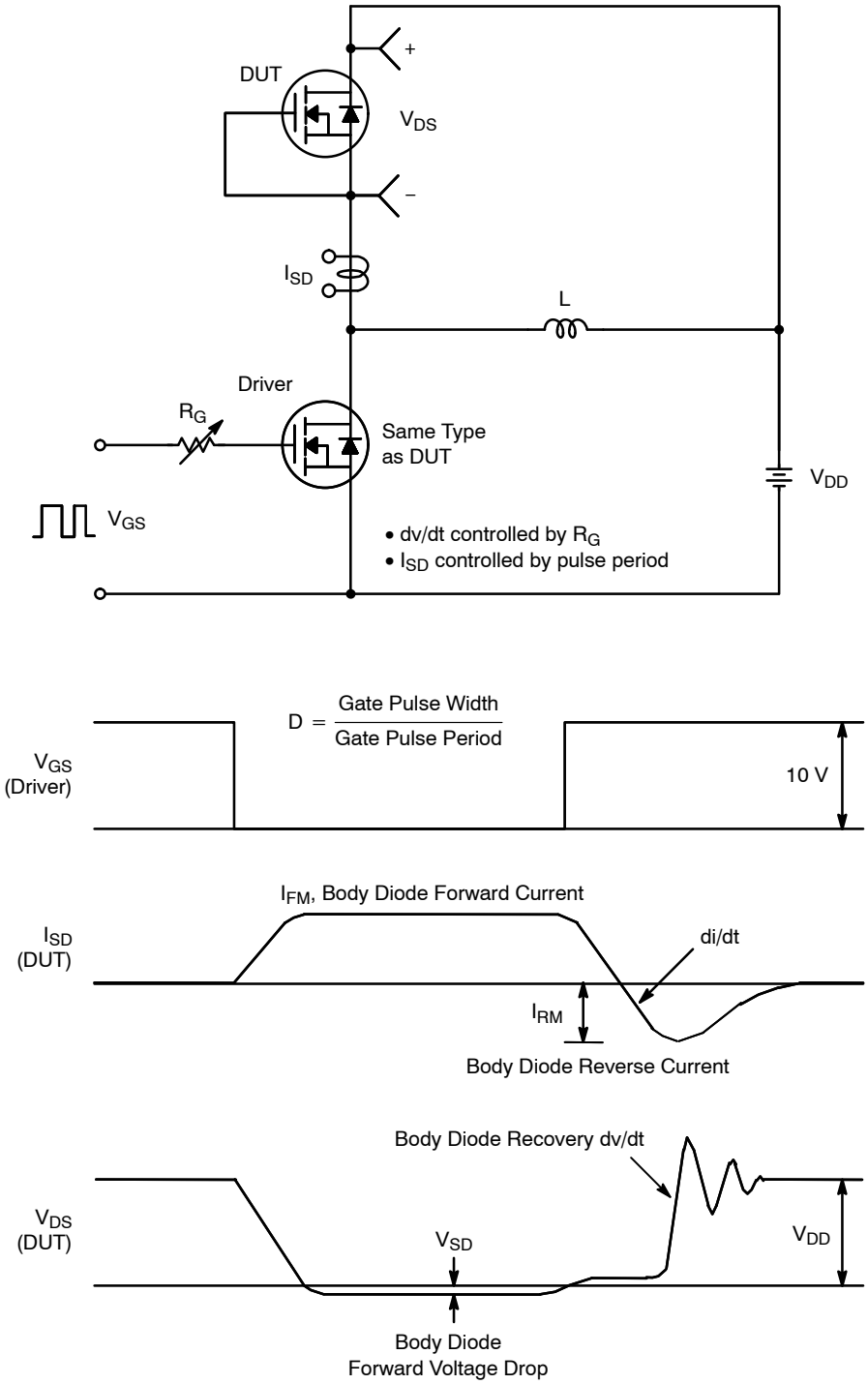


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

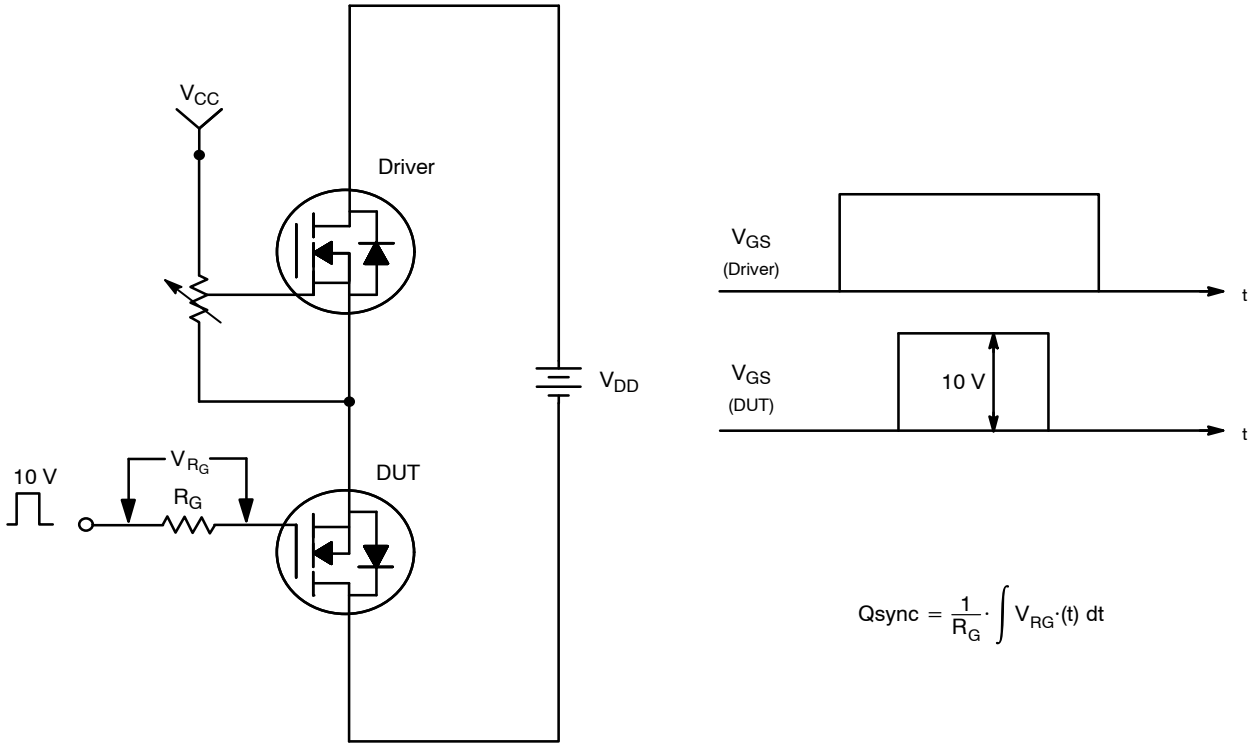
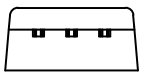


Figure 18. Total Gate Charge Qsync. Test Circuit & Waveforms

TO−220 FULLPACK, 3−LEAD (ULTRA NARROW LEAD)

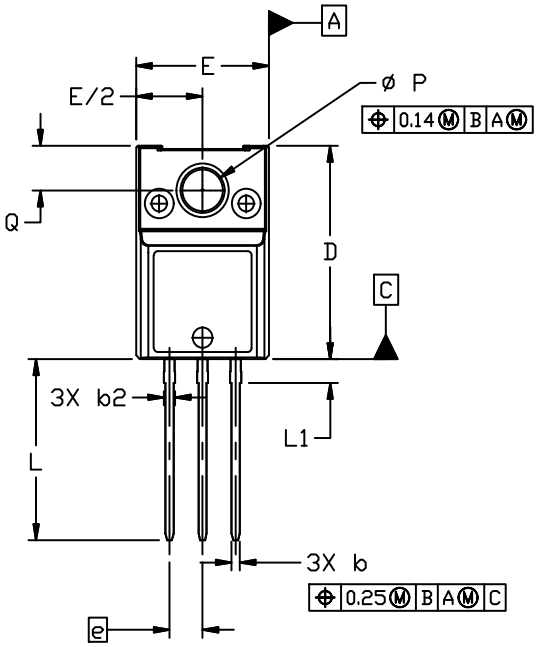
CASE 221BN
ISSUE A

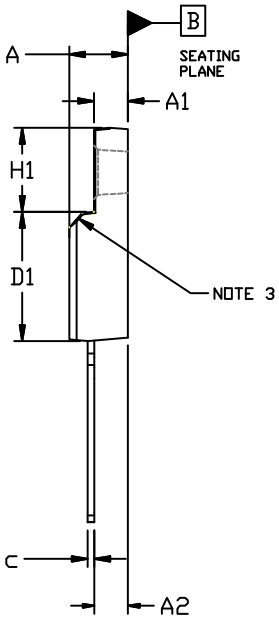
DATE 07 MAY 2021



NOTES:

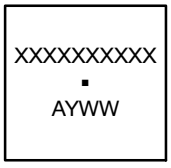
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS EXCLUDE BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS.





DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
A1	2.50	2.60	2.70
A2	2.47	2.57	2.67
b	0.56	0.63	0.69
b2	---	---	0.90
c	0.46	0.53	0.59
D	15.80	16.00	16.20
D1	9.58	9.68	9.78
E	10.00	10.20	10.40
e	2.54 BSC		
H1	6.32 REF		
L	13.45	13.60	13.75
L1	1.70	1.80	1.90
P	3.00	3.10	3.20
Q	3.25	3.35	3.45

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TO−220 FULLPACK, 3−LEAD (ULTRA NARROW LEAD)	PAGE 1 OF 1

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