

MOSFET – N-Channel, UniFET™

200 V, 52 A, 49 mΩ

FDP52N20

Description

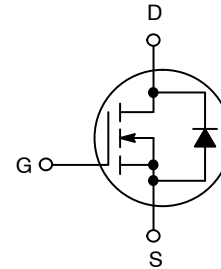
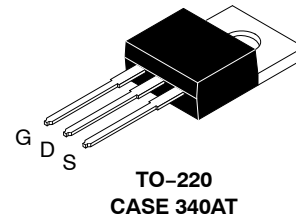
UniFET MOSFET is onsemi's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

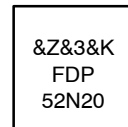
- $R_{DS(on)} = 41 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 26 \text{ A}$
- Low Gate Charge (Typ. 49 nC)
- Low C_{RSS} (Typ. 66 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

- PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply



MARKING DIAGRAM



&Z = Assembly Code
 &3 = Date Code (Year & Week)
 &K = Lot Run Traceability Code
 FDP52N20 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

FDP52N20

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	200	V
V _{GSS}	Gate to Source Voltage	±30	V
I _D	Drain Current	Continuous (T _C = 25°C)	52
		Continuous (T _C = 100°C)	33
I _{DM}	Drain Current	Pulsed (Note 1)	208
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	2520	mJ
I _{AR}	Avalanche Current (Note 1)	52	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	35.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P _D	Power Dissipation	(T _C = 25°C)	357
		Derate Above 25°C	2.86
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 1.4 mH, I_{AS} = 52 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 52 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.35	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA, T _J = 25°C	200	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.2	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 200 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 160 V, T _C = 125°C	–	–	10	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	3.0	–	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 26 A	–	0.041	0.049	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 26 A	–	35	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	2230	2900	pF
C _{oss}	Output Capacitance		–	540	700	pF
C _{rss}	Reverse Transfer Capacitance		–	66	100	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 160 V, I _D = 52 A, V _{GS} = 10 V (Note 5)	–	49	63	nC
Q _{gs}	Gate to Source Gate Charge		–	19	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	24	–	nC

FDP52N20

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}$, $I_D = 20\text{ A}$, $R_G = 25\ \Omega$ (Note 5)	–	53	115	ns
t_r	Turn-On Rise Time		–	175	359	ns
$t_{d(off)}$	Turn-Off Delay Time		–	48	107	ns
t_f	Turn-Off Fall Time		–	29	68	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	52	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	204	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 52\text{ A}$	–	–	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $I_{SD} = 52\text{ A}$, $dI_F/dt = 100\text{ A}/\mu\text{s}$	–	162	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.3	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

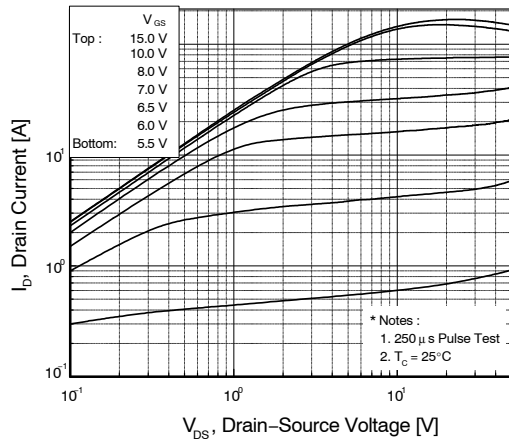


Figure 1. On-Region Characteristics

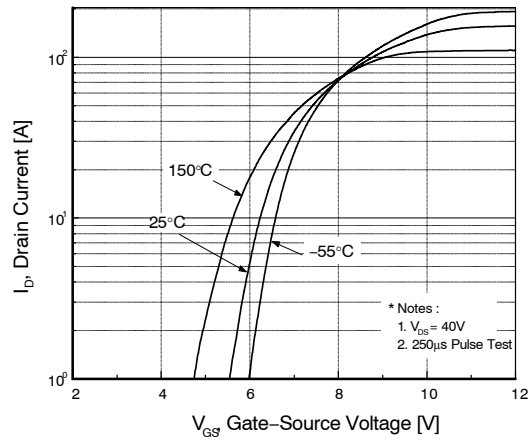


Figure 2. Transfer Characteristics

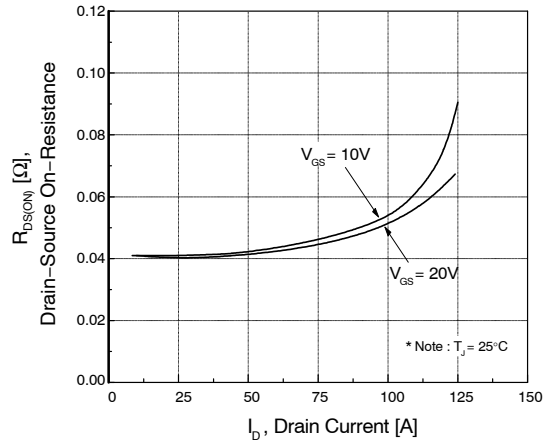


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

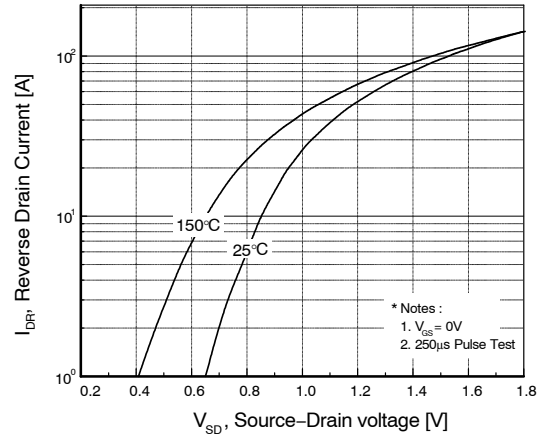


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

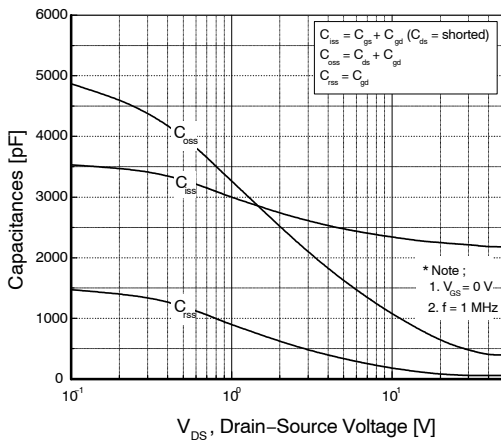


Figure 5. Capacitance Characteristics

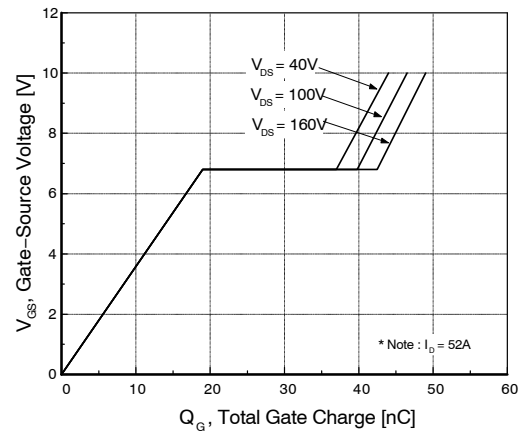


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

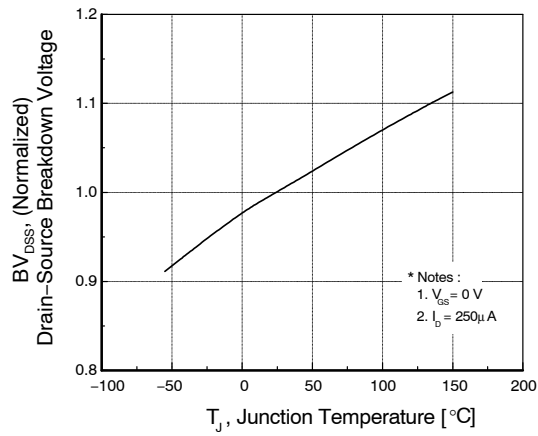


Figure 7. Breakdown Voltage Variation vs. Temperature

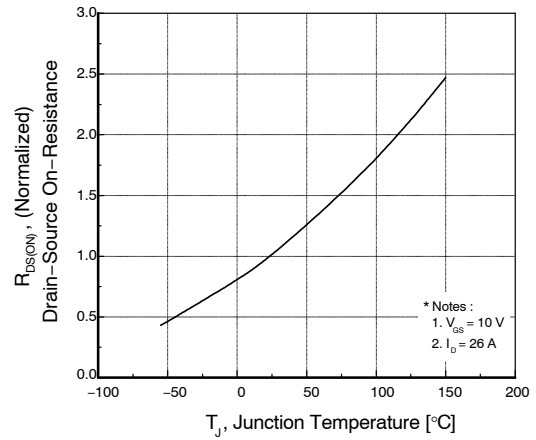


Figure 8. On-Resistance Variation vs. Temperature

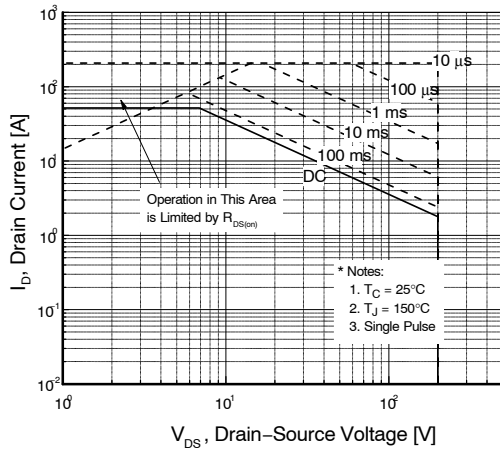


Figure 9. Maximum Safe Operation Area

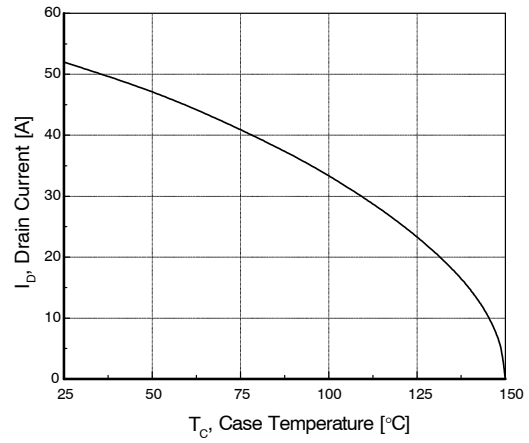


Figure 10. Maximum Drain Current

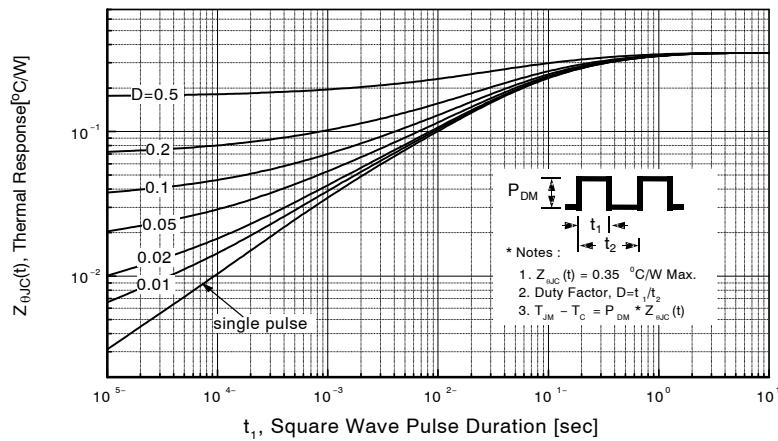


Figure 11. Transient Thermal Response Curve

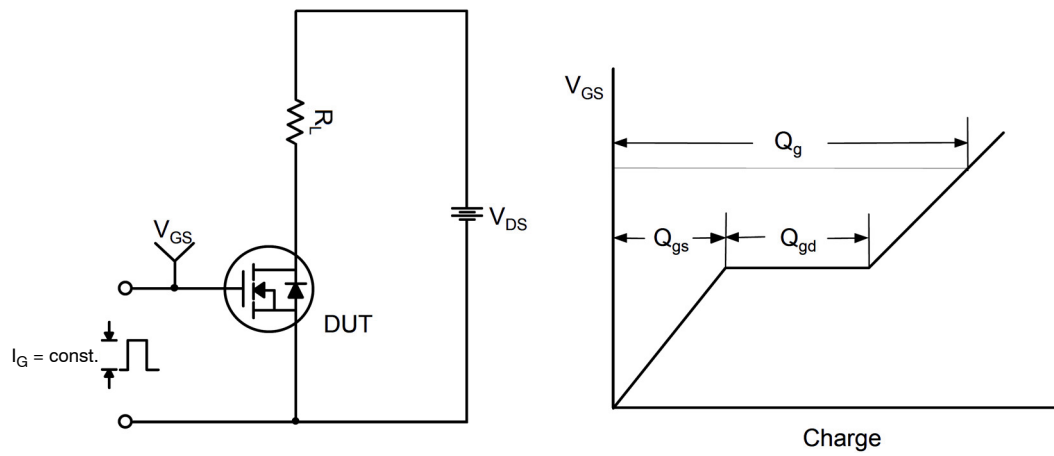


Figure 12. Gate Charge Test Circuit & Waveform

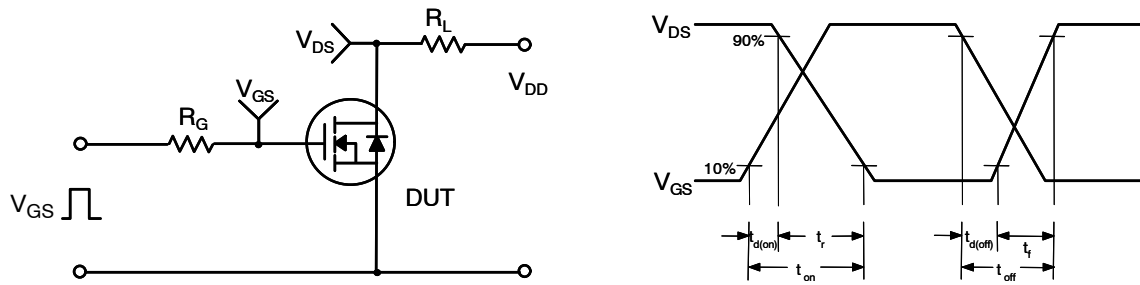


Figure 13. Resistive Switching Test Circuit & Waveforms

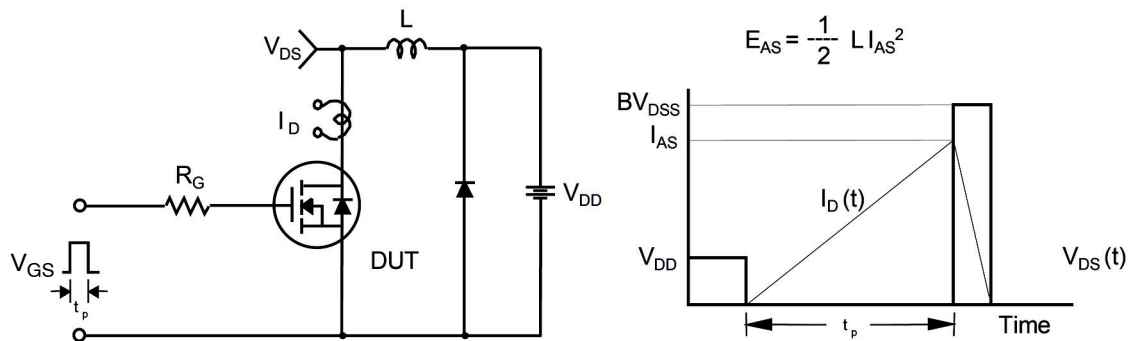
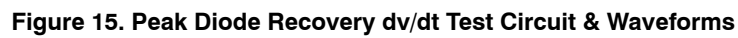


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

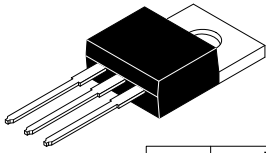
The diagram illustrates a switching transient test setup for a MOSFET DUT. The DUT is represented by a MOSFET symbol with its gate connected to a driver MOSFET. The driver MOSFET's gate is driven by a square-wave voltage source V_{GS} through a gate resistor R_G . The DUT's drain is connected to a load inductor L and a DC supply V_{DD} . The source of the DUT is connected to a current source I_{SD} and the source of the driver MOSFET. The drain-source voltage of the DUT is labeled V_{DS} . The current through the DUT is labeled I_{SD} . The driver MOSFET is labeled "Same Type as DUT".

- dv/dt controlled by R_G
- I_{SD} controlled by pulse period



Device	Device Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP52N20	FDP52N20	TO-220	Tube	N/A	N/A	1,000 Units / Tube

7



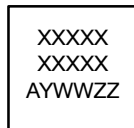
TO-220-3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

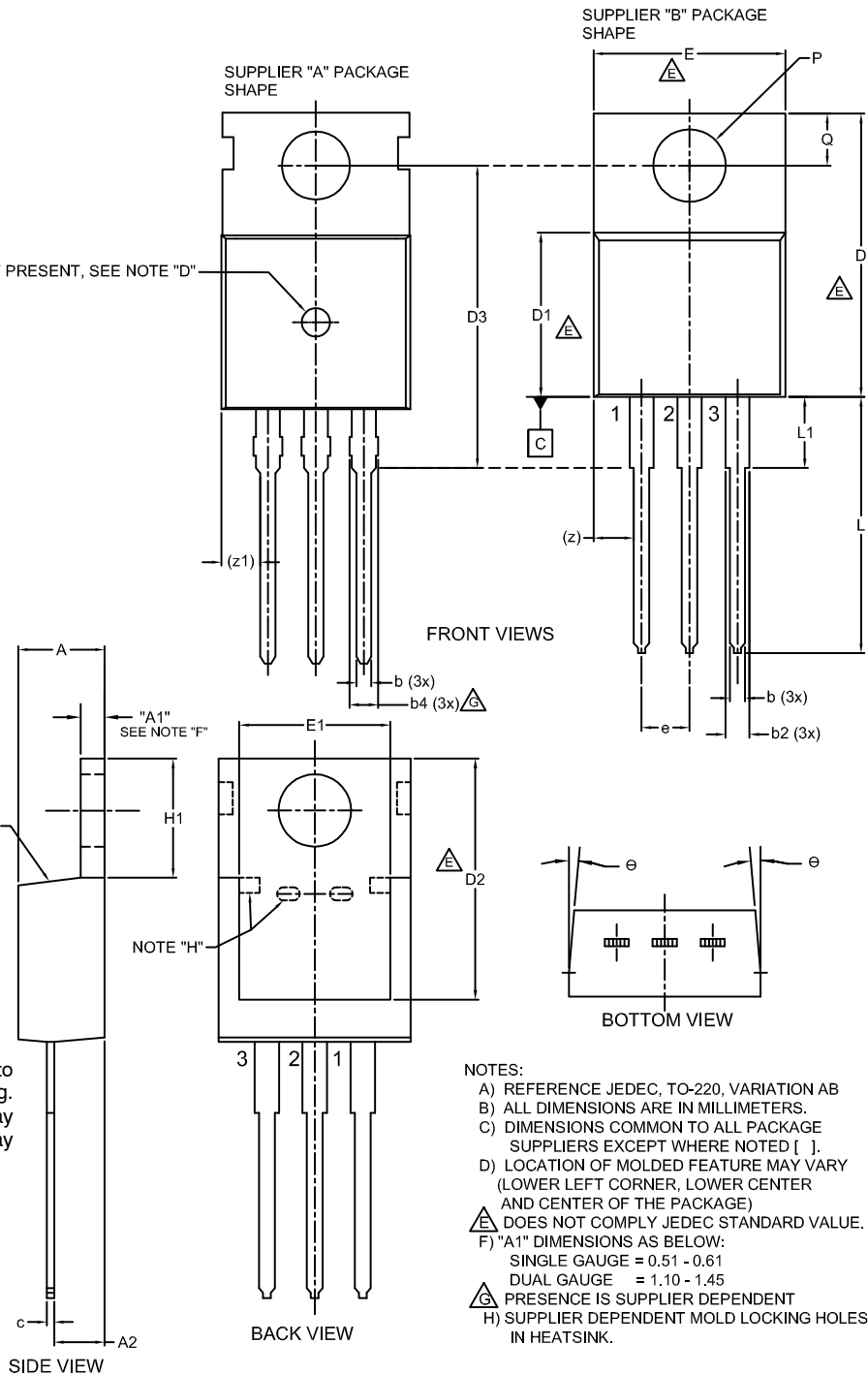
IF PRESENT, SEE NOTE "D"

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E) DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
- PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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