

MOSFET – N-Channel, POWERTRENCH®

150 V, 29 A, 54 mΩ

FDP2572

Features

- $R_{DS(on)} = 45 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 9 \text{ A}$
- $Q_{G(tot)} = 26 \text{ nC}$ (Typ.) @ $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- This Device is Pb-Free and Halide Free

Applications

- Consumer Appliances
- Synchronous Rectification
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

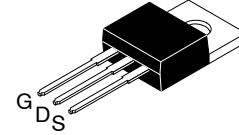
Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$)	29 A
		Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 10 \text{ V}$)	20 A
		Continuous ($T_{amb} = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $R_{\theta JA} = 43^\circ\text{C/W}$)	4 A
		Pulsed	Figure 4 A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	36	mJ
P_D	Power Dissipation	135	W
	Derate above 25°C	0.9	W/ $^\circ\text{C}$
T_J , T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

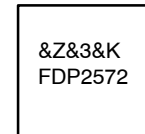
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.11	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2)	62.5	$^\circ\text{C/W}$

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
150 V	54 mΩ @ 10 V	29 A

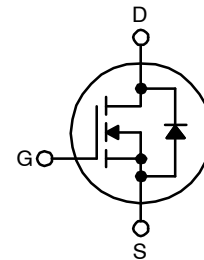


TO-220-3LD
CASE 340AT

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = 3-Digit Date Code
&K = 2-Digits Lot Run Traceability Code
FDP2572 = Specific Device Code



N-Channel

ORDERING INFORMATION

Device	Package	Shipping
FDP2572	TO-220-3LD	800 Units / Tube

FDP2572

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

B _{VDSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	150	–	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 120 V	–	–	1	μA
		V _{GS} = 0 V, V _{DS} = 120 V, T _C = 150°C	–	–	250	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(TH)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2	–	4	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10 V, I _D = 9 A	–	0.045	0.054	Ω
		V _{GS} = 6 V, I _D = 4 A	–	0.050	0.075	
		V _{GS} = 10 V, I _D = 9 A, T _C = 175°C	–	0.126	0.146	

DYNAMIC CHARACTERISTICS

C _{ISS}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	1770	–	pF
C _{OSS}	Output Capacitance		–	183	–	pF
C _{RSS}	Reverse Transfer Capacitance		–	40	–	pF
Q _{g(TOT)}	Total Gate Charge at 10 V	V _{DD} = 75 V, I _D = 9 A, I _g = 1.0 mA, V _{GS} = 0 V to 10 V	–	26	34	nC
Q _{g(TH)}	Threshold Gate Charge	V _{DD} = 75 V, I _D = 9 A, I _g = 1.0 mA, V _{GS} = 0 V to 2 V	–	3.3	4.3	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 75 V, I _D = 9 A, I _g = 1.0 mA	–	8	–	nC
Q _{gs2}	Gate Charge Threshold to Plateau		–	5	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	6	–	nC

RESISTIVE SWITCHING CHARACTERISTICS (V_{GS} = 10 V)

t _{ON}	Turn-On Time	V _{DD} = 75 V, I _D = 9 A, V _{GS} = 10 V, R _{GS} = 11.0 Ω	–	–	36	ns
t _{d(ON)}	Turn-On Delay Time		–	11	–	ns
t _r	Rise Time		–	14	–	ns
t _{d(OFF)}	Turn-Off Delay Time		–	31	–	ns
t _f	Fall Time		–	14	–	ns
t _{OFF}	Turn-Off Time		–	–	66	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Voltage	I _{SD} = 9 A	–	–	1.25	V
		I _{SD} = 4 A	–	–	1.0	V
t _{rr}	Reverse Recovery Time	I _{SD} = 9 A, dI _{SD} /dt = 100 A/μs	–	–	74	ns
Q _{RR}	Reverse Recovered Charge	I _{SD} = 9 A, dI _{SD} /dt = 100 A/μs	–	–	169	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Starting T_J = 25°C, L = 0.2 mH, I_{AS} = 19 A.
- Pulse Width = 100 μs

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

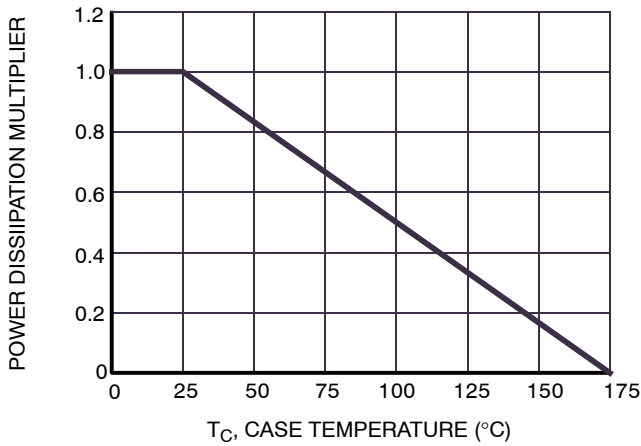


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

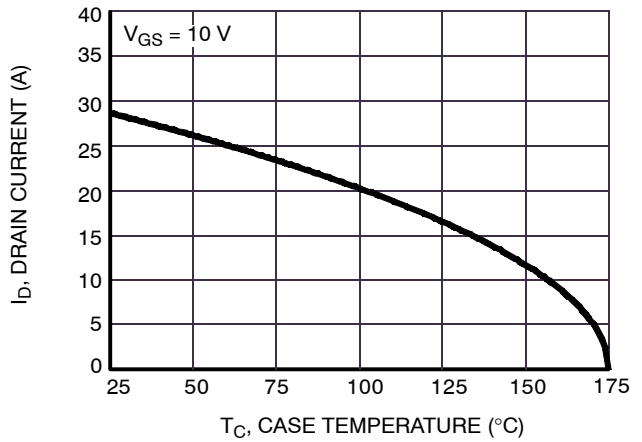


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

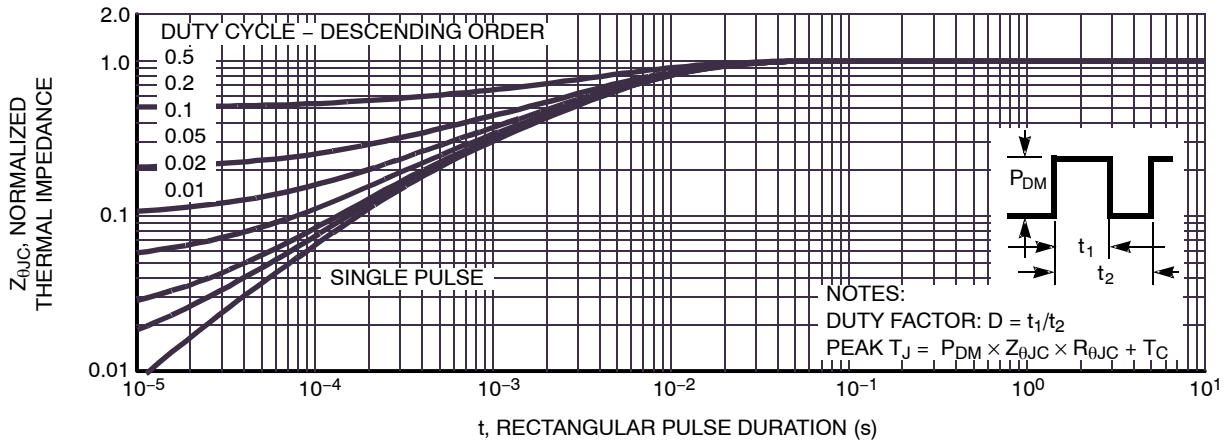


Figure 3. Normalized Maximum Transient Thermal Impedance

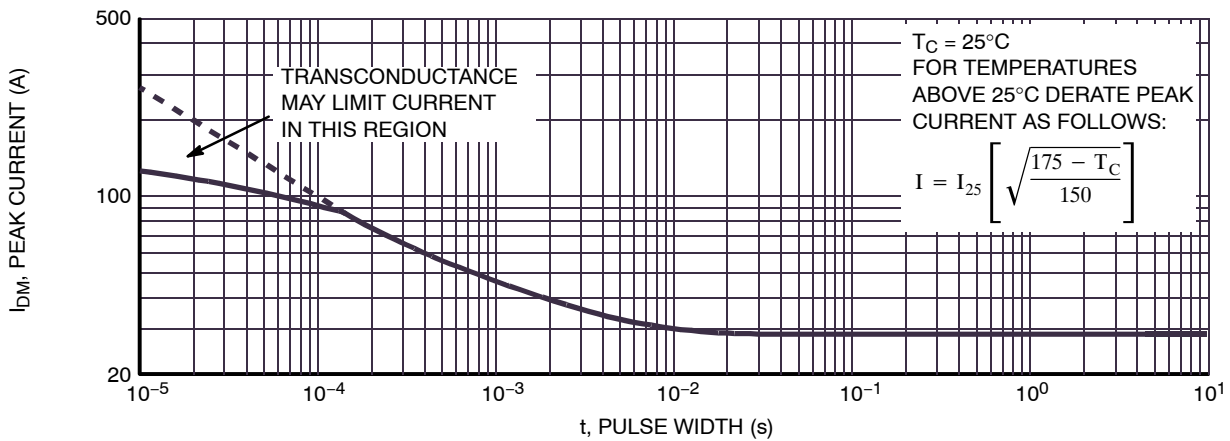


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

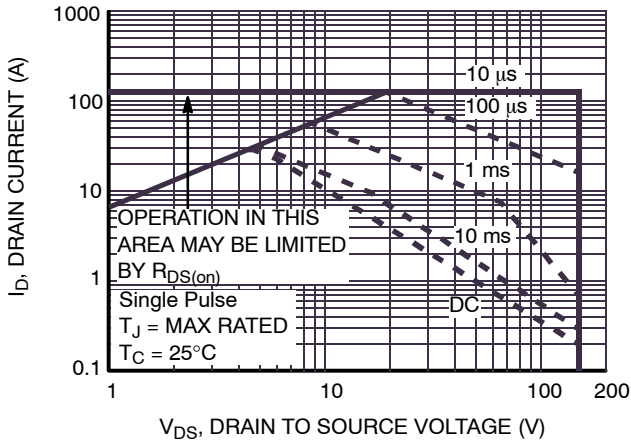


Figure 5. Forward Bias Safe Operating Area

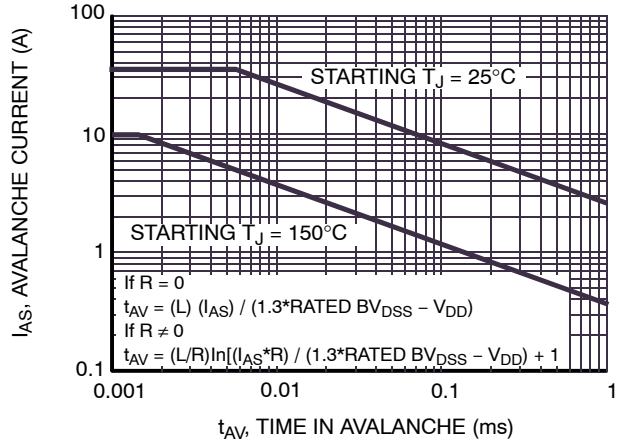


Figure 6. Unclamped Inductive Switching Capability

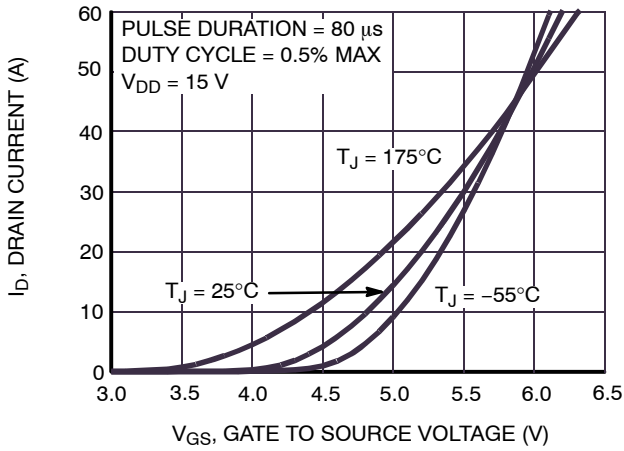


Figure 7. Transfer Characteristics

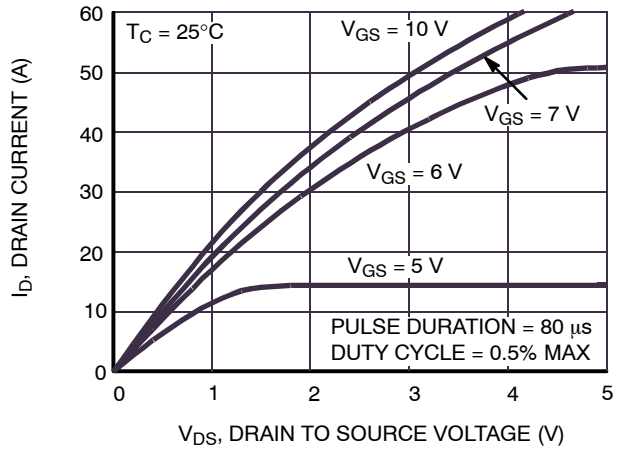


Figure 8. Saturation Characteristics

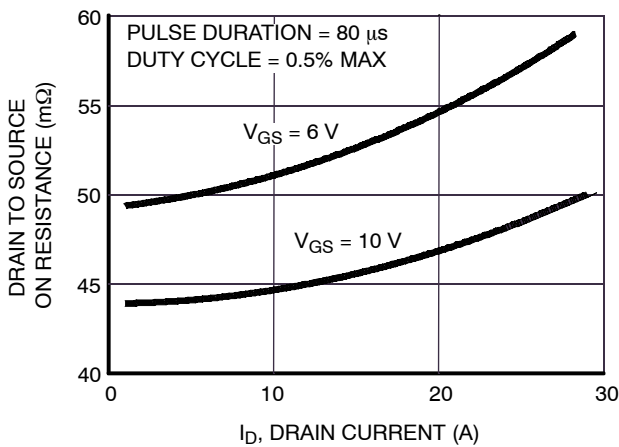


Figure 9. Drain to Source On Resistance vs. Drain Current

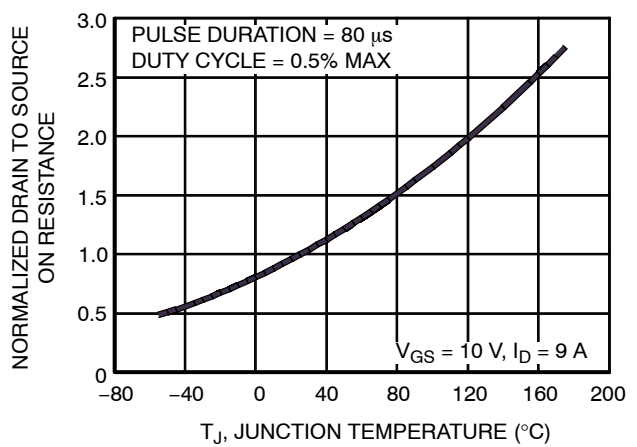


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

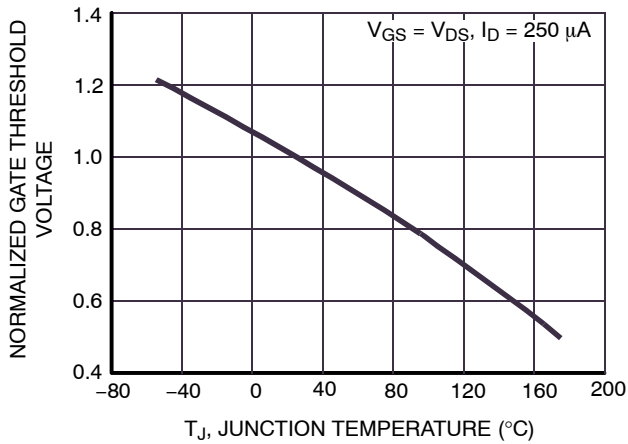


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

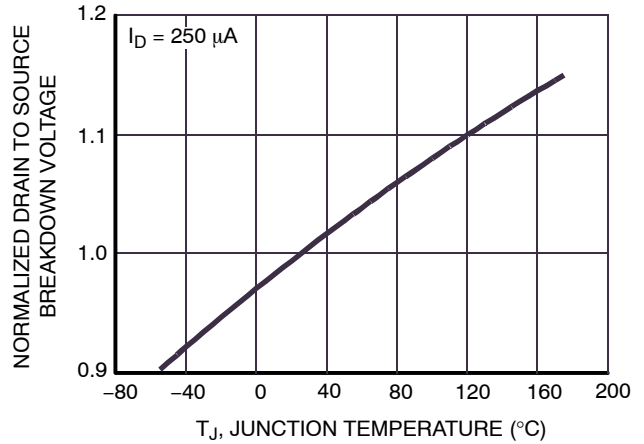


Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

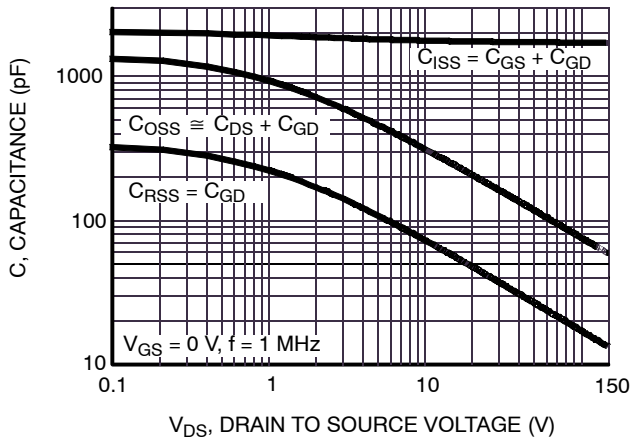


Figure 13. Capacitance vs. Drain to Source Voltage

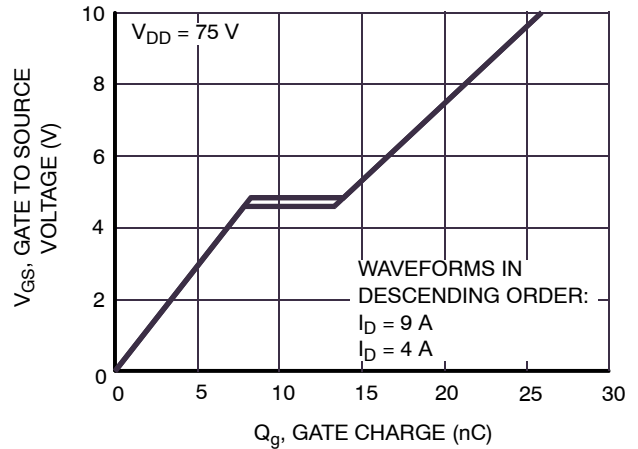


Figure 14. Gate Charge Waveforms for Constant Gate Currents

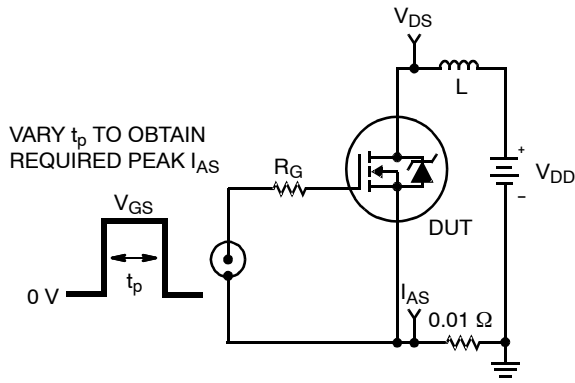


Figure 15. Unclamped Energy Test Circuit

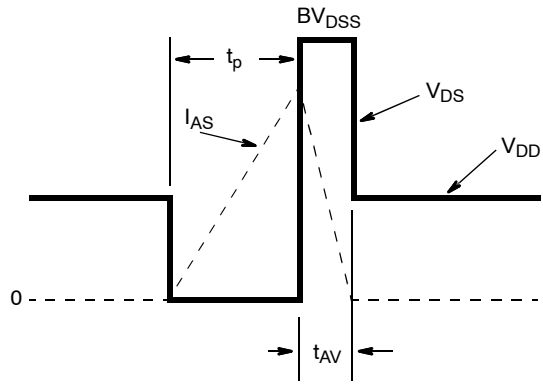


Figure 16. Unclamped Energy Waveforms

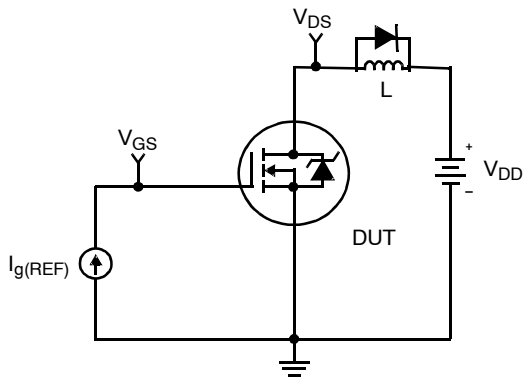


Figure 17. Gate Charge Test Circuit

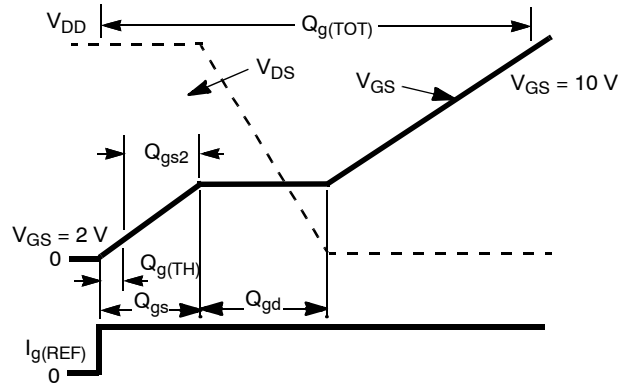


Figure 18. Gate Charge Waveforms

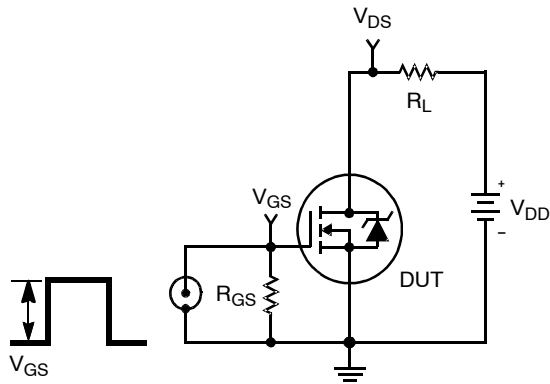


Figure 19. Switching Time Test Circuit

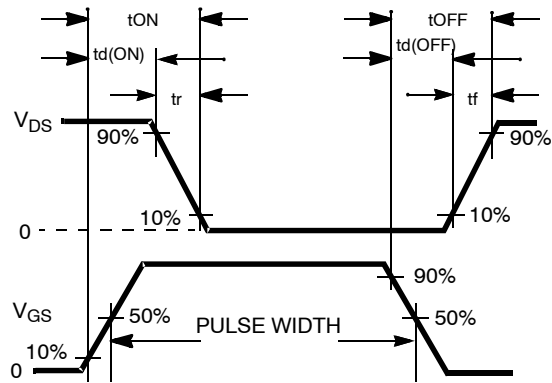


Figure 20. Switching Time Waveforms

FDP2572

PSPICE Electrical Model

```
.SUBCKT FDP2572 2 1 3 ; rev April 2002
CA 12 8 5.5e-10
Cb 15 14 7.4e-10
Cin 6 8 1.7e-9
```

```
Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD
```

```
Ebreak 11 7 17 18 160
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evttemp 20 6 18 22 1
```

```
It 8 17 1
```

```
Lgate 1 9 9.56e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 7.71e-9
```

```
RLgate 1 9 95.6
RLdrain 2 5 10
RLsource 3 7 77.1
```

```
Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD
```

```
Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 35e-3
Rgate 9 20 1.6
RSLC1 5 51 RSLCMOD 1.0e-6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 3.0e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD
```

```
Vbat 22 19 DC 1
```

```
ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)/(1e-6*52),3)) }
```

```
.MODEL DbodyMOD D (IS=6.0E-11 N=1.14 RS=3.9e-3 TRS1=3.5e-3 TRS2=3.0e-6
+ CJO=1.1e-9 M=0.63 TT=6.2e-8 XTI=4.5)
```

```
.MODEL DbreakMOD D (RS=10 TRS1=5.0e-3 TRS2=-5.0e-6)
```

```
.MODEL DplcapMOD D (CJO=3.5e-10 IS=1.0e-30 N=10 M=0.65)
```

```
.MODEL MmedMOD NMOS (VTO=3.55 KP=3 IS=1e-40 N=10 TOX=1 L=1u W=1u RG=1.6)
```

```
.MODEL MstroMOD NMOS (VTO=4.0 KP=25 IS=1e-30 N=10 TOX=1 L=1u W=1u)
```

```
.MODEL MweakMOD NMOS (VTO=2.95 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=16 RS=0.1)
```

```
.MODEL RbreakMOD RES (TC1=1.15e-3 TC2=-9.5e-7)
```

```
.MODEL RdrainMOD RES (TC1=9.0e-3 TC2=2.5e-5)
```

```
.MODEL RSLCMOD RES (TC1=3.0e-3 TC2=2.5e-6)
```

```
.MODEL RsourceMOD RES (TC1=4.0e-3 TC2=1.0e-6)
```

```
.MODEL RvthresMOD RES (TC1=-4.1e-3 TC2=-1.0e-5)
```

```
.MODEL RvtempMOD RES (TC1=-4.0e-3 TC2=1.0e-6)
```

```
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-3.5)
```

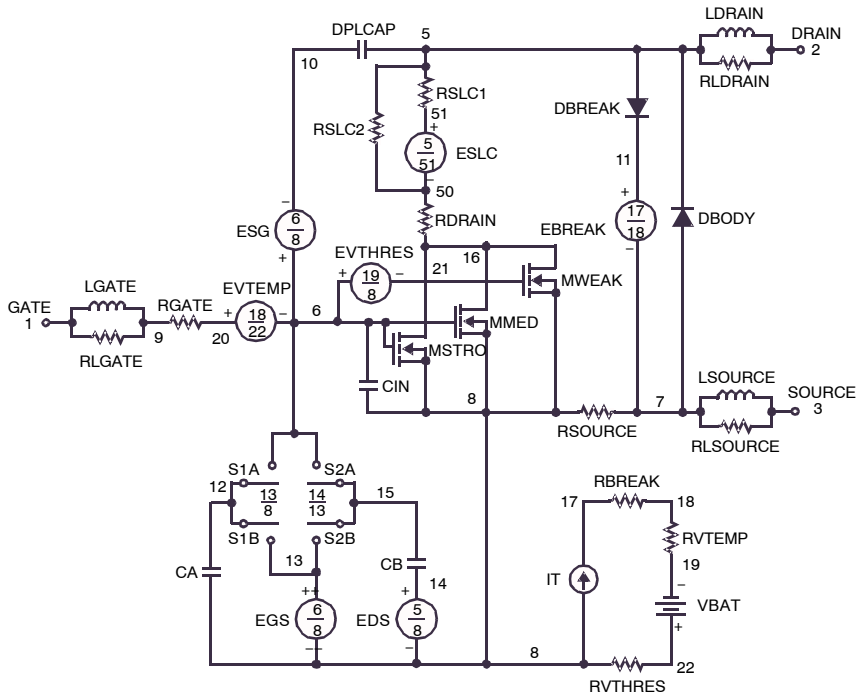
```
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-5.0)
```

```
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.3)
```

```
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.5)
```

```
.ENDS
```

NOTE: For further discussion of the PSPICE model, consult *A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options*; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



FDP2572

SABER Electrical Model

```
REV April 2002
ttemplate FDB2572 n2,n1,n3
electrical n2,n1,n3
```

```
{
var i iscl
dp..model dbodymod = (is1=6.0e-11,n1=1.14,rs=3.9e-3,trs1=3.5e-3,trs2=3.0e-6,cjo=1.1e-9,m=0.63,tt=6.2e-8,xti=4.5)
dp..model dbreakmod = (rs=10,trs1=5.0e-3,trs2=-5.0e-6)
dp..model dplcapmod = (cjo=3.5e-10,is1=10.0e-30,n1=10,m=0.65)
m..model mmedmod = (type=_n,vto=3.55,kp=3,is=1e-40, tox=1)
m..model mstrongmod = (type=_n,vto=4.0,kp=25,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=2.95,kp=0.05,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model slbmod = (ron=1e-5,roff=0.1,von=-3.5,voff=-5.0)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.5,voff=0.3)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.3,voff=-0.5)
c.ca n12 n8 = 5.5e-10
c.cb n15 n14 = 7.4e-10
c.cin n6 n8 = 1.7e-9
```

```
dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod
```

```
spe.ebreak n11 n7 n17 n18 = 160
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
```

```
i.it n8 n17 = 1
```

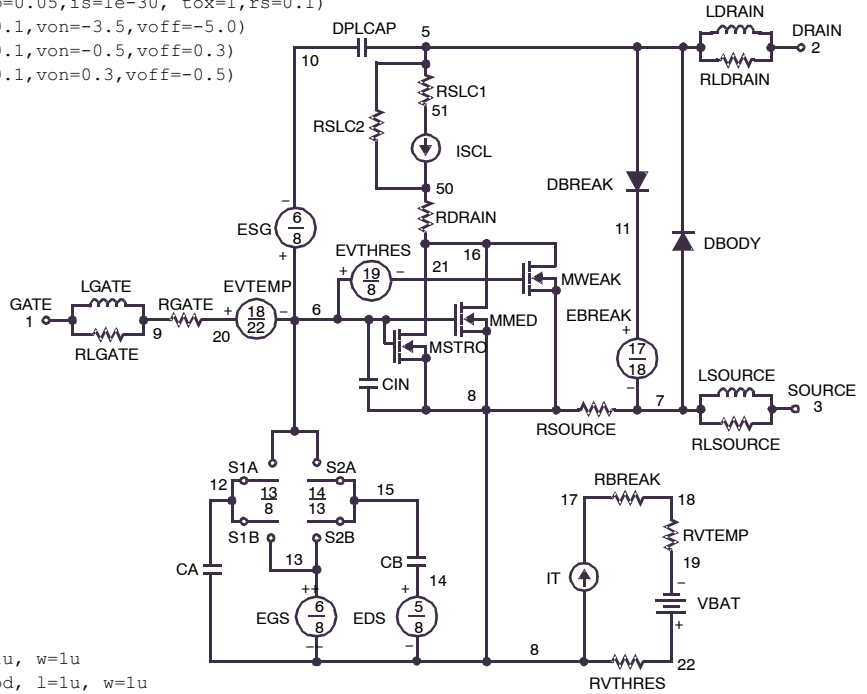
```
l.lgate n1 n9 = 9.56e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 7.71e-9
```

```
res.rlgate n1 n9 = 95.6
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 77.1
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
res.rbreak n17 n18 = 1, tc1=1.15e-3,tc2=-9.5e-7
res.rdrain n50 n16 = 35e-3, tc1=9.0e-3,tc2=2.5e-5
res.rgate n9 n20 = 1.6
res.rslc1 n5 n51 = 1.0e-6, tc1=3.0e-3,tc2=2.5e-6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7 = 3.0e-3, tc1=4.0e-3,tc2=1.0e-6
res.rvthres n22 n8 = 1, tc1=-4.1e-3,tc2=-1.0e-5
res.rvtemp n18 n19 = 1, tc1=-4.0e-3,tc2=1.0e-6
```

```
sw_vcsp.sla n6 n12 n13 n8 = model=slamod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/52)** 3))
}
```



SABER Electrical Model

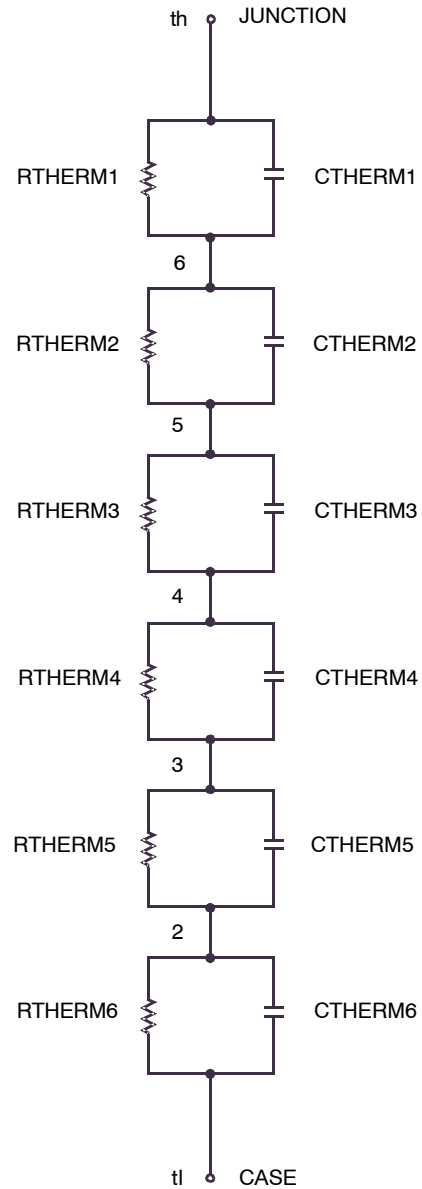
```

REV 26 April 2002
FDB2572
CTHERM1 TH 6 3.8e-3
CTHERM2 6 5 4.0e-3
CTHERM3 5 4 4.2e-3
CTHERM4 4 3 4.3e-3
CTHERM5 3 2 8.5e-3
CTHERM6 2 TL 3.0e-2
R THERM1 TH 6 5.5e-4
R THERM2 6 5 5.0e-3
R THERM3 5 4 4.5e-2
R THERM4 4 3 10.5e-2
R THERM5 3 2 3.7e-1
R THERM6 2 TL 3.8e-1
    
```

SABER Thermal Model

```

SABER thermal model FDB2572
template thermal_model th t1
thermal_c th, t1
{
ctherm.ctherm1 th 6 =3.8e-3
ctherm.ctherm2 6 5 =4.0e-3
ctherm.ctherm3 5 4 =4.2e-3
ctherm.ctherm4 4 3 =4.3e-3
ctherm.ctherm5 3 2 =8.5e-3
ctherm.ctherm6 2 t1 =3.0e-2
rtherm.rtherm1 th 6 =5.5e-4
rtherm.rtherm2 6 5 =5.0e-3
rtherm.rtherm3 5 4 =4.5e-2
rtherm.rtherm4 4 3 =10.5e-2
rtherm.rtherm5 3 2 =3.7e-1
rtherm.rtherm6 2 t1 =3.8e-1
}
    
```



MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



Scale 1:1

TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



- NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
 - D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
 - E) DOES NOT COMPLY JEDEC STANDARD VALUE.
 - F) "A1" DIMENSIONS AS BELOW:
 SINGLE GAUGE = 0.51 - 0.61
 DUAL GAUGE = 1.10 - 1.45
 - G) PRESENCE IS SUPPLIER DEPENDENT
 - H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	TO-220-3LD	PAGE 1 OF 1

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