

MOSFET – N-Channel, POWER TRENCH®

80 V, 171 A, 3.9 mΩ

FDP039N08B-F102

Description

This N-Channel MOSFET is produced using onsemi's advanced POWER TRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

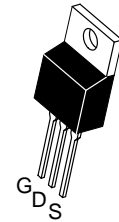
- $R_{DS(on)} = 3.16 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$
- Low FOM $R_{DS(on)} * Q_G$
- Low Reverse-Recovery Charge, $Q_{rr} = 87.9 \text{ nC}$
- Soft Reverse-Recovery Body Diode
- Enables High Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies

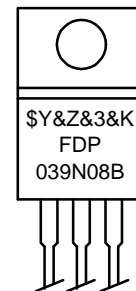
V_{DS}	$R_{DS(on)}$ TYP	I_D MAX
80 V	3.16 mΩ @ 10 V	171 A*

*Package limitation current is 120 A.

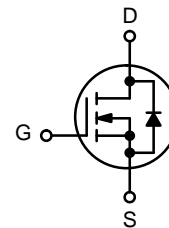


TO-220
CASE 221A

MARKING DIAGRAM



\$Y = Logo
&Z = Assembly Plant Code
&3 = 3-Digit Date Code Format
&K = 2-Digits Lot Run Traceability Code
FDP039N08B = Device Code



N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

FDP039N08B–F102

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	FDP039N08B–F102	Unit
V _{DSS}	Drain to Source Voltage	80	V
V _{GSS}	Gate to Source Voltage	±20	V
I _D	Drain Current	– Continuous (T _C = 25°C, Silicon Limited)	171*
		– Continuous (T _C = 100°C, Silicon Limited)	121*
		– Continuous (T _C = 25°C, Package Limited)	120
I _{DM}	Drain Current	– Pulsed (Note 1)	684
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	547	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P _D	Power Dissipation	(T _C = 25°C)	214
		– Derate Above 25°C	1.43
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to +175	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Package limitation current is 120 A.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 3 mH, I_{AS} = 19.1 A, starting T_J = 25°C.
3. I_{SD} ≤ 100 A, di/dt ≤ 200 A/ms, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP039N08B–F102	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.7	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	62.5	

FDP039N08B-F102

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	80	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.089	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 64 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 64 V, T _C = 150°C	–	–	500	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 100 A	–	3.16	3.9	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 100 A	–	180	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	–	7105	9450	pF
C _{oss}	Output Capacitance		–	1110	1475	pF
C _{rss}	Reverse Transfer Capacitance		–	30	–	pF
C _{oss(er)}	Energy Related Output Capacitance	V _{DS} = 40 V, V _{GS} = 0 V	–	1656	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 40 V, I _D = 100 A, V _{GS} = 10 V (Note 4)	–	102	133	nC
Q _{gs}	Gate to Source Gate Charge		–	39.9	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	22	–	nC
V _{plateau}	Gate Plateau Voltage		–	5.6	–	V
Q _{sync}	Total Gate Charge Sync.	V _{DS} = 0 V, I _D = 50 A	–	87.4	–	nC
Q _{oss}	Output Charge	V _{DS} = 40 V, V _{GS} = 0 V	–	99.2	–	nC

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 40 V, I _D = 100 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	–	36	82	ns
t _r	Turn-On Rise Time		–	49	108	ns
t _{d(off)}	Turn-Off Delay Time		–	71	152	ns
t _f	Turn-Off Fall Time		–	29	68	ns
ESR	Equivalent Series Resistance (G–S)	f = 1 MHz	–	2.2	–	Ω

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	171*	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	684	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 100 A	–	–	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 40 V, I _{SD} = 100 A, dI _F /dt = 100 A/μs	–	70.1	–	ns
Q _{rr}	Reverse Recovery Charge		–	87.9	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Package limitation current is 120 A.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

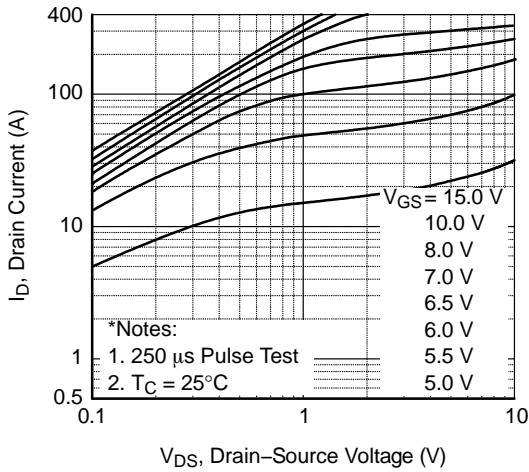


Figure 1. On-Region Characteristics

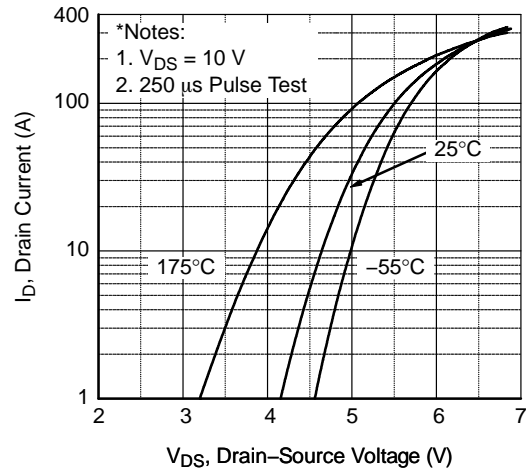


Figure 2. Transfer Characteristics

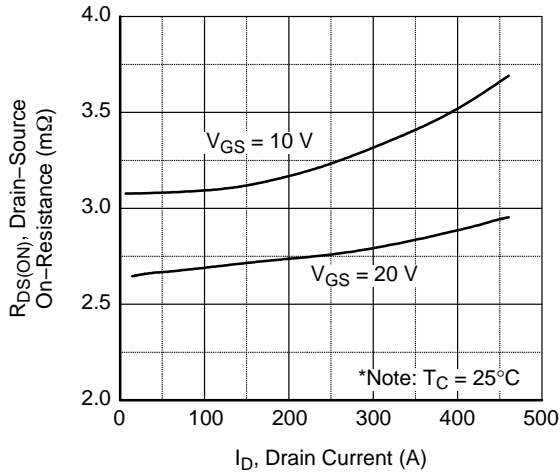


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

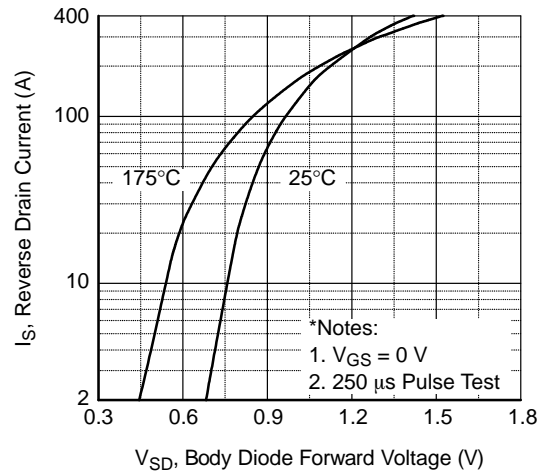


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

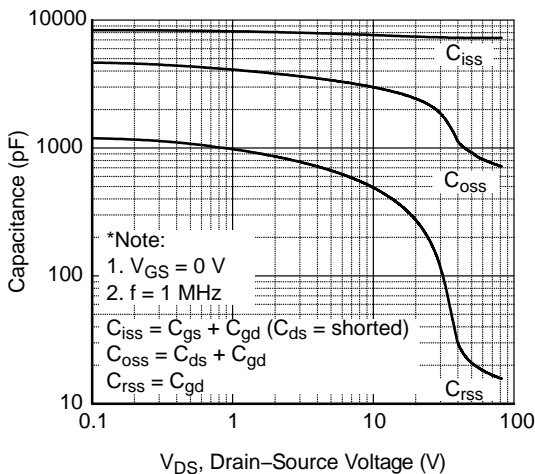


Figure 5. Capacitance Characteristics

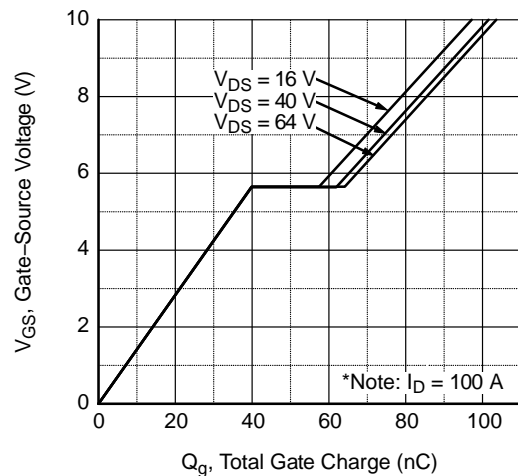


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

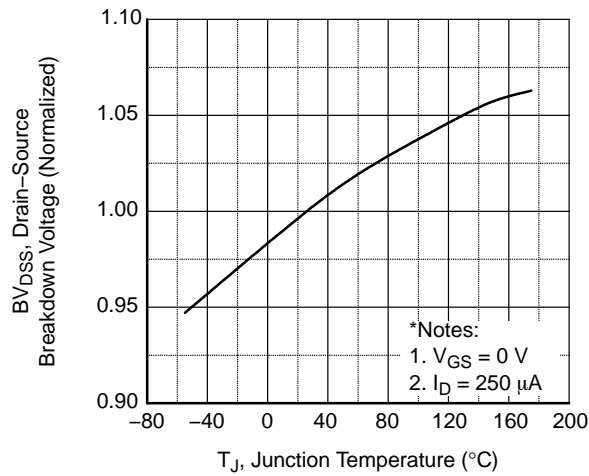


Figure 7. Breakdown Voltage Variation vs. Temperature

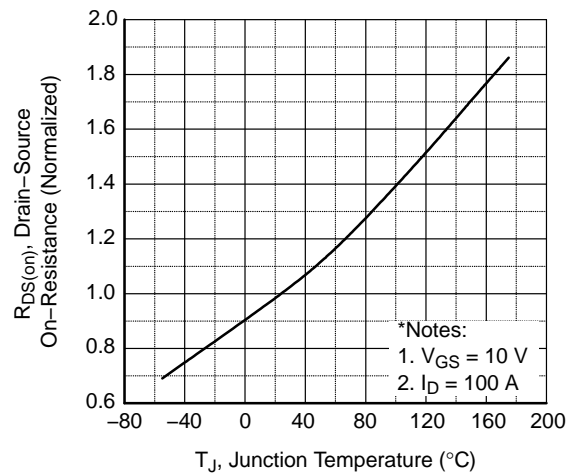


Figure 8. On-Resistance Variation vs. Temperature

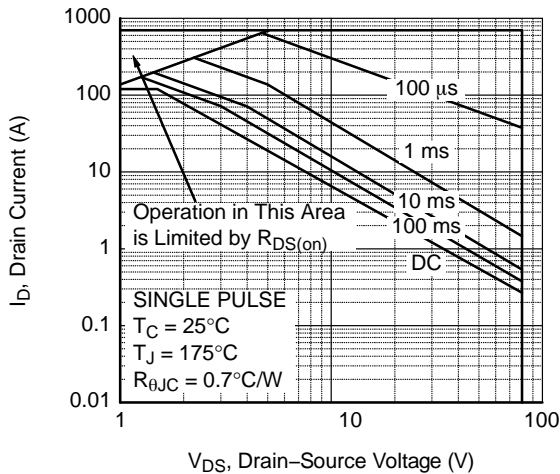


Figure 9. Maximum Safe Operating Area

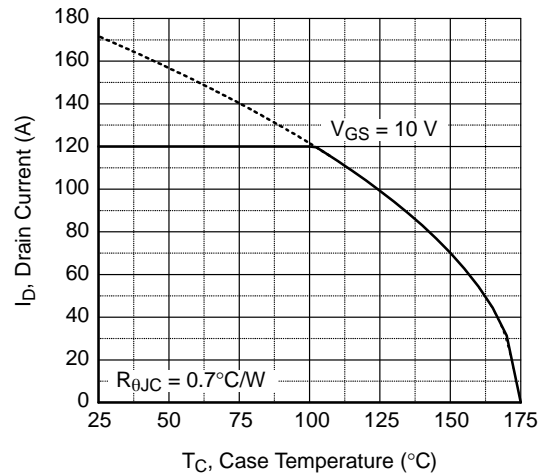


Figure 10. Maximum Drain Current vs. Case Temperature

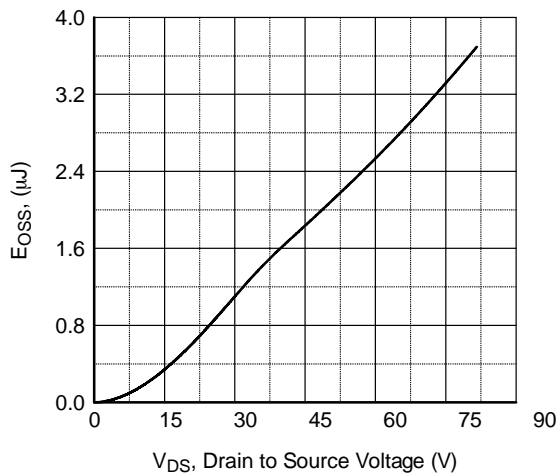


Figure 11. E_{oss} vs. Drain to Source Voltage

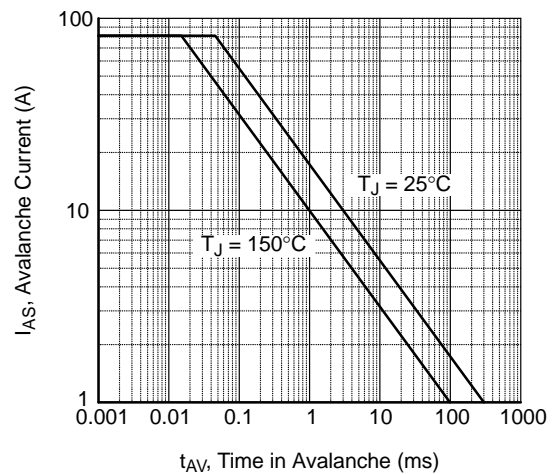


Figure 12. Unclamped Inductive Switching Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

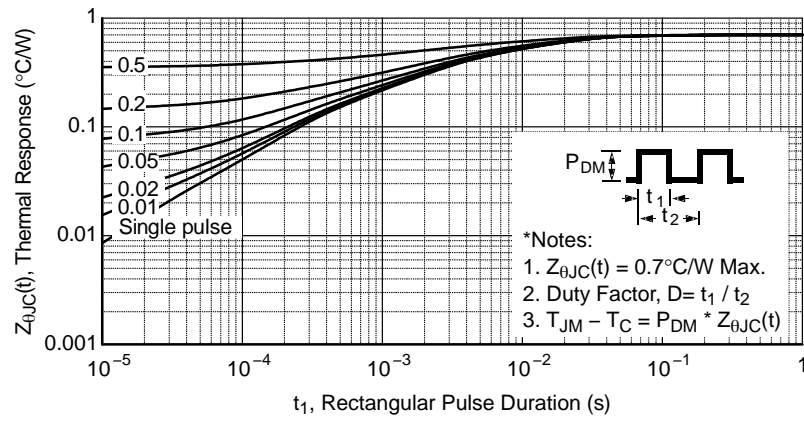


Figure 13. Transient Thermal Response Curve

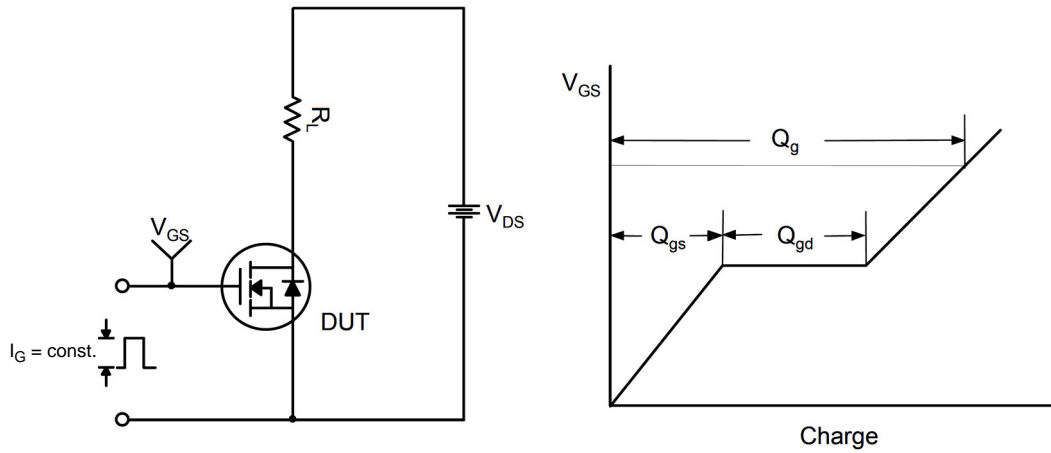


Figure 14. Gate Charge Test Circuit & Waveform

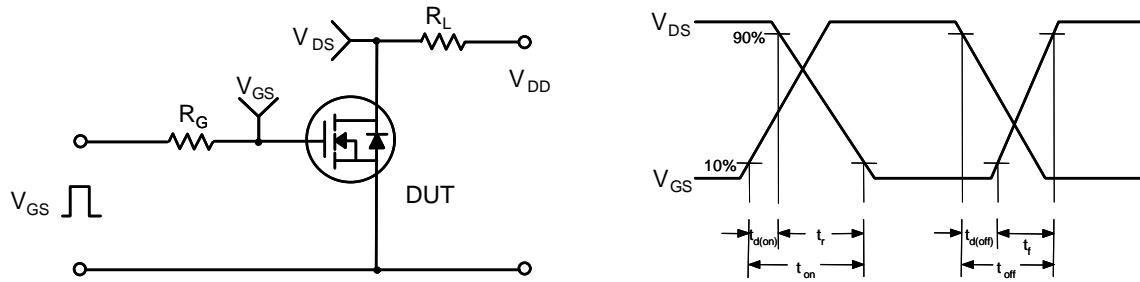


Figure 15. Resistive Switching Test Circuit & Waveforms

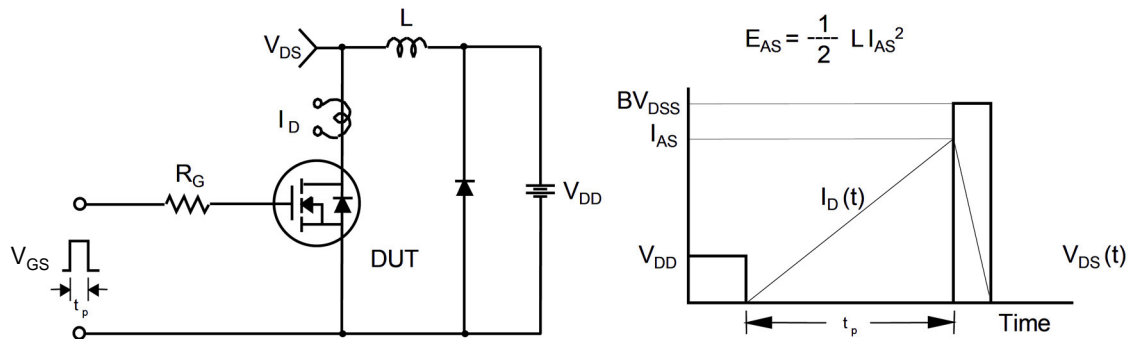


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

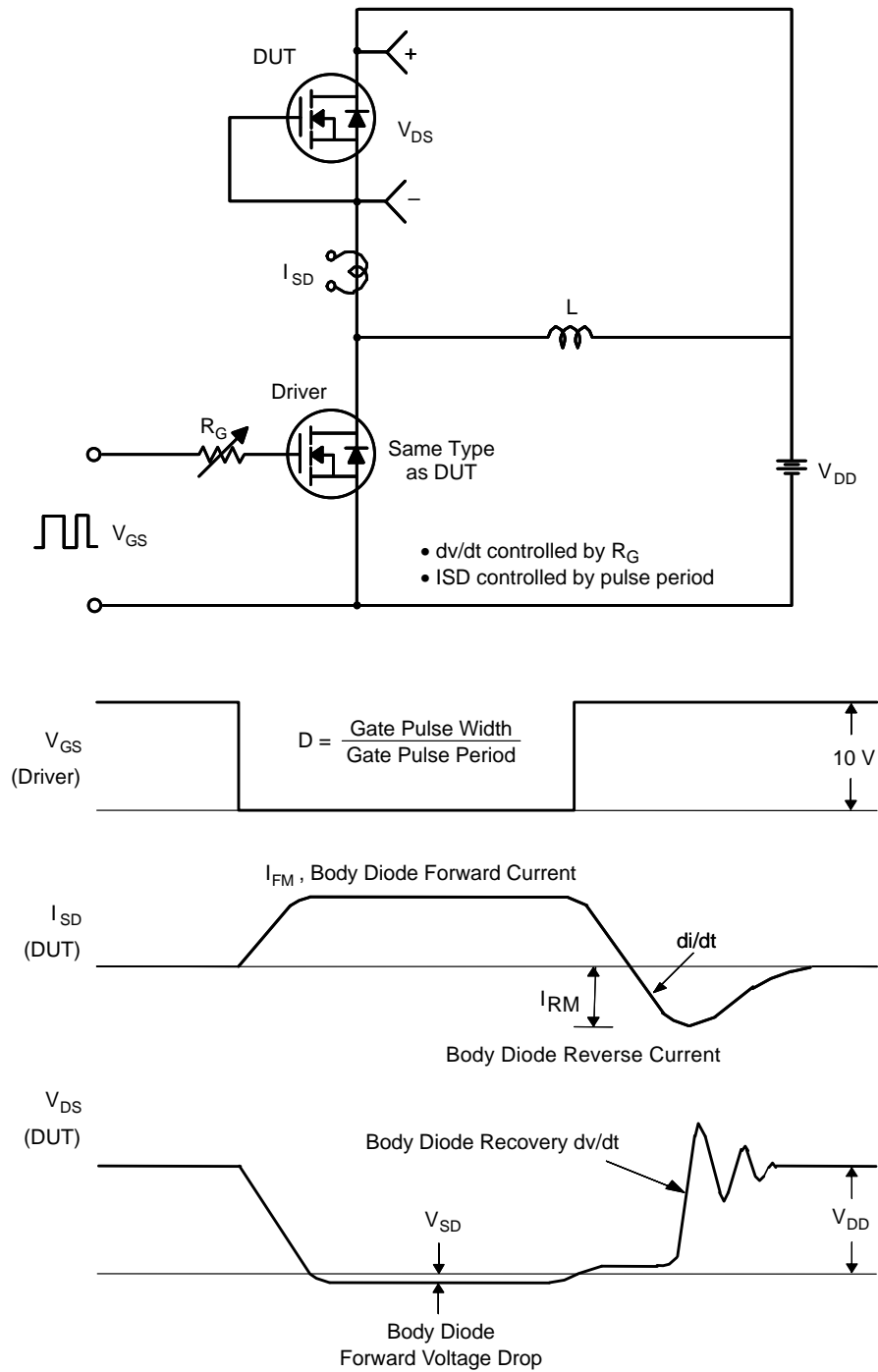


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

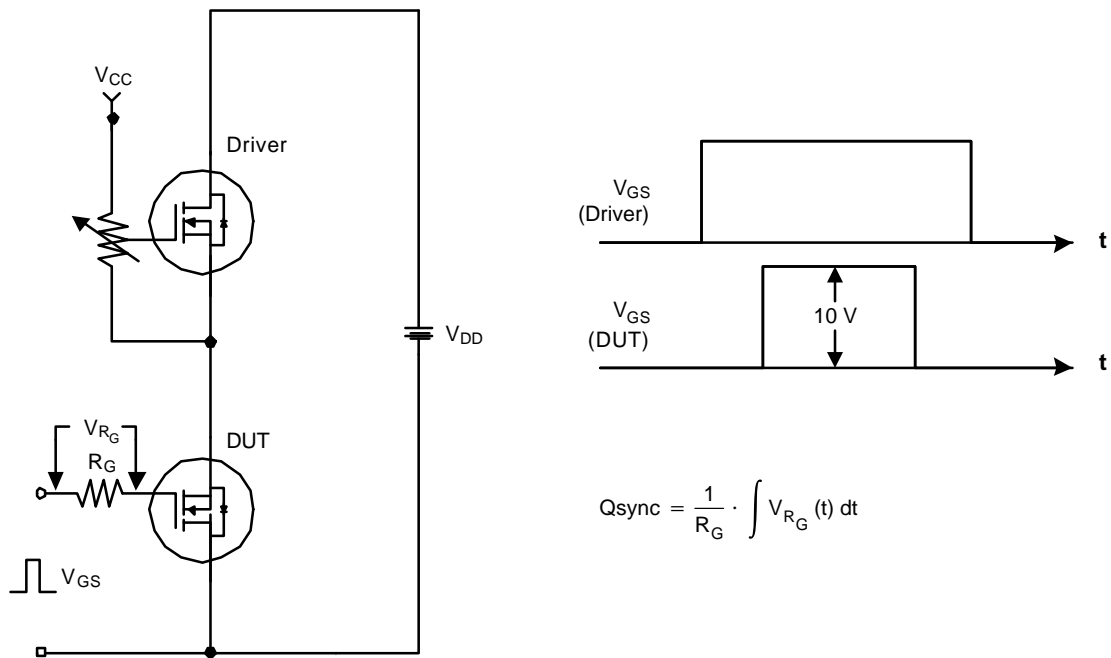
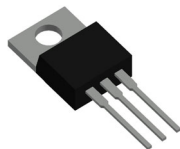


Figure 18. Total Gate Charge Q_{sync} . Test Circuit & Waveforms

ORDERING INFORMATION

Part Number	Device Marking	Package	Shipping
FDP039N08B-F102	FDP039N08B	TO-220	50 Units / Tube

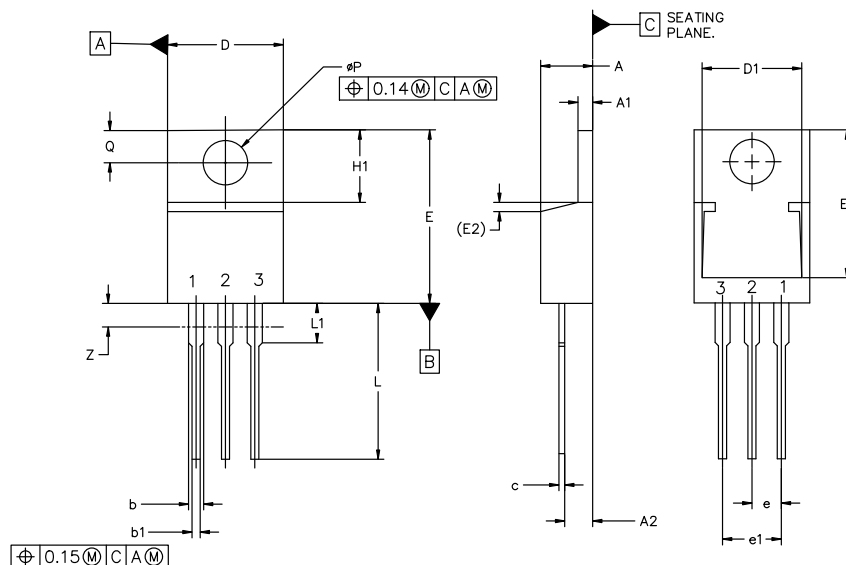


TO-220-3 10.10x15.12x4.45, 2.54P

CASE 221A

ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	---	---	3.48

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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