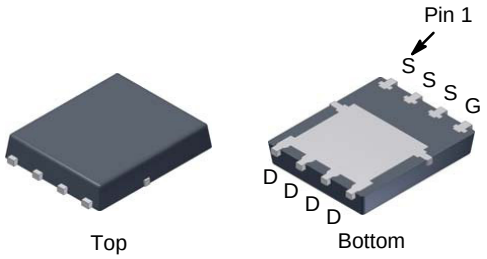
MOSFET – N-Channel, POWERTRENCH®

80 V, 100 A, 3.9 mΩ

FDMS039N08B

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
80 V	3.9 mΩ @ 10 V	100 A



PQFN8 5X6, 1.27P
(Power 56)
CASE 483AE

General Description

This N−Channel MOSFET is produced using **onsemi**'s advance POWERTRENCH process that has been tailored to minimize the on−state resistance while maintaining superior switching performance.

Features

- Max $R_{DS(on)}$ = 3.2 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 50 A
- Low FOM $R_{DS(on)}$ * Q_G
- Low Reverse Recovery Charge, Q_{rr} = 80 nC
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb−Free, Halide Free and is RoHS Compliant

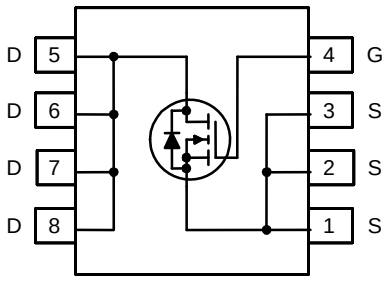
Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies

MARKING DIAGRAM

&Z = Assembly Plant Code
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Code
FDMS039N08B = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

MOSFET MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter	FDMS039N08B	Unit
V_{DSS}	Drain to Source Voltage	80	V
V_{GSS}	Gate to Source Voltage	±20	V
I_D	Drain Current − Continuous (T_C = 25°C) − Continuous (T_A = 25°C) (Note 1a)	 100 19.4	A
I_{DM}	Drain Current − Pulsed (Note 2)	 400	mJ
E_{AS}	Single Pulse Avalanche Energy (Note 3)	240	mJ
P_D	Power Dissipation (T_C = 25°C) (T_A = 25°C) (Note 1a)	 104 2.5	W
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

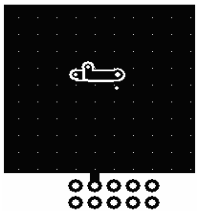
Symbol	Parameter	FDMS039N08B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

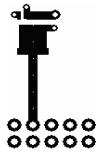
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.04	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 50 A	–	3.2	3.9	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 50 A	–	100	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V f = 1 MHz	–	5715	7600	pF
C_{oss}	Output Capacitance		–	881	1170	pF
C_{rss}	Reverse Transfer Capacitance		–	15	–	pF
C_{oss}(er)	Engry Releted Output Capacitance	V_{DS} = 40 V, V_{GS} = 0 V	–	1646	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 40 V, I_D = 50 A V_{GS} = 0 V to 10 V (Note 4)	–	77	100	nC
Q_{gs}	Gate to Source Gate Charge		–	34	–	nC
Q_{gs2}	Gate Charge Threshold to Plateau		–	13	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	16	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.2	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 40 V, I_D = 50 A V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	–	42	94	ns
t_r	Turn−On Rise Time		–	25	60	ns
$t_{d(off)}$	Turn−Off Delay Time		–	48	106	ns
t_f	Turn−Off Fall Time		–	17	44	ns
DRAIN−SOURCE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	100	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	400	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 50 A	–	–	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 50 A, V_{DD} = 40 V dI_F/dt = 100 A/μs	–	68	–	ns
Q_{rr}	Reverse Recovery Charge		–	80	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Repetitive rating: pulse−width limited by maximum junction temperature.
3. L = 0.3 mH, I_{AS} = 40 A, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

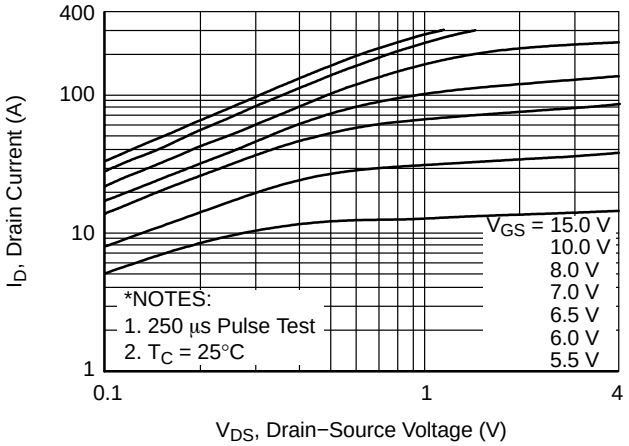


Figure 1. On−Region Characteristics

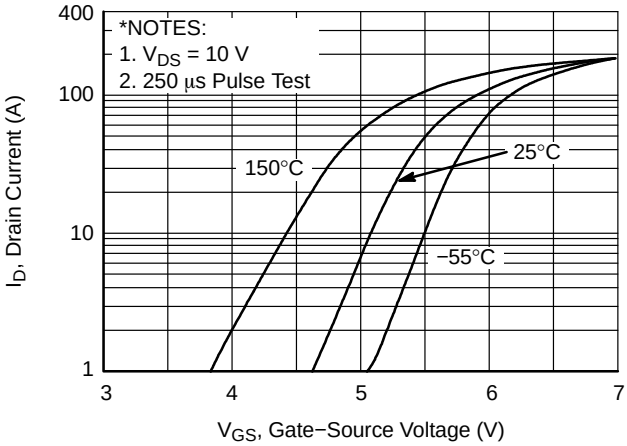


Figure 2. Transfer Characteristics

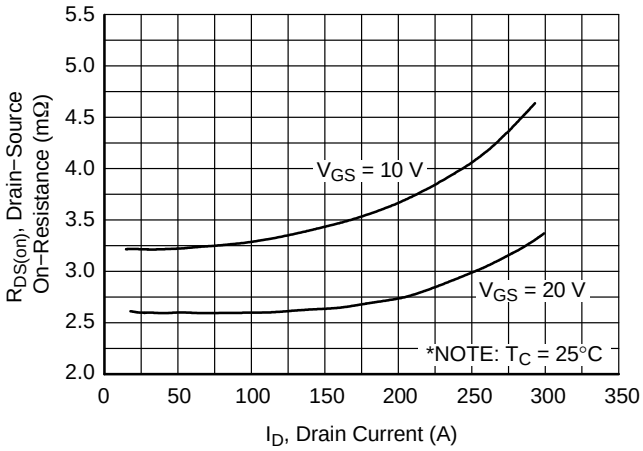


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

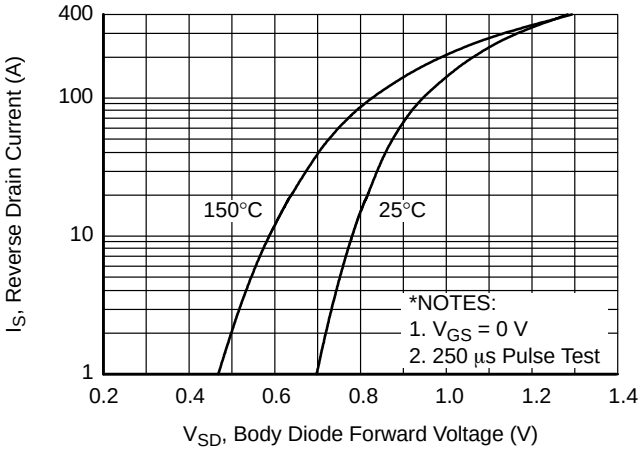


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

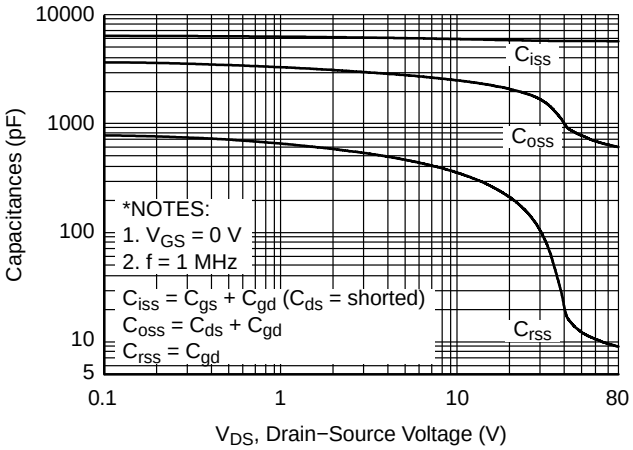


Figure 5. Capacitance Characteristics

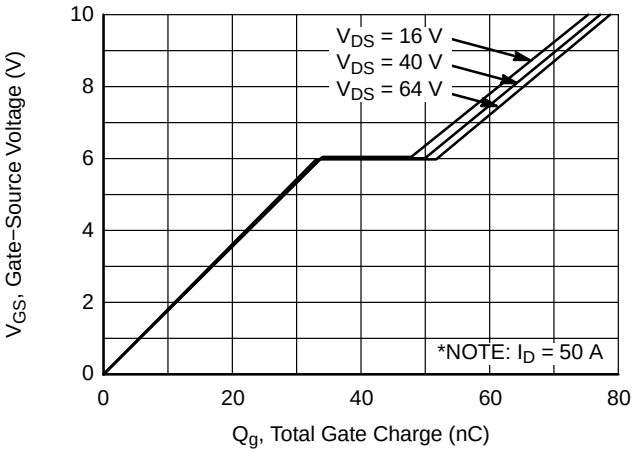


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

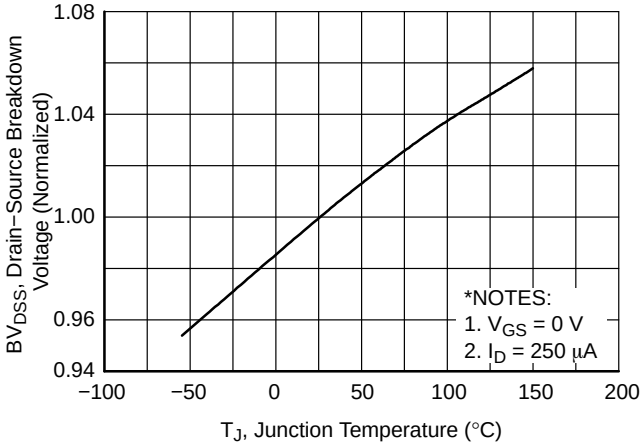


Figure 7. Breakdown Voltage Variation vs. Temperature

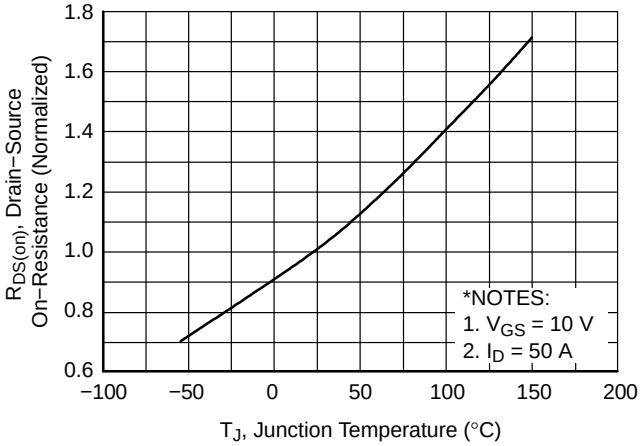


Figure 8. On−Resistance Variation vs. Temperature

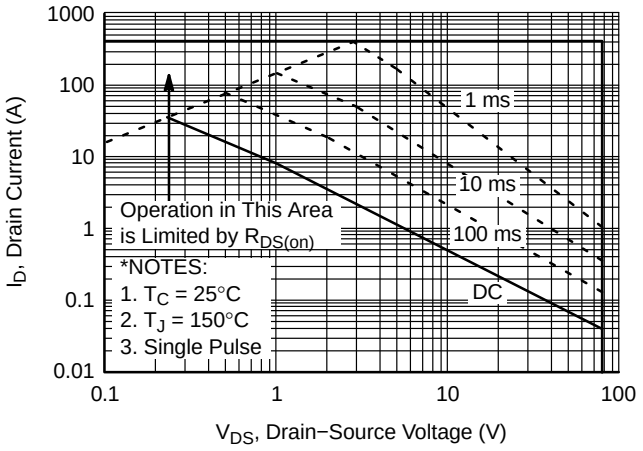


Figure 9. Maximum Safe Operating Area

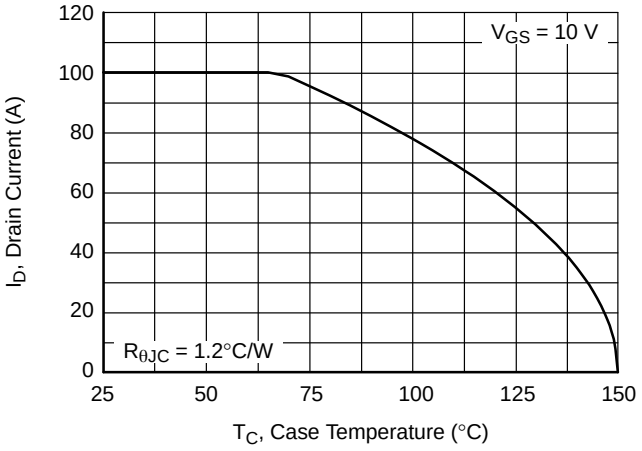


Figure 10. Maximum Drain Current vs. Case Temperature

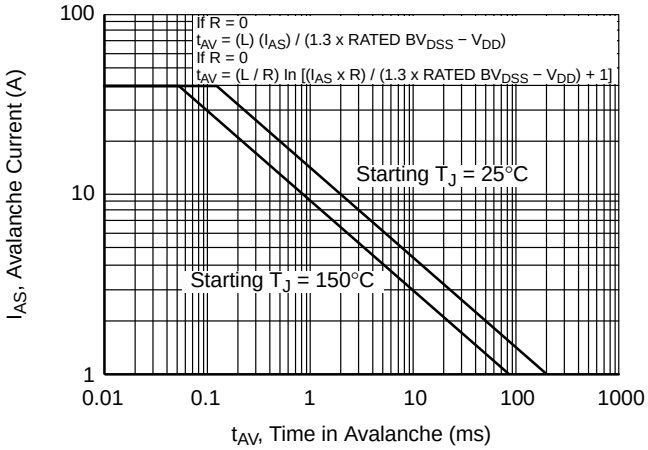


Figure 11. Unclamped Inductive Switching Capability

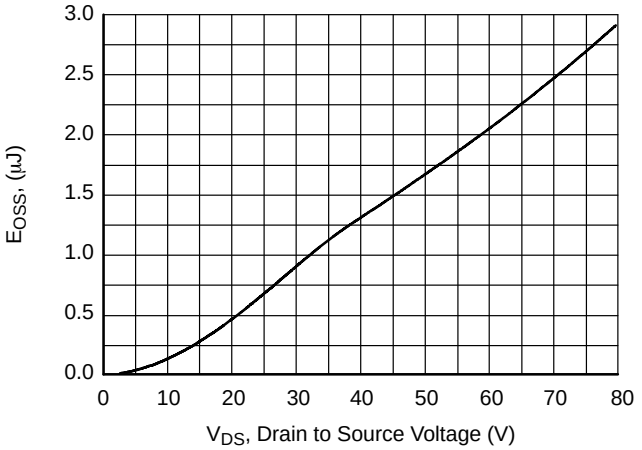


Figure 12. Eoss vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

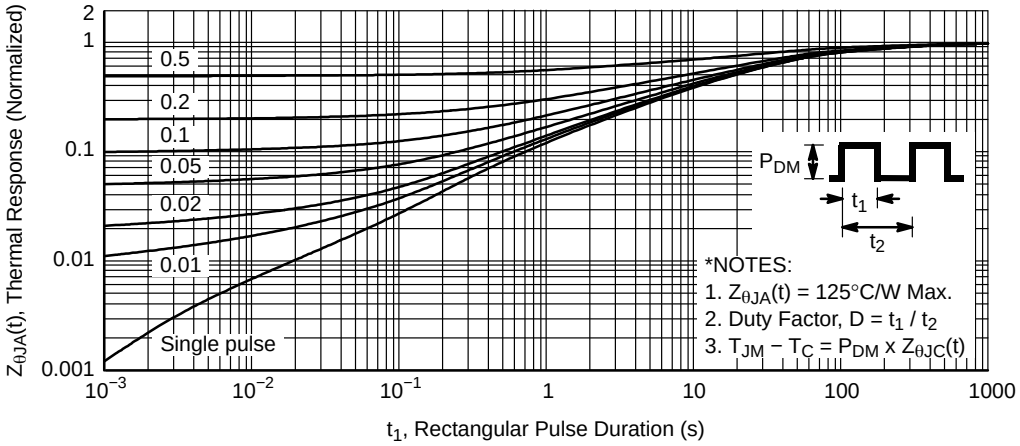


Figure 13. Transient Thermal Response Curve

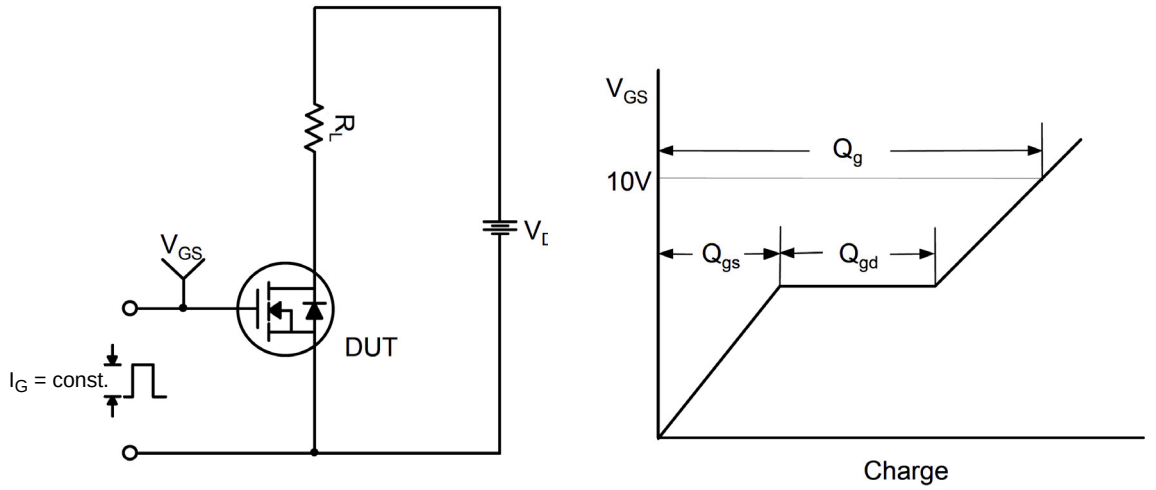


Figure 14. Gate Charge Test Circuit & Waveform

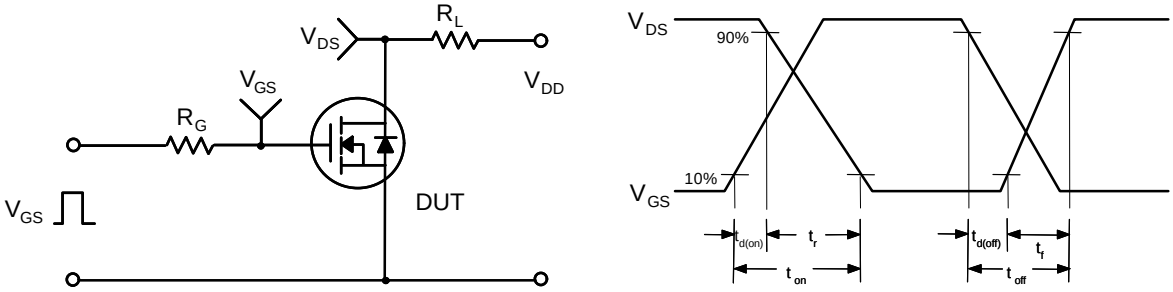


Figure 15. Resistive Switching Test Circuit & Waveforms

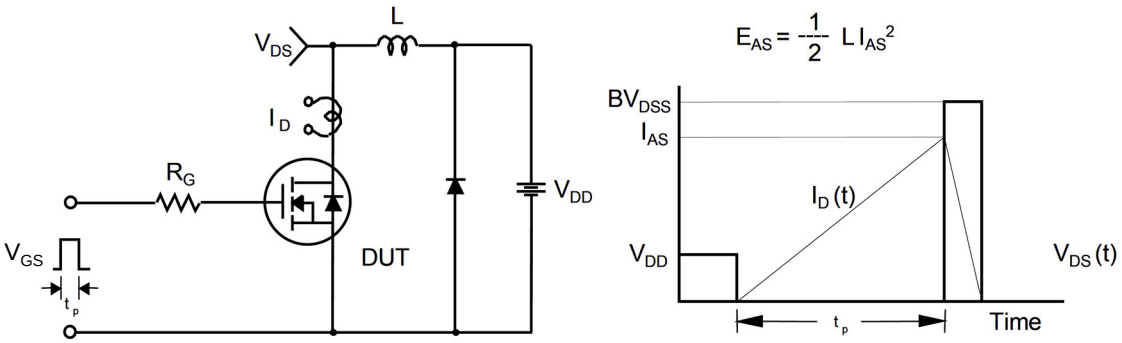


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

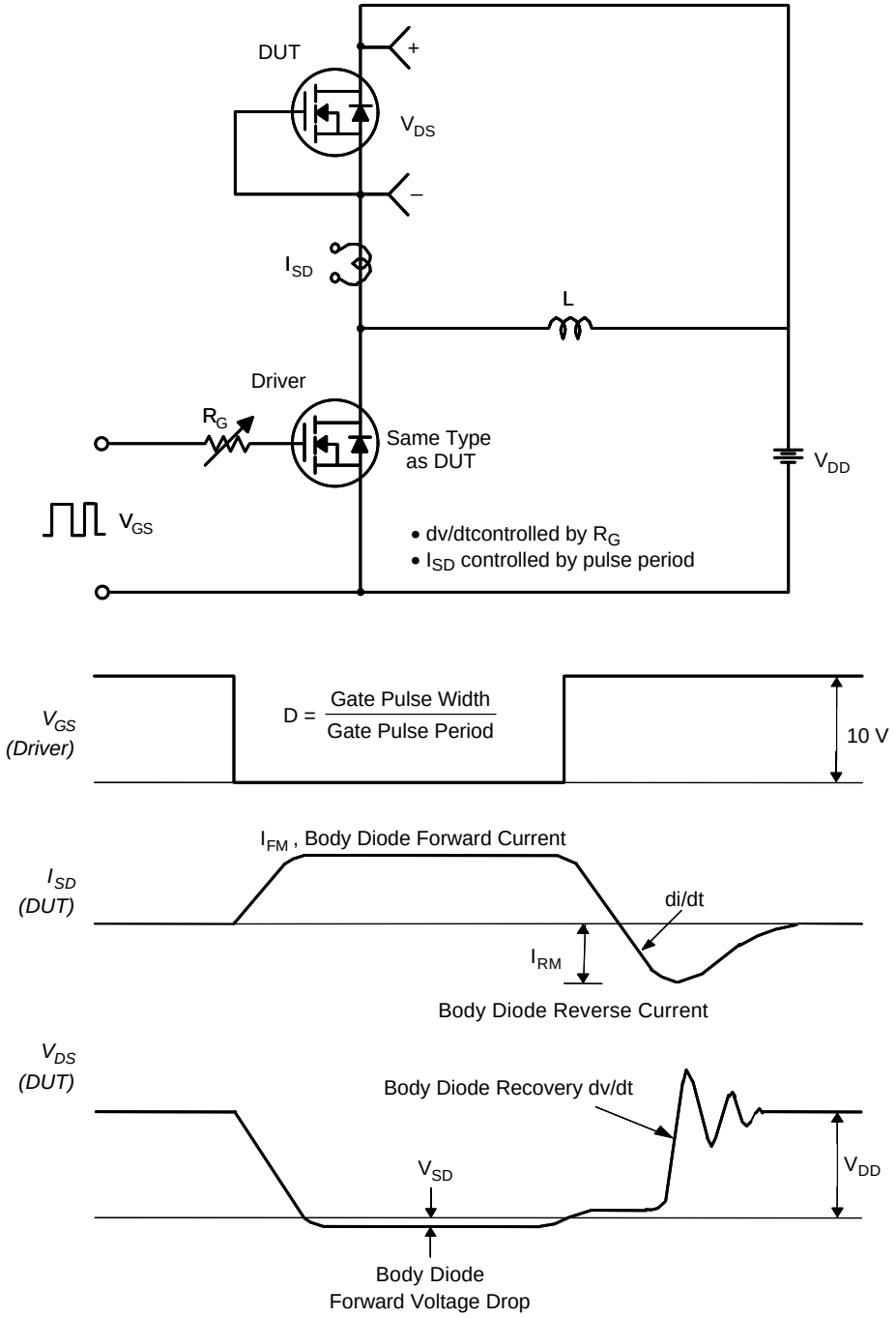


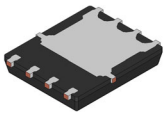
Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMS039N08B	FDMS039N08B	PQFN8 5X6, 1.27P (Power 56) (Pb−Free, Halide Free)	13”	12 mm	3000 / Tape & Reel

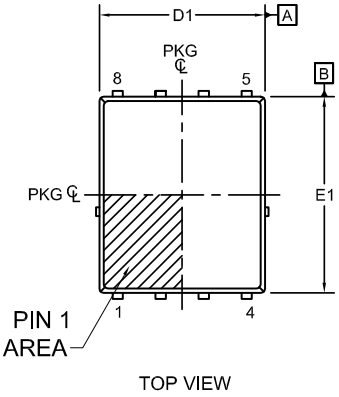
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

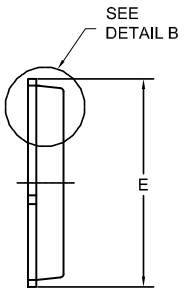


PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

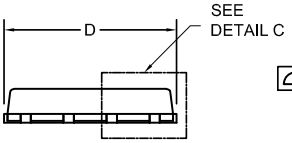
DATE 21 JAN 2022



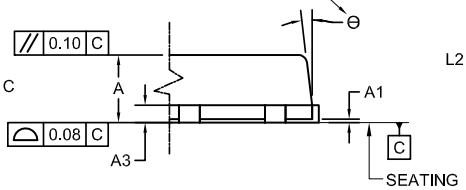
TOP VIEW



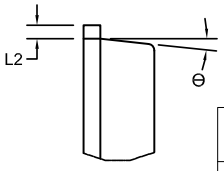
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



SIDE VIEW



DETAIL C
SCALE: 2:1

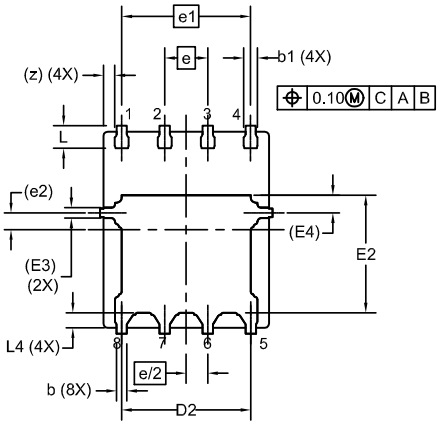


DETAIL B
SCALE: 2:1

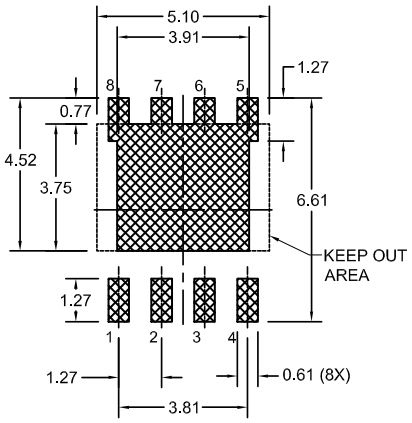
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



BOTTOM VIEW



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON13655G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**PQFN8 5X6, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales