MOSFET - N-Channel Shielded Gate POWERTRENCH®

80 V, 84 A, 6.7 mΩ

FDMS007N08LC

Description

This N−Channel MV MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimize on−state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

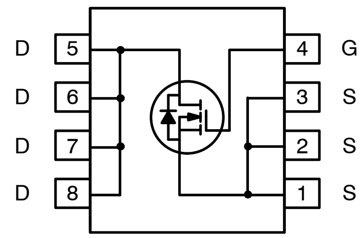
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 6.7 mΩ at V_{GS} = 10 V, I_D = 21 A
- Max $r_{DS(on)}$ = 9.9 mΩ at V_{GS} = 4.5 V, I_D = 17 A
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

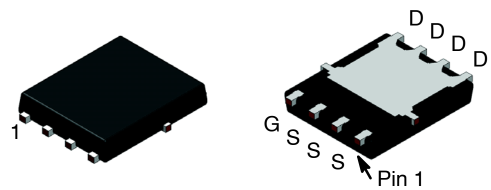
Typical Applications

- Primary DC−DC MOSFET
- Synchronous Rectifier in DC−DC and AC−DC
- Motor Drive
- Solar

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
80 V	6.7 mΩ @ 10 V	84 A

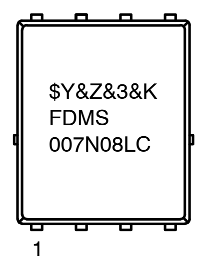
N−Channel





**PQFN8 5×6, 1.27P
(Power 56)
CASE 483AE**

MARKING DIAGRAM



$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMS007N08LC	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMS007N08LC	PQFN−8 (Pb−Free)	000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter			Ratings	Unit
V_{DS}	Drain to Source Voltage			80	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current	– Continuous	T_C = 25°C (Note 5)	84	A
		– Continuous	T_C = 100°C (Note 5)	53	
		– Continuous	T_A = 25°C (Note 1a)	14	
		– Pulsed (Note 4)		345	
E_{AS}	Single Pulse Avalanche Energy (Note 3)			181.5	mJ
P_D	Power Dissipation		T_C = 25°C	92.6	W
	Power Dissipation		T_A = 25°C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	32	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 120 μA	1.0	1.4	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 120 μA, referenced to 25°C	–	−5.6	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 21 A	–	4.9	6.7	mΩ
		V_{GS} = 4.5 V, I_D = 17 A	–	6.7	9.9	
		V_{GS} = 10 V, I_D = 21 A, T_J = 125°C	–	8.5	11.6	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 21 A	–	84	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	2227	3100	pF
C_{oss}	Output Capacitance		–	520	760	pF
C_{rss}	Reverse Transfer Capacitance		–	27	40	pF
R_G	Gate Resistance		0.1	0.4	0.8	Ω

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn−on Delay Time	V_{DD} = 40 V, I_D = 21 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	10	21	ns
t_r	Rise Time		–	3	10	
$t_{d(off)}$	Turn−off Delay Time		–	38	61	
t_f	Fall Time		–	8	16	
Q_g	Total Gate Charge	V_{GS} = 0V to 10 V, V_{DD} = 40 V, I_D = 21 A	–	33	46	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 4.5 V, V_{DD} = 40 V, I_D = 21 A	–	16	22	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40 V, I_D = 21 A	–	5	–	nC
Q_{gd}	Gate to Drain "Miller" Charge	V_{DD} = 40 V, I_D = 21 A	–	4	–	nC
Q_{oss}	Output Charge	V_{DD} = 40 V, V_{GS} = 0 V	–	30	–	nC
Q_{sync}	Total Gate Charge Sync	V_{DS} = 0 V, I_D = 21 A	–	35	–	nC

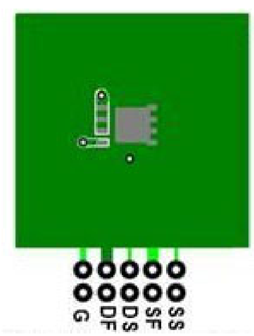
DRAIN−SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)	–	0.7	1.2	V
		V_{GS} = 0 V, I_S = 21 A (Note 2)	–	0.8	1.3	V
t_{rr}	Reverse Recovery Time	I_F = 10 A, di/dt = 300 A/μs	–	18	32	ns
Q_{rr}	Reverse Recovery Charge		–	24	28	nC
t_{rr}	Reverse Recovery Time	I_F = 10 A, di/dt = 1000 A/μs	–	13	23	ns
Q_{rr}	Reverse Recovery Charge		–	58	92	nC

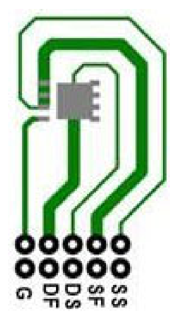
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 181 mJ is based on starting T_J = 25°C; L = 3 mH, I_{AS} = 11 A, V_{DD} = 80 V, V_{GS} = 10 V. 100% tested at L = 0.1 mH, I_{AS} = 35 A.
4. Pulsed I_D please refer to Fig. 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

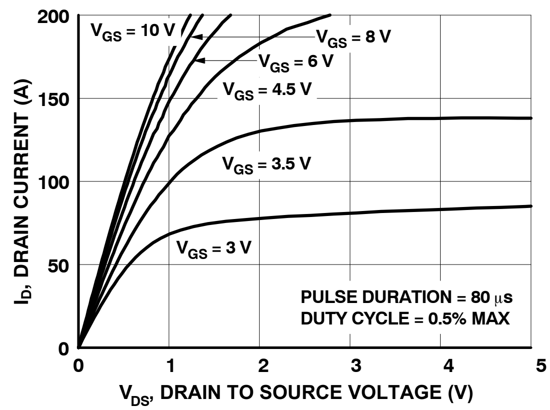


Figure 1. On Region Characteristics

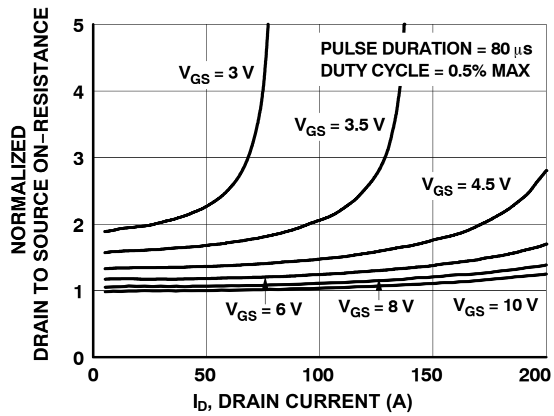


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

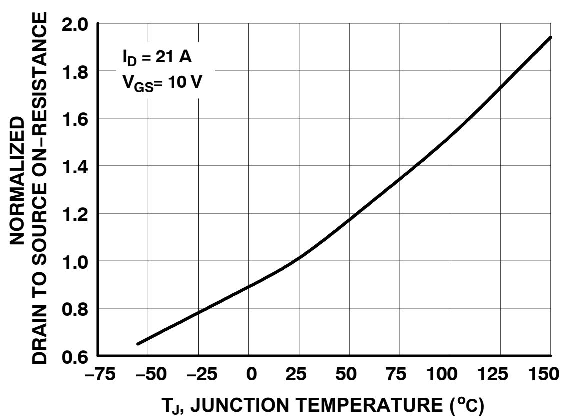


Figure 3. Normalized On Resistance vs. Junction Temperature

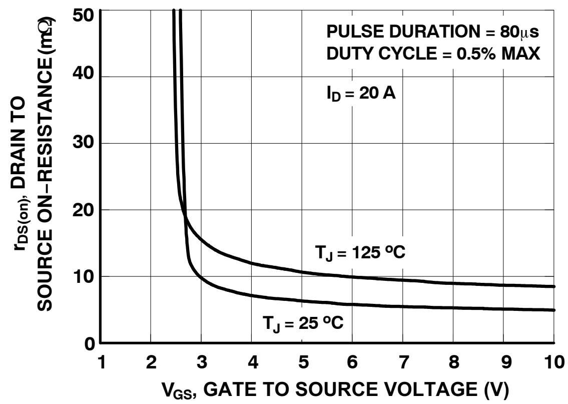


Figure 4. On-Resistance vs. Gate to Source Voltage

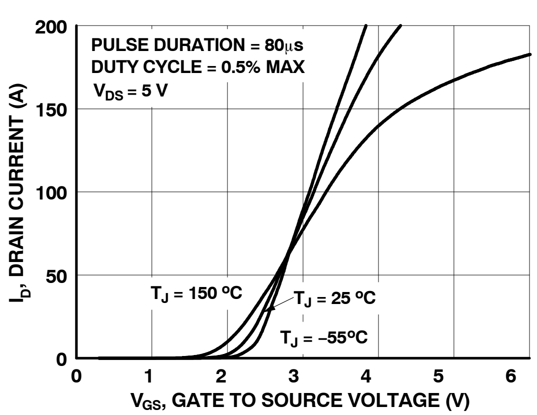


Figure 5. Transfer Characteristics

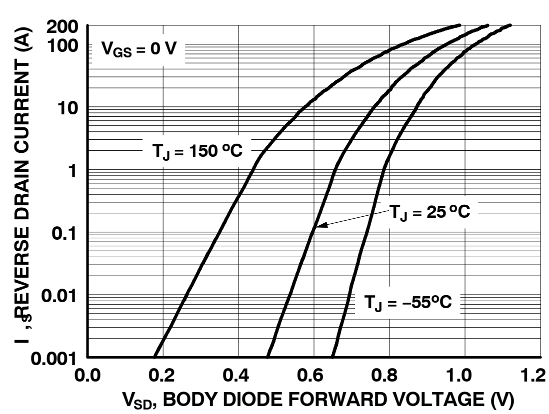


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

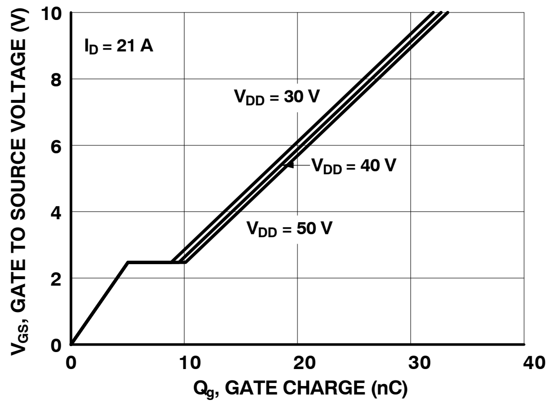


Figure 7. Gate Charge Characteristics

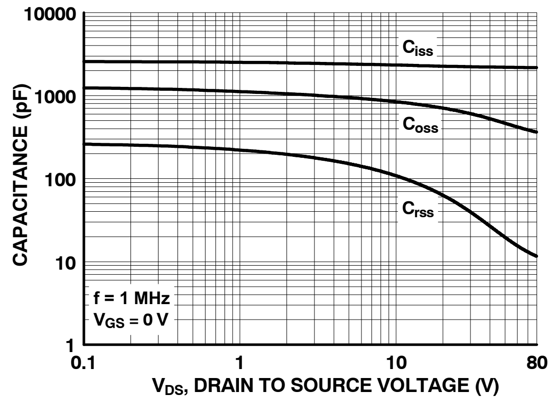


Figure 8. Capacitance vs. Drain to Source Voltage

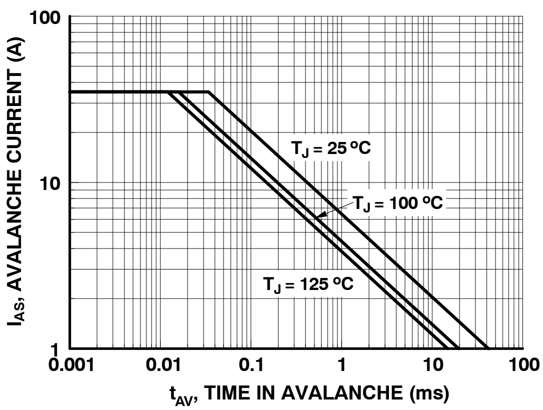


Figure 9. Unclamped Inductive Switching Capability

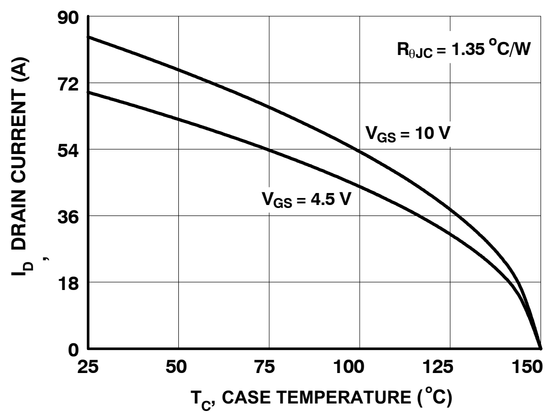


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

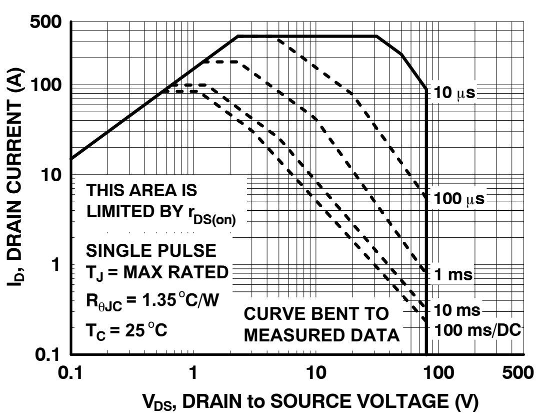


Figure 11. Forward Bias Safe Operating Area

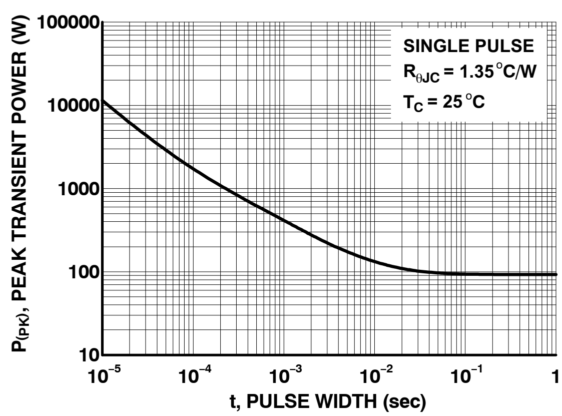


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

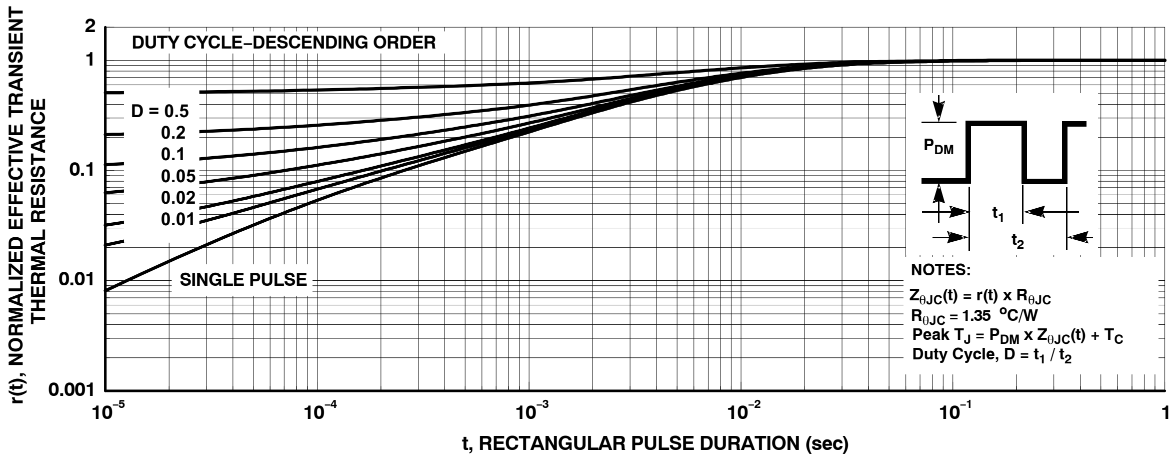


Figure 13. Junction−to−Case Transient Thermal Response Curve

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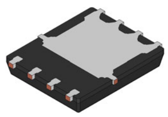

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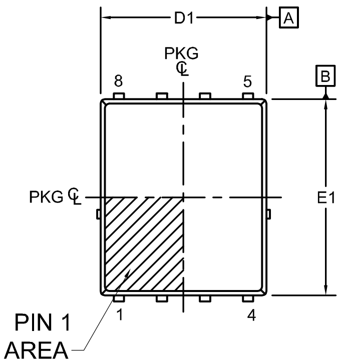
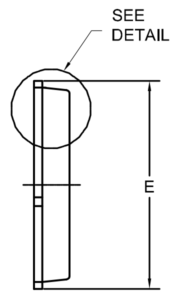
CASE 483AE
ISSUE C

DATE 21 JAN 2022

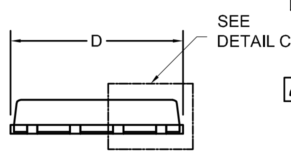


TOP VIEW

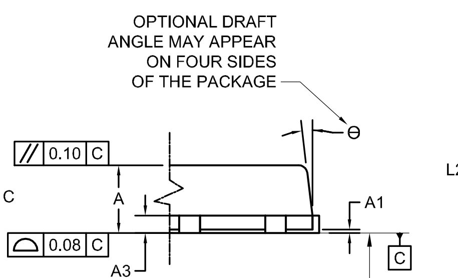


NOTES:

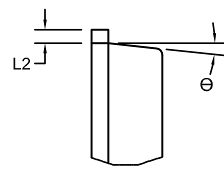
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



SIDE VIEW

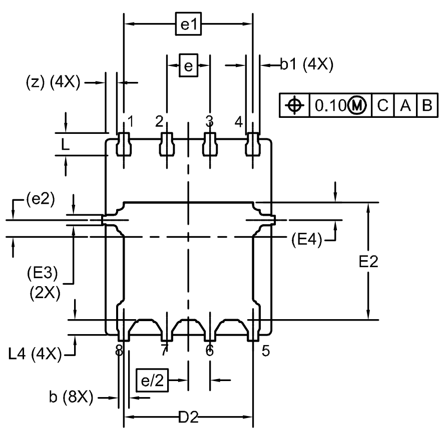


DETAIL C
SCALE: 2:1

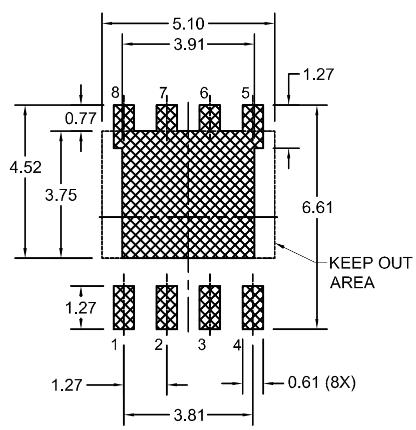


DETAIL B
SCALE: 2:1

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**PQFN8 5X6, 1.27P**	**PAGE 1 OF 1**

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