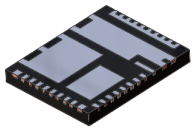
High Performance 60 V Smart Power Stage Module

FDMF4061



PQFN36 6X7.5, 0.5P
CASE 483BB

General Description

The FDMF4061 is a compact 60 V Smart Power Stage (SPS) module that is a fully optimized for use in high current switching applications. The FDMF4061 module integrates a driver IC plus two N−channel Power MOSFETs into a thermally enhanced, 6.0 mm x 7.5 mm PQFN package. The PQFN packaging provides very low package inductance and resistance improving the current handling capability and performance of the part. With an integrated approach, the complete switching power stage is optimized with regards to driver and MOSFET dynamic performance, system parasitic inductance, and Power MOSFET $R_{DS(ON)}$. The FDMF4061 uses **onsemi**'s high performance POWERTRENCH® MOSFET technology, which reduces high voltage and current stresses in switching applications. The driver IC features a low delay times and matched PWM input propagation delays, which further enhance the performance of the part.

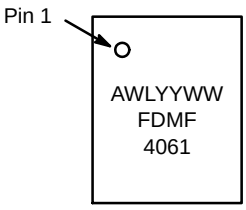
Features

- Compact Size − 6.0 mm x 7.5 mm PQFN
- High Current Handling: 25 A
- Next Generation 60 V Power MOSFETs:
  - Typ. $R_{DS(ON)}$ = 2.4 (HS) / 2.4 (LS) mΩ at V_{GS} = 10 V, I_D = 25 A
- Wide Driver Power Supply Voltage Range: 10 V to 20 V
- Internal Pull−down Resistors for PWM Inputs (HI, LI)
- Short PWM Propagation Delays
- Under−voltage Lockout (UVLO)
- Fully Optimized System Efficiency
- High Performance Low Profile Package
- Integrated 60 V Half−Bridge Gate Driver
- **onsemi** 60 V POWERTRENCH MOSFETs for Clean Switching Waveforms and Reduced Ringing
- Low Inductance and Low Resistance Packaging for Minimal Operating Power Losses
- Reduced EMI due to Low Side Flip−chip MOSFET
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

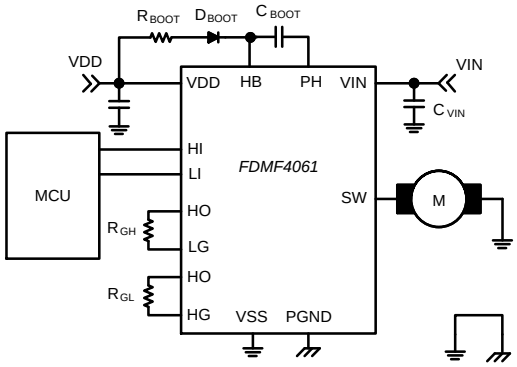
- Motor Drives (Power Tools & Drowns etc.)
- Telecom Half / Full − Bridge DC−DC Converters
- Buck−Boost Converters
- High−current DC−DC Point of Load (POL) Converters

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
FDMF4061 = Device Code

APPLICATION DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 26 of this data sheet.

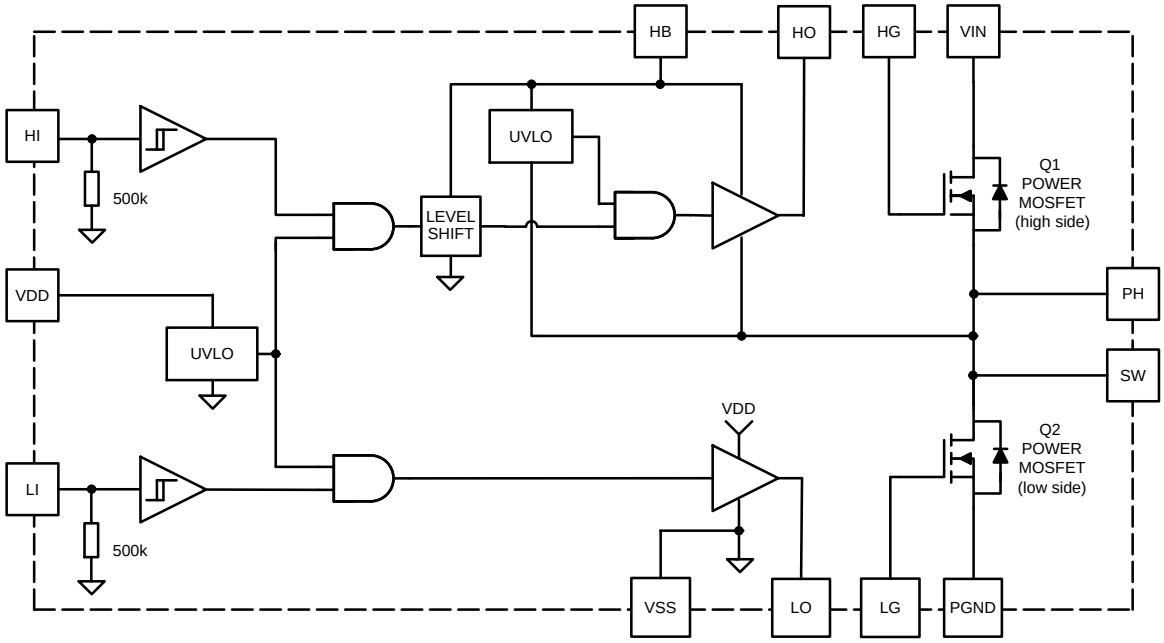


Figure 1. Functional Block Diagram

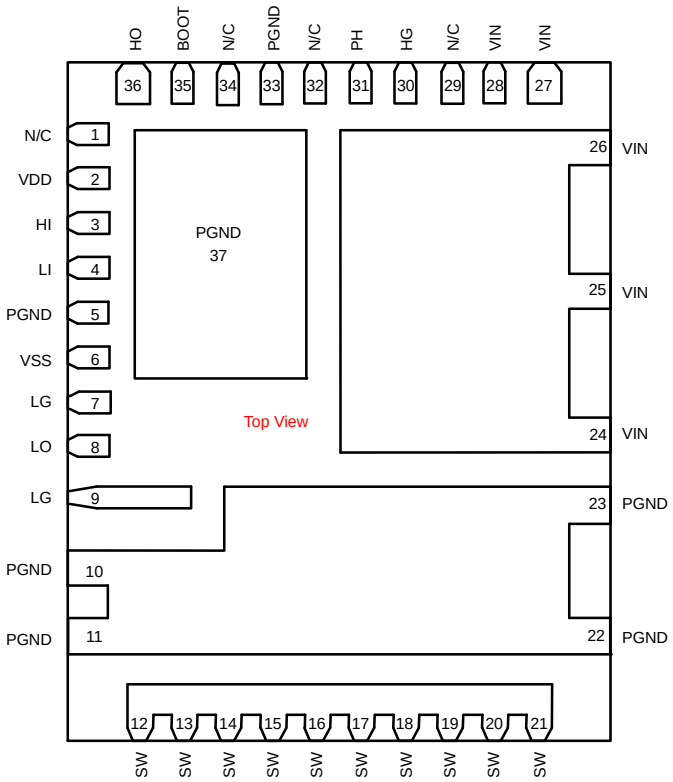


Figure 2. Pin Configuration

Table 1. PIN DEFINITIONS

Pin	Symbol	Function
1, 29, 32, 34	N/C	No connect
2	VDD	Power supply input for low−side gate drive and bootstrap diode. Bypass this pin to VSS with a low impedance capacitor.
3	HI	High−side PWM input.
4	LI	Low−side PWM input.
5, 10,11, 22, 23, 33, 37	PGND	Power return for the power stage. Package header, pin 37 and PGND are internally fused (shorted).
6	VSS	Analog ground for driver IC analog circuits.
7,9	LG	Low−side MOSFET gate.
8	LO	Low−side gate drive output.
12 − 21	SW	Switching node junction between high−side and Low−side MOSFETs.
24 − 28	VIN	Power input for the power stage. Bypass this pin to PGND with low impedance capacitor.
30	HG	High−side MOSFET gate.
31	PH	High−side source connection (SW node) for the bootstrap capacitor.
35	HB	Bootstrap supply for high−side driver. Bypass this pin to PH with low impedance capacitor.
36	HO	High−side gate drive output.

TYPICAL APPLICATION DIAGRAM

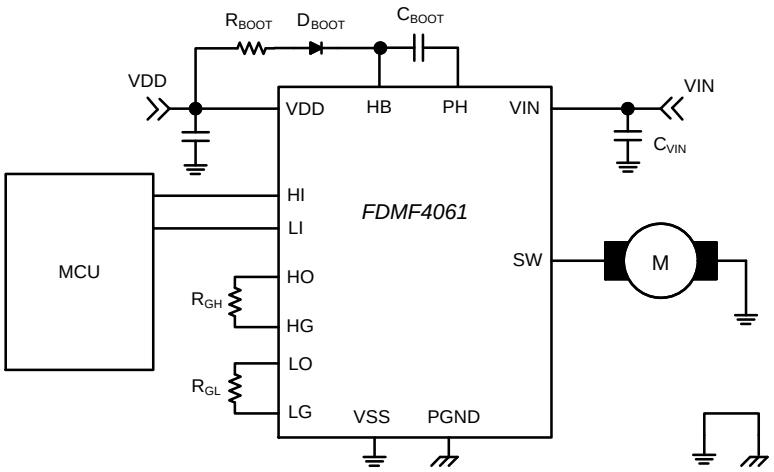


Figure 3. Half−Bridge DC Motor

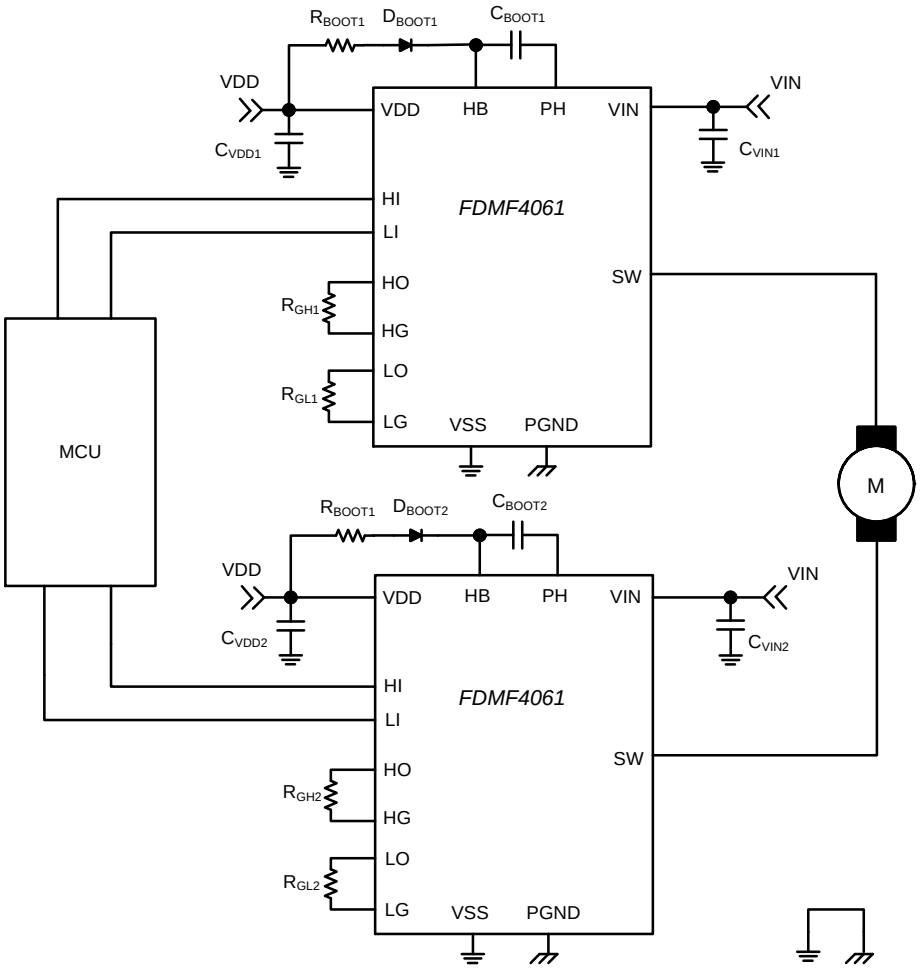


Figure 4. Full−Bridge DC Motor

TYPICAL APPLICATION DIAGRAM (Continued)

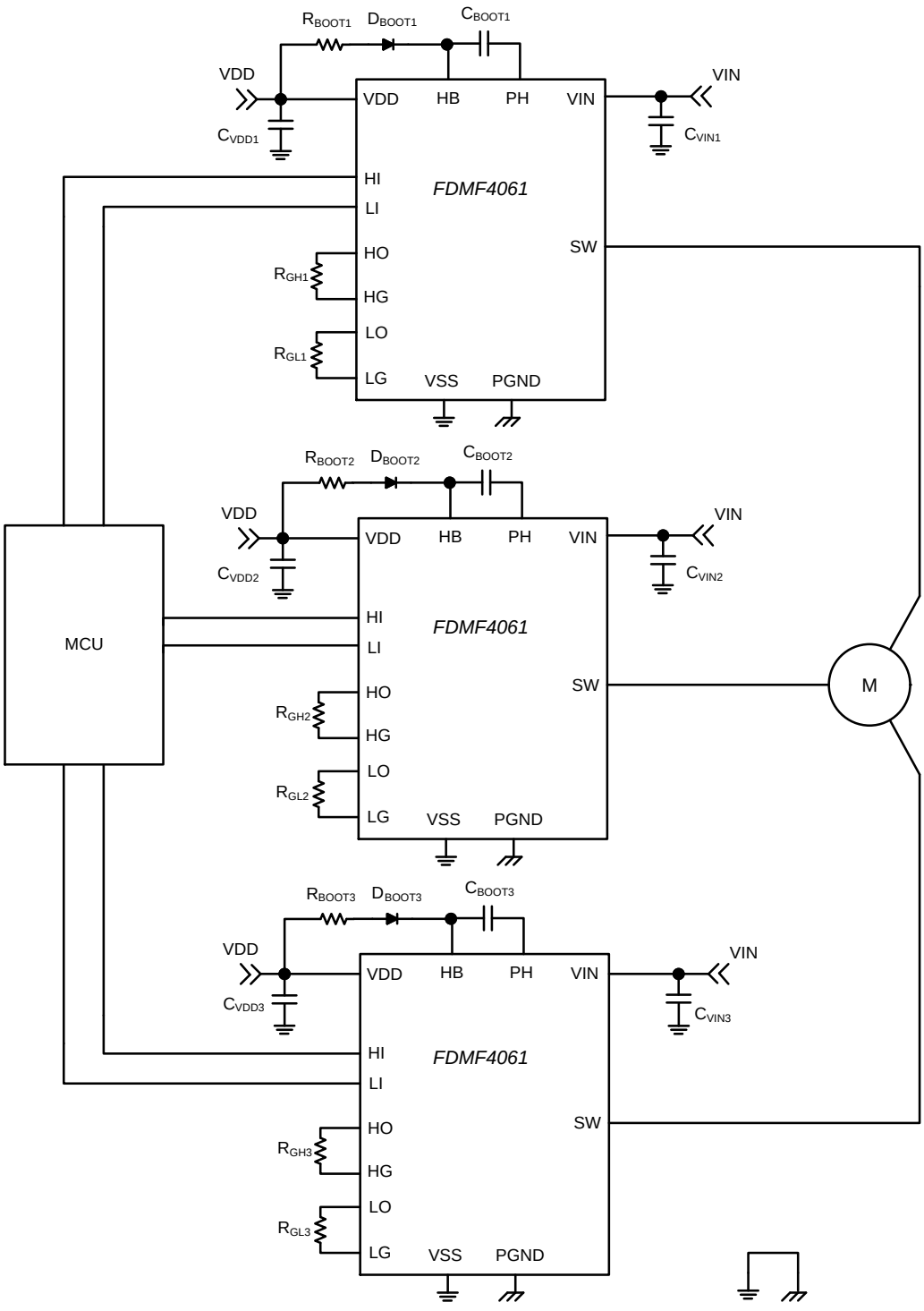


Figure 5. 3−Phase DC Motor

TYPICAL APPLICATION DIAGRAM (Continued)

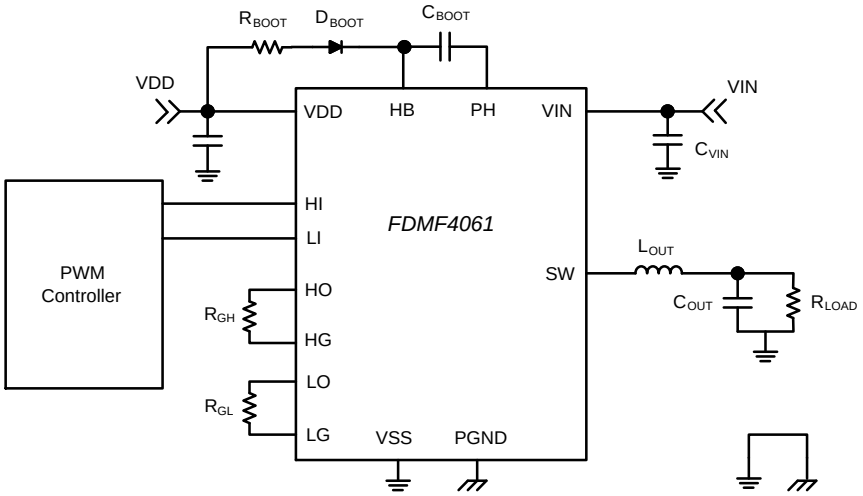


Figure 6. Buck Converter

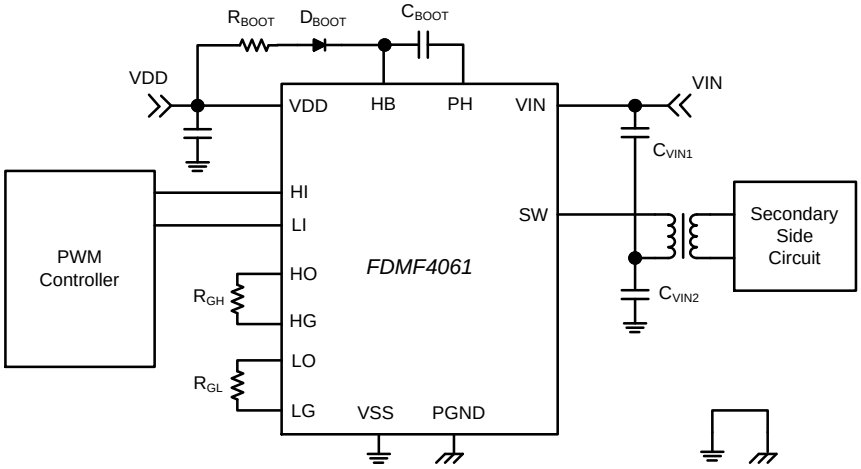


Figure 7. Half−Bridge Converter

TYPICAL APPLICATION DIAGRAM (Continued)

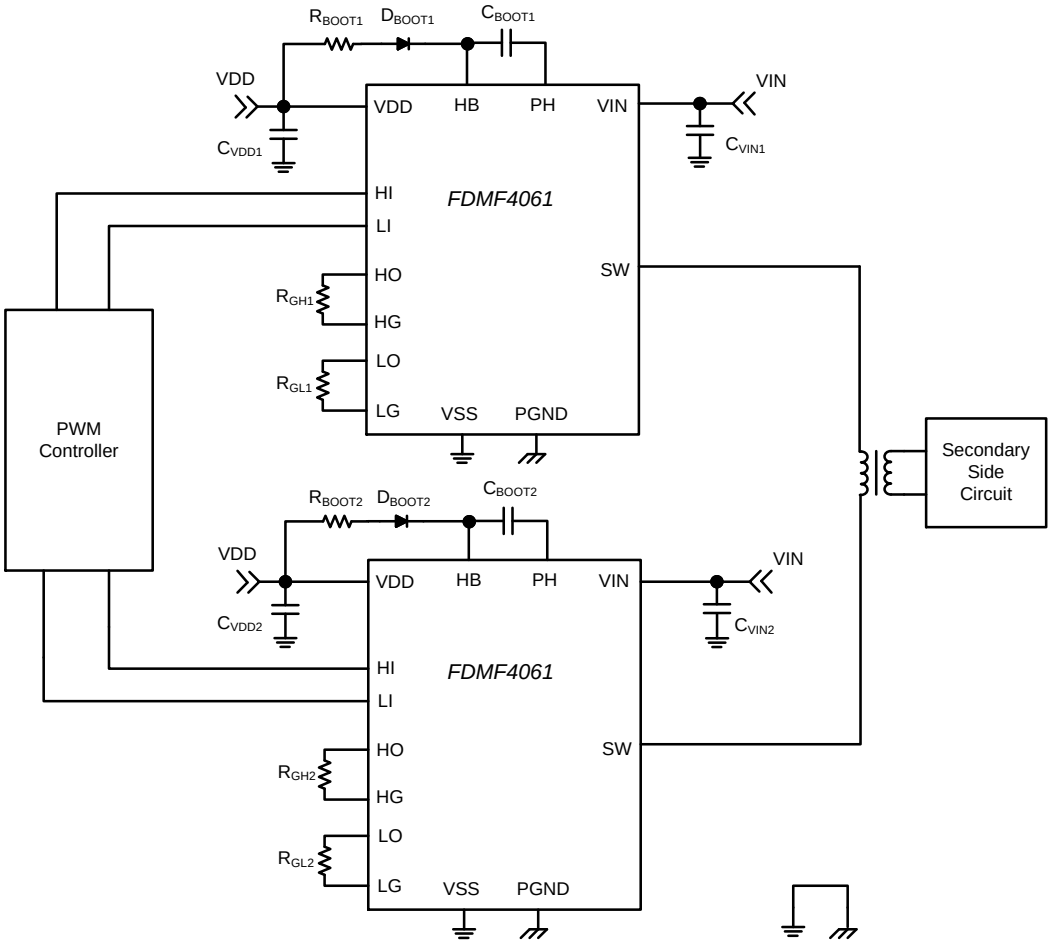


Figure 8. Full−Bridge Converter

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{IN}	Power Stage Supply Voltage	Referenced to VSS	−0.3	60	V
V_{PH}	PH Voltage	Referenced to VSS	V_{HB} − 25	V_{HB} + 0.3	V
V_{DD}	Driver Supply Voltage	Referenced to VSS	−0.3	25	V
V_{HB}	Bootstrap to VSS	Referenced to VSS	−0.3	85	V
V_{LI}, V_{HI}	Gate Drive Input Signals	Referenced to VSS	−0.3	V_{DD} + 0.3 V	V
V_{HO}	High Side Driver Output	Referenced to PHASE	V_{PH} − 0.3 V	V_{BOOT} + 0.3 V	V
V_{LO}	Low Side Driver Output	Referenced to VSS	−0.3	V_{DD} + 0.3V	V
V_{HG}	High Side MOSFET Gate	Referenced to PHASE	−26	28	V
V_{LG}	Low Side MOSFET Gate	Referenced to VSS	−26	28	V
Θ_{JA}	Junction to Ambient Thermal Resistance − Q1 (Note 1)		−	17	°C/W
	Junction to Ambient Thermal Resistance − Q2 (Note 1)		−	15	°C/W
T_J	Junction Temperature		−	150	°C
T_{STG}	Storage Temperature		−40	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on a 4−layer FR4 PCB with a dissipating copper surface on the top side of 49 cm^2, 2 oz.

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IN}	Power Stage Supply Voltage		3	50	V
V_{DD}	Driver Supply Voltage		10	20	V
V_{SW}, V_{PH}	SW or PHASE	DC	−0.3	60	V
		Repetitive Pulse (< 20 ns, 10 μJ)	6 − V_{DD}	60	V
V_{HB}	Voltage on HB	Reference to PH	V_{PH} + 10	V_{PH} + 20	V
dV_{SW}/dt	Voltage Slew Rate on SW		−	50	V/ns
T_J	Operating Temperature		−40	125	°C

Table 4. ELECTRICAL SPECIFICATIONS (V_{DD} = V_{HB} = 15 V, V_{SW} = V_{SS} = 0 V, V_{IN} = 30 V, T_J = +25°C unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SUPPLY CURRENTS						
I_{INQ}	Power Stage Quiescent Current	V_{LI} = V_{HI} = 0 V	–	–	1	μA
I_{DDQ}	Driver Quiescent Current	V_{LI} = V_{HI} = 0 V	–	67	180	μA
I_{DDO}	VDD operating Current	F_{SW} = 20 kHz	–	0.3	0.6	mA
		F_{SW} = 200 kHz	–	2.1	4.2	mA
I_{HBQ}	BOOT Quiescent Current	V_{LI} = V_{HI} = 0 V	–	38	120	μA
I_{HBO}	BOOT Operating Current	F_{SW} = 20 kHz	–	0.3	0.6	mA
		F_{SW} = 200 kHz	–	2.4	4.8	mA
UNDER−VOLTAGE PROTECTION						
V_{DDR}, V_{HBR}	UVLO Rising Threshold	V_{DD} or V_{HB}−V_{PH} rising threshold	8.2	9.5	10.0	V
V_{DDF}, V_{HBF}	UVLO Falling Threshold	V_{DD} or V_{HB}−V_{PH} falling threshold	7.6	8.9	9.6	V
V_{DDH}	UVLO Hysteresis	V_{DD} Hysterisis	–	0.6	–	V
t_{D_POR}	POR Delay to Enable IC	UVLO rising to internal PWM enable	–	–	10	μs
CONTROL INPUTS (TTL: LI, HI)						
V_{IL}	Low Level Input Voltage	V_{DD} = 10 V to 20 V	1.2	–	–	V
V_{IH}	High Level Input Voltage		–	–	2.9	V
V_{HYS}	Input Voltage Hysteresis		–	1.0	–	V
R_{IN}	Input Pull−Down Resistance		–	468	–	kΩ
PWM INPUT (HI,LI)						
t_{LPLH}	LI to LO Propagation Delays	LI *Low→HIGH* to LO *Low→HIGH,* V_{IH} to 10% LG	100	153	300	ns
t_{LPHL}		LI *High→Low* to LO *High→Low,* V_{IL} to 90% LG	100	208	300	ns
t_{HPLH}	HI to HO Propagation Delays	HI *Low→HIGH* to HO *Low→HIGH,* V_{IH} to 10% HG−PH	100	170	300	ns
t_{HPHL}		HI *High→Low* to HO *High→Low,* V_{IL} to 90% HG−PH	100	205	300	ns
MT	Delay Matching, HS and LS Turn−on/off		–	–	50	ns
t_{PW}	Minimum Input Pulse Width that Changes the Output	LI/HI Rising to Vth of Q1, Q2 R_G = 0 Ω	–	75	–	ns
		LI/HI Falling to Vth of Q1, Q2 R_G = 0 Ω	–	130	–	ns
HIGH−SIDE DRIVER (HDRV) (VDD = VHB = 15 V)						
I_{SOURCE_HO}	Output Sourcing Peak Current	V_{HO} = 0 V	250	350	–	mA
I_{SINK_HO}	Output Sinking Peak Current	V_{HO} = 15 V	500	650	–	mA
t_{R_HG}	Rise Time	GH = 10% to 90%, R_{GH} = 0 Ω	–	356	711	ns
t_{F_HG}	Fall Time	GH = 90% to 10%, R_{GH} = 0 Ω	–	151	302	ns
LOW−SIDE DRIVER (LDRV) (VDD = VHB = 15 V)						
I_{SOURCE_LO}	Output Sourcing Peak Current	V_{LO} = 0 V	250	350	–	mA
I_{SINK_LO}	Output Sinking Peak Current	V_{LO} = 15 V	500	650	–	mA
t_{R_LG}	Rise Time	GL= 10% to 90%, R_{GL} = 0 Ω	–	346	692	ns
t_{F_LG}	Fall Time	GL = 90% to 10%, R_{GL} = 0 Ω	–	142	283	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. FDMF4061 MOSFET ELECTRICAL SPECIFICATIONS (T_J = +25°C unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
HIGH SIDE MOSFET, Q1						
BV_{DSS}	Drain−Source Breakdown Voltage	I_{DS} = 250 uA, V_{GS} = 0 V	60	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate−Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V	–	–	100	nA
$V_{GS(th)}$	Gate−Source Threshold Voltage	V_{DS} = V_{GS} , I_{DS} = 250 μA	2.5	3.7	4.5	V
$R_{DS(ON)}$	Drain−Source On−Resistance	V_{GS} = 10 V, I_{DS} = 25 A	–	2.4	3.2	mΩ
Q_G	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 30 V, I_{DS} = 25 A	–	56	78	nC
Q_{GS}	Gate−Source Charge		–	23	–	nC
Q_{GD}	Gate−Drain “Miller” Charge		–	8	–	nC
Q_{OSS}	Total Output Charge		–	65	–	nC
R_G	Series Gate Resistance		–	1.0	–	Ω
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Forward Voltage	V_{HG} − V_{PH} = 0 V, I_{SD} = 2 A	–	0.7	1.2	V
		V_{HG} − V_{PH} = 0 V, I_{SD} = 25 A	–	0.8	1.3	
t_{RR}	Reverse Recovery Time	I_F = 25 A, di_F/dt = 100 A/μs	–	58	117	ns
Q_{RR}	Reverse Recovery Charge		–	51	103	nC
t_{RR}	Reverse Recovery Time	I_F = 25 A, di_F/dt = 300 A/μs	–	44	88	ns
Q_{RR}	Reverse Recovery Charge		–	79	158	nC
LOW SIDE MOSFET, Q2						
BV_{DSS}	Drain−Source Breakdown Voltage	I_{DS} = 250 μA, V_{GS} = 0 V	60	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate−Source Leakage Current	V_{DS} = 0 V, $V_{G\ S}$= ±20 V	–	–	100	nA
$V_{GS(th)}$	Gate−Source Threshold Voltage	V_{DS} = V_{GS} , I_{DS} = 250 μ A	2.5	3.5	4.5	V
$R_{DS(ON)}$	Drain−Source On−Resistance	V_{GS} = 10 V, I_{DS} = 25 A	–	2.4	3.2	mΩ
Q_G	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 30 V, I_{DS} = 25 A	–	59	82	nC
Q_{GS}	Gate−Source Charge		–	25	–	nC
Q_{GD}	Gate−Drain “Miller” Charge		–	11	–	nC
Q_{OSS}	Total Output Charge		–	63	–	nC
R_G	Series Gate Resistance		–	1.0	–	Ω
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Forward Voltage	V_{HG} − V_{PH} = 0 V, I_{SD} = 2 A	–	0.7	1.2	V
		V_{HG} − V_{PH} = 0 V, I_{SD} = 25 A	–	0.8	1.3	
t_{RR}	Reverse Recovery Time	I_F = 25 A, di_F/dt = 100 A/μs	–	57	114	ns
Q_{RR}	Reverse Recovery Charge		–	52	105	nC
t_{RR}	Reverse Recovery Time	I_F = 25 A, di_F/dt = 300 A/μs	–	43	86	ns
Q_{RR}	Reverse Recovery Charge		–	81	161	nC

TYPICAL PERFORMANCE CHARACTERISTICS

(Tj = 25°C unless otherwise noted)

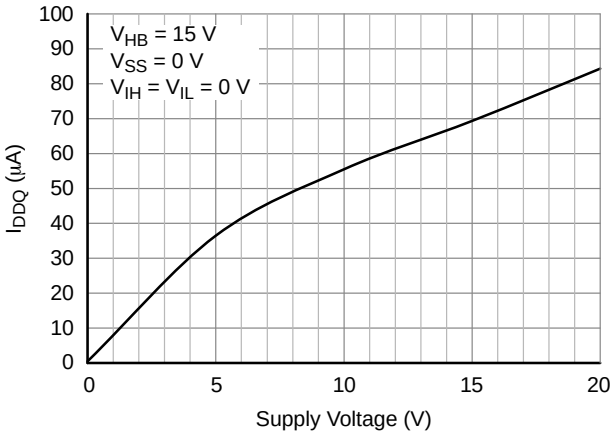


Figure 9. I_{DDQ} vs. Supply Voltage (V_{DD})

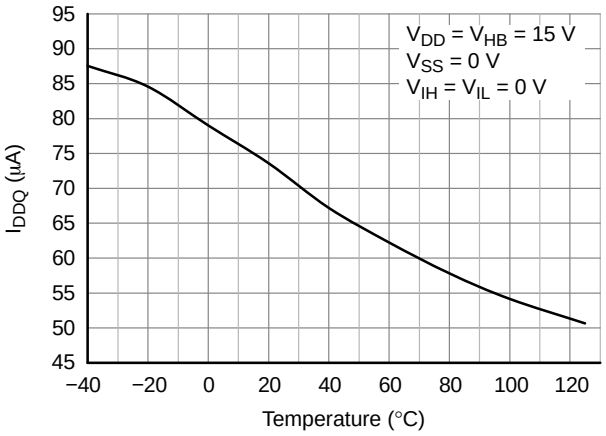


Figure 10. I_{DDQ} vs. Temperature

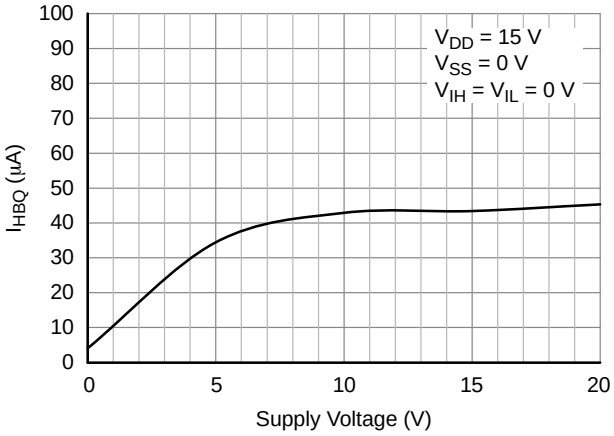


Figure 11. I_{HBQ} vs. Supply Voltage (V_{DD})

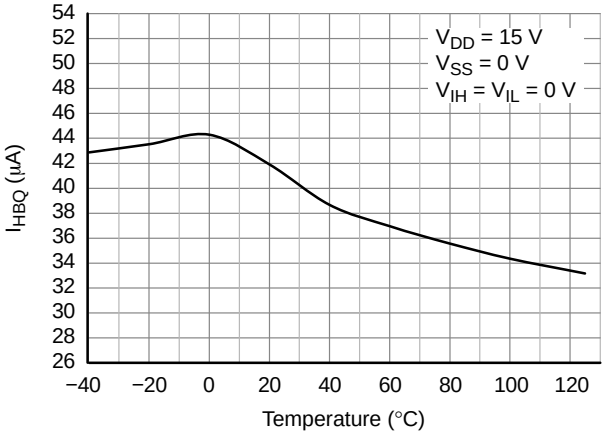


Figure 12. I_{HBQ} vs. Temperature

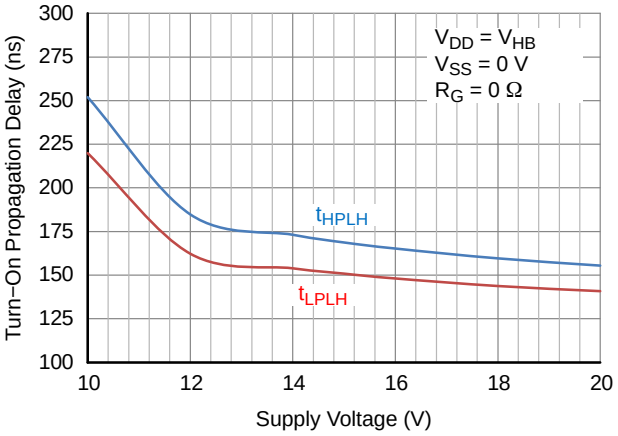


Figure 13. Turn−On Propagation Delay vs. Supply Voltage (V_{DD})

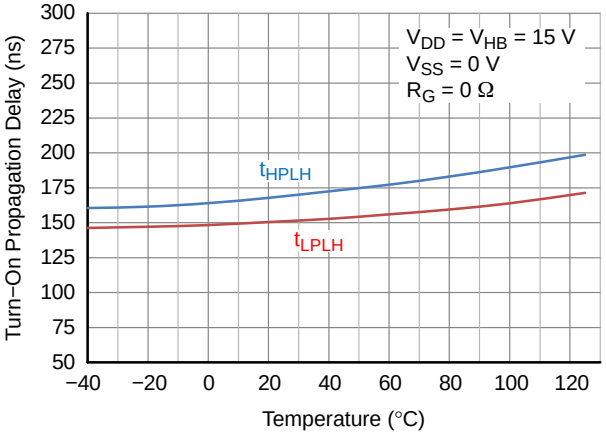


Figure 14. Turn−On Propagation Delay vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

(Tj = 25°C unless otherwise noted) (Continued)

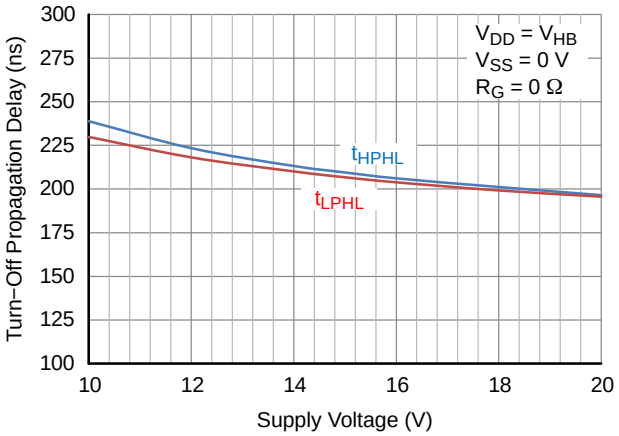


Figure 15. Turn−Off Propagation Delay vs. Supply Voltage (V_{DD})

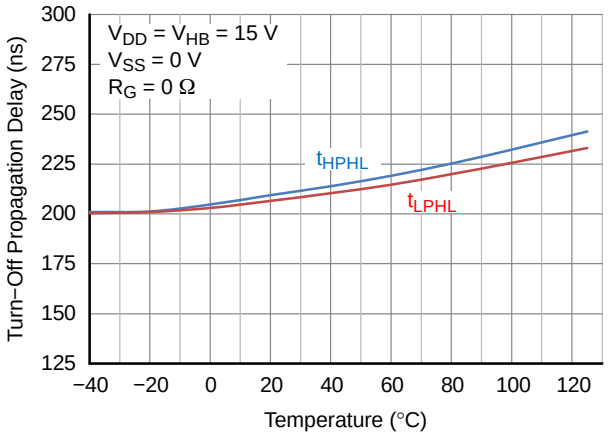


Figure 16. Turn−Off Propagation Delay vs. Temperature

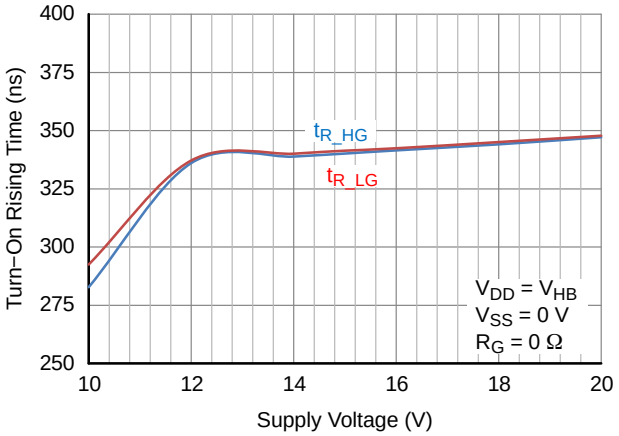


Figure 17. Turn−On Rising Time vs. Supply Voltage (V_{DD})

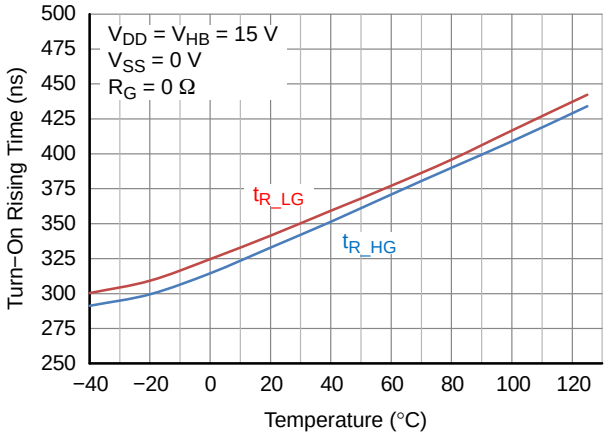


Figure 18. Turn−On Rising Time vs. Temperature

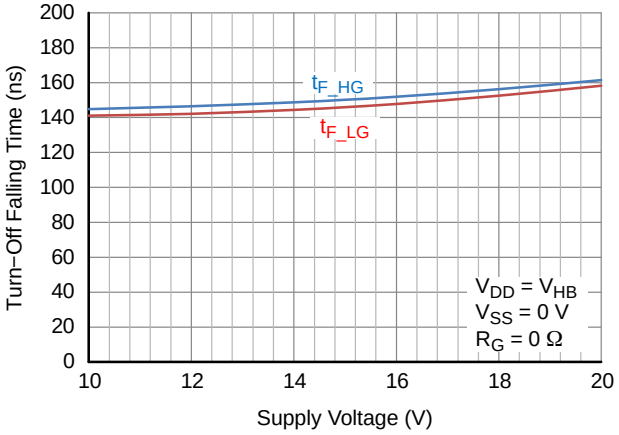


Figure 19. Turn−Off Falling Time vs. Supply Voltage (V_{DD})

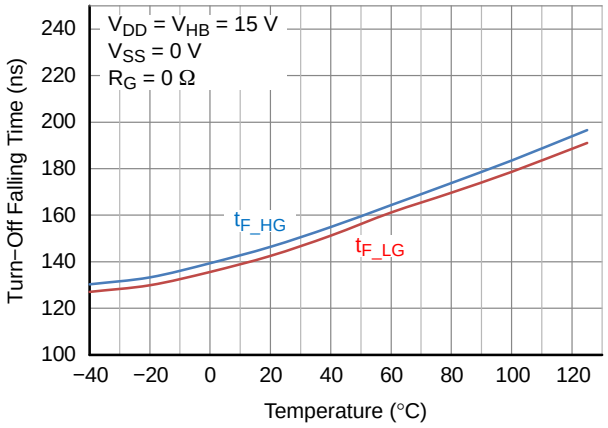


Figure 20. Turn−Off Falling Time vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

(Tj = 25°C unless otherwise noted) (Continued)

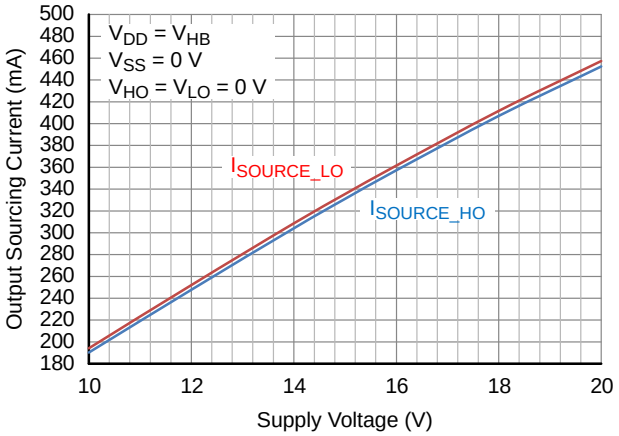


Figure 21. Output Sourcing Current vs. Supply Voltage (V_{DD})

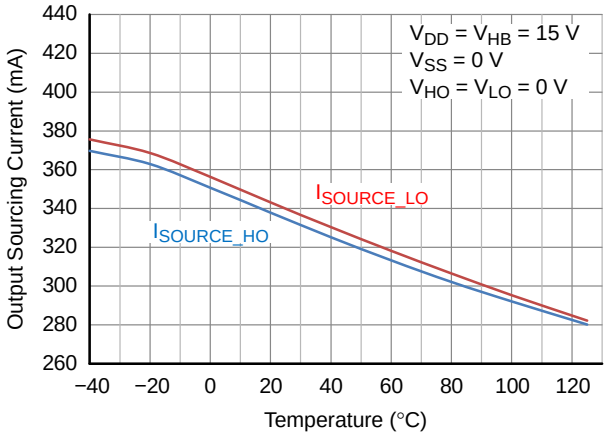


Figure 22. Output Sourcing Current vs. Temperature

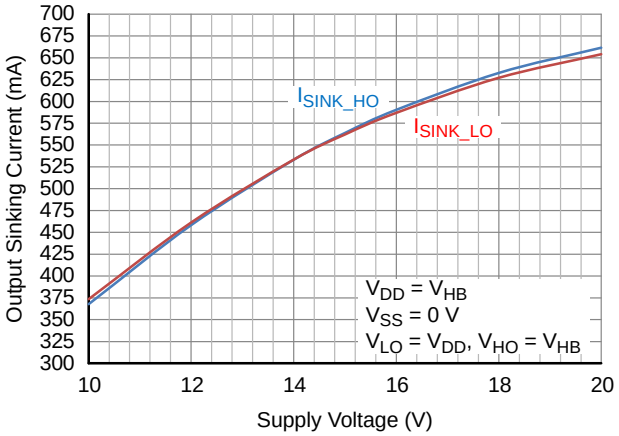


Figure 23. Output Sinking Current vs. Supply Voltage (V_{DD})

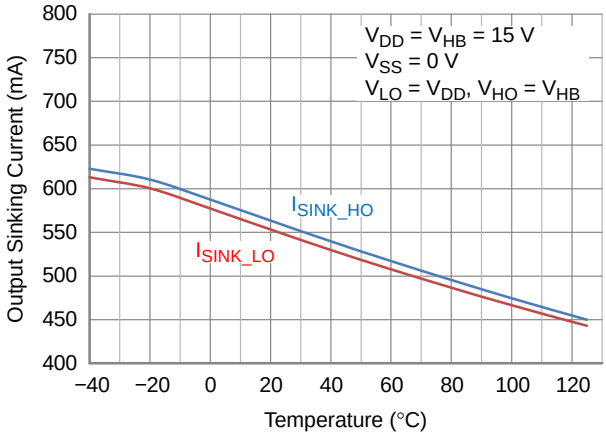


Figure 24. Output Sinking Current vs. Temperature

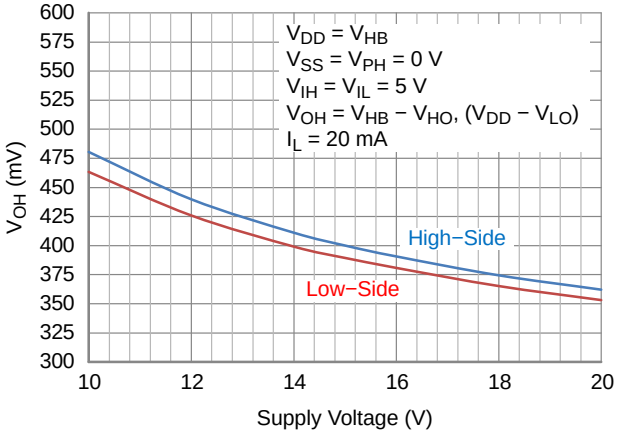


Figure 25. High−Level Output Voltage Deviation from the V_{BH} (V_{DD}) vs. Supply Voltage (V_{DD})

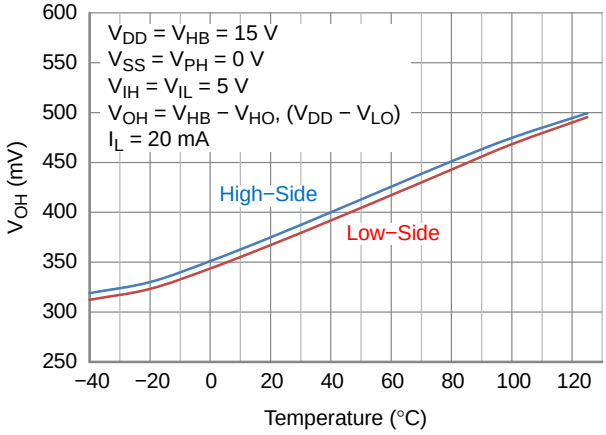


Figure 26. High−Level Output Voltage Deviation from the V_{BH} (V_{DD}) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

(Tj = 25°C unless otherwise noted) (Continued)

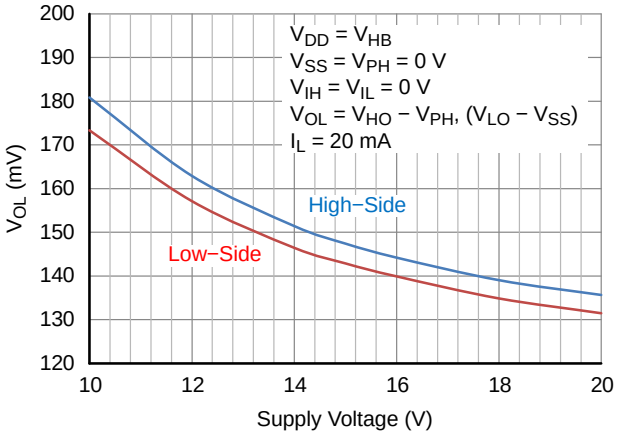


Figure 27. Low−Level Output Voltage Deviation from the V_{PH} (V_{SS}) vs. Supply Voltage (V_{DD})

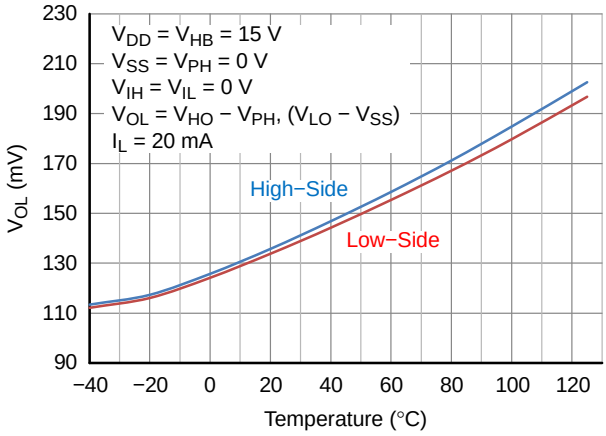


Figure 28. Low−Level Output Voltage Deviation from the V_{PH} (V_{SS}) vs. Temperature

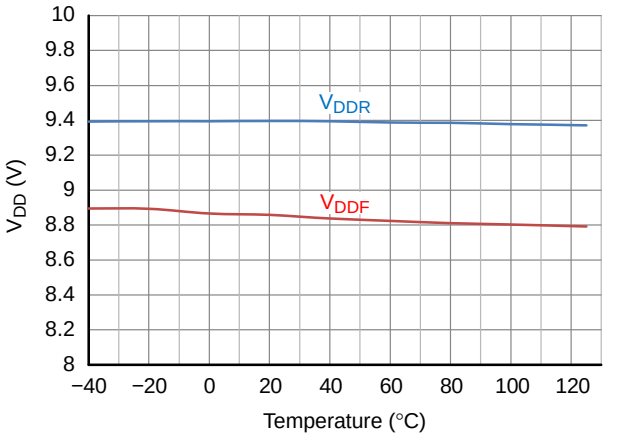


Figure 29. V_{DD} UVLO Threshold Voltage vs. Temperature

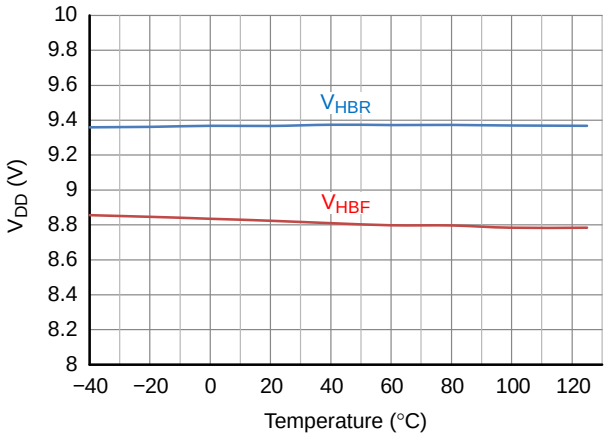


Figure 30. V_{HB} UVLO Threshold Voltage vs. Temperature

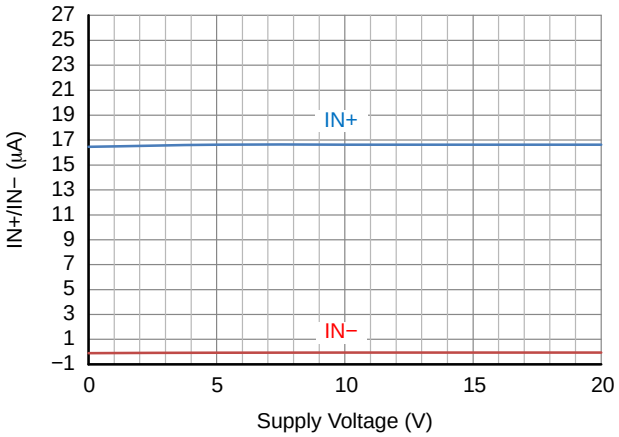


Figure 31. IN+ IN− vs. Supply Voltage (V_{DD})

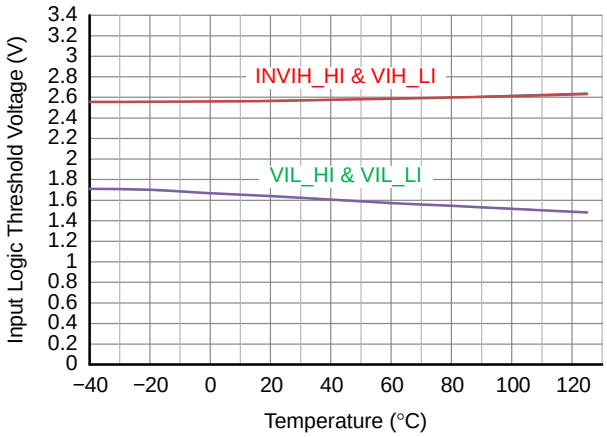


Figure 32. Input Logic Threshold Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

(Tj = 25°C unless otherwise noted) (Continued)

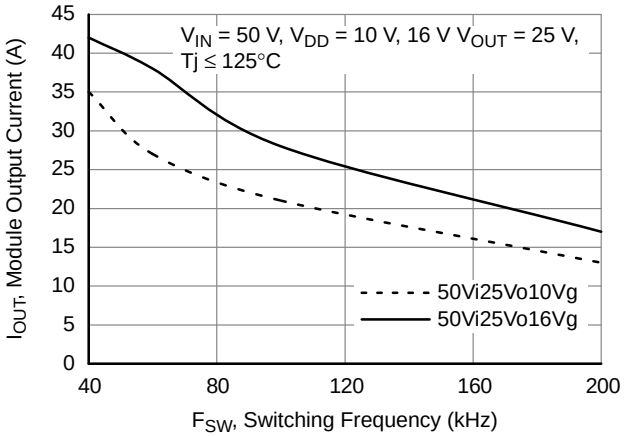


Figure 33. Static SOA, V_{IN} = 50 V

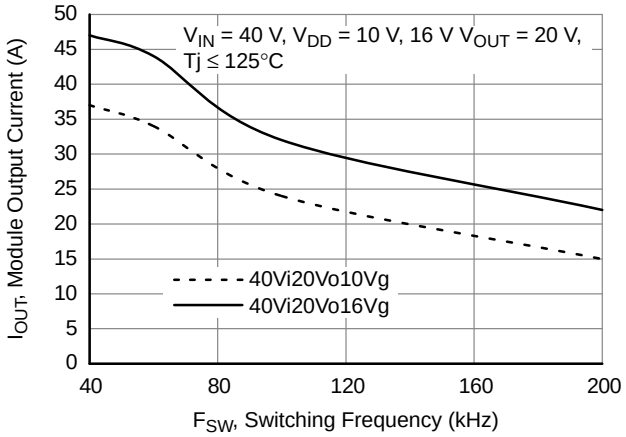


Figure 34. Static SOA, V_{IN} = 40 V

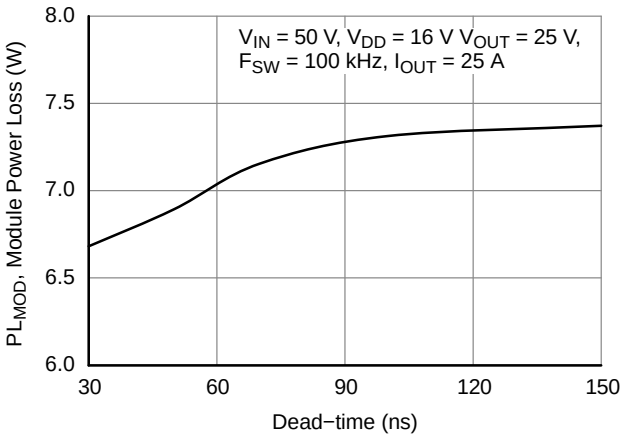


Figure 35. Module Power Loss vs. T_{DEAD}

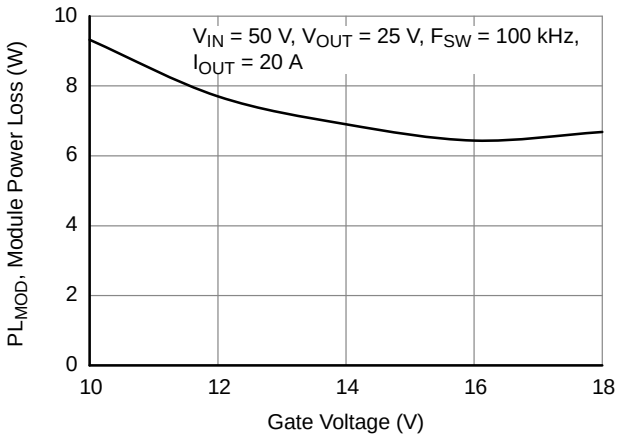


Figure 36. Module Power Loss vs. V_{GS}

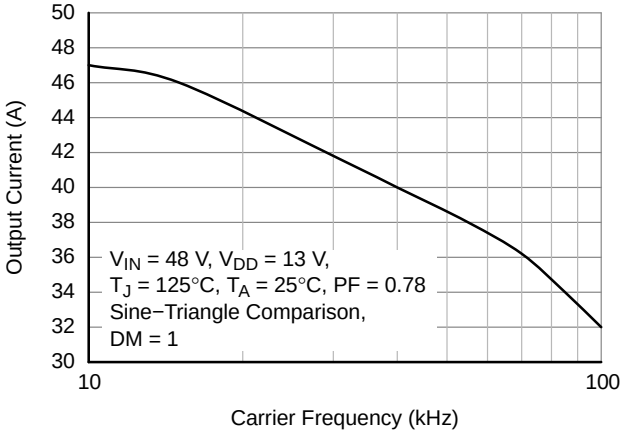


Figure 37. Output Current vs. Carrier or Modulation Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (Q1 N−CHANNEL)

(Tj = 25°C unless otherwise noted)

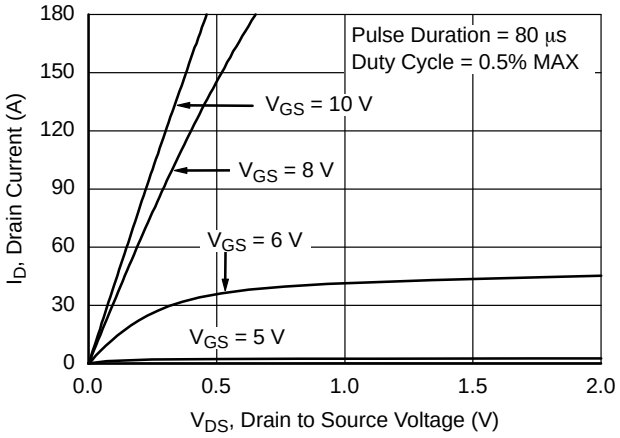


Figure 38. On Region Characteristics

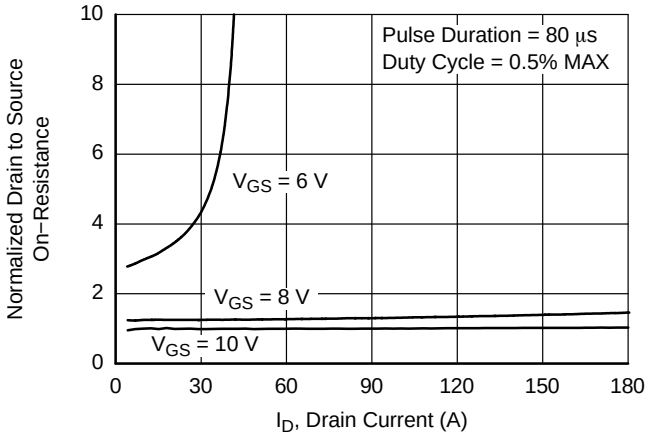


Figure 39. Normalized On−Resistance vs. Drain Current and Gate Voltage

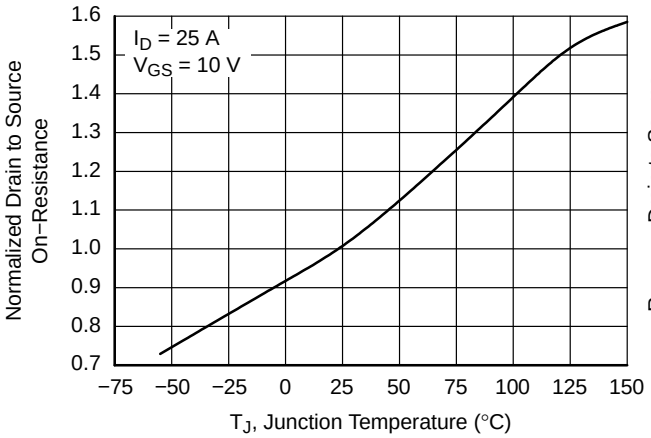


Figure 40. Normalized On Resistance vs. Junction Temperature

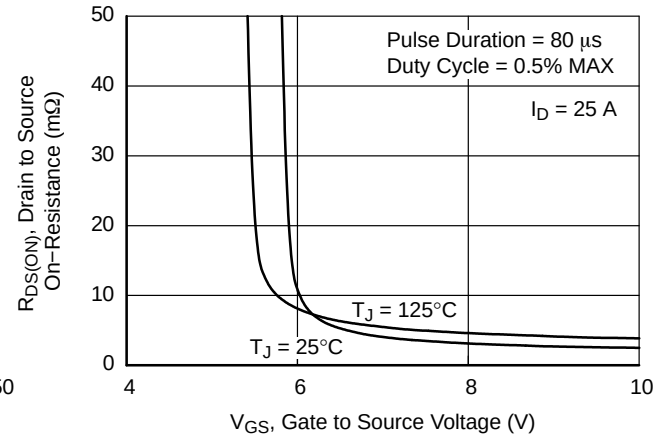


Figure 41. On−Resistance vs. Gate to Source Voltage

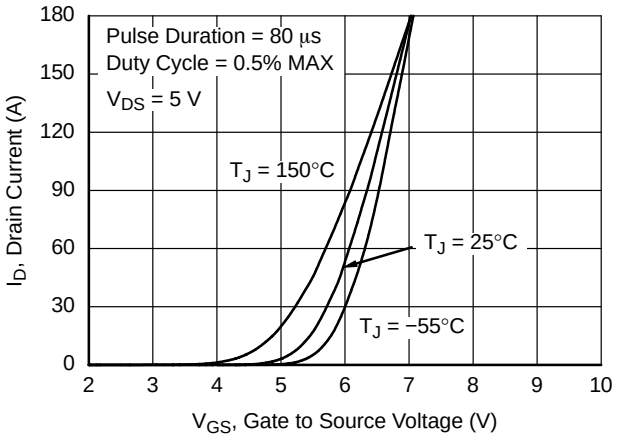


Figure 42. Transfer Characteristics

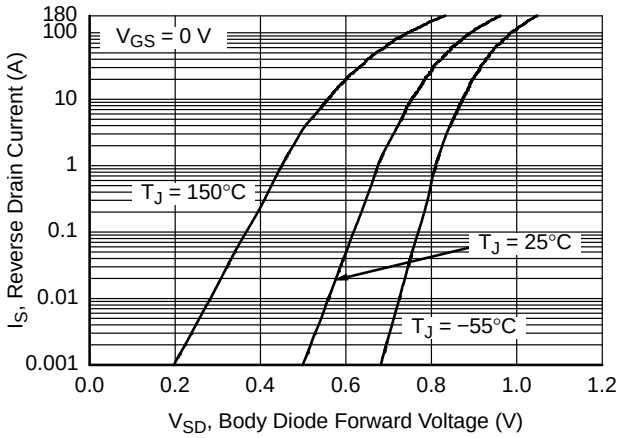


Figure 43. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (Q1 N−CHANNEL)

(Tj = 25°C unless otherwise noted) (Continued)

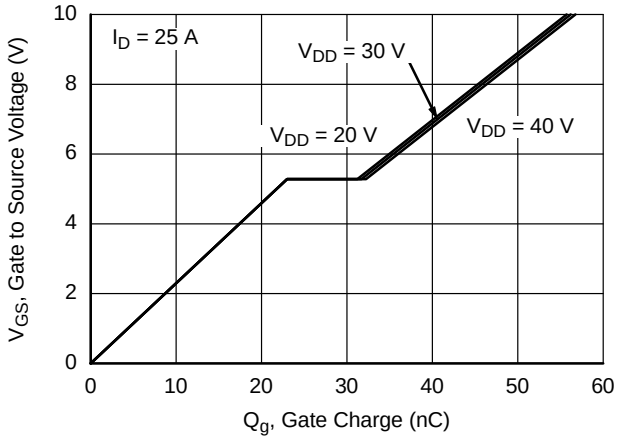


Figure 44. Gate Charge Characteristics

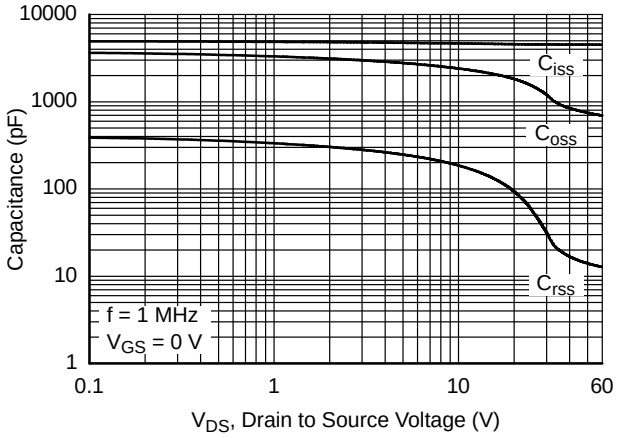


Figure 45. Capacitance vs. Drain to Source Voltage

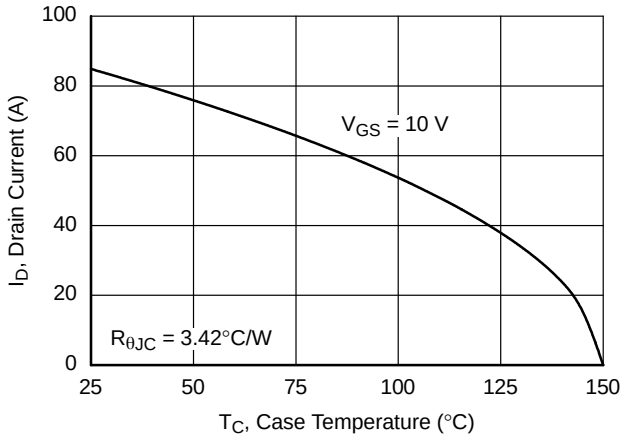


Figure 46. Maximum Continuous Drain Current vs. Case Temperature

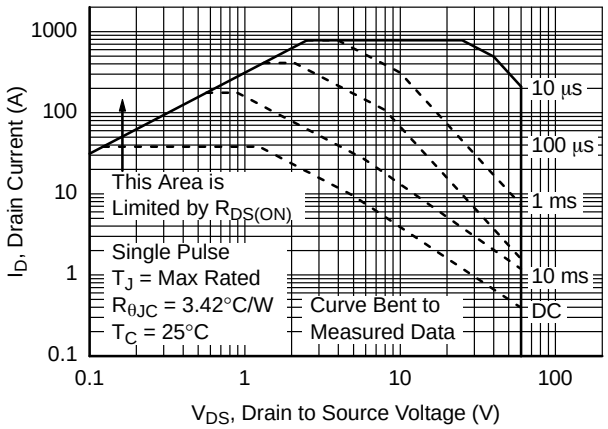


Figure 47. Forward Bias Safe Operating Area

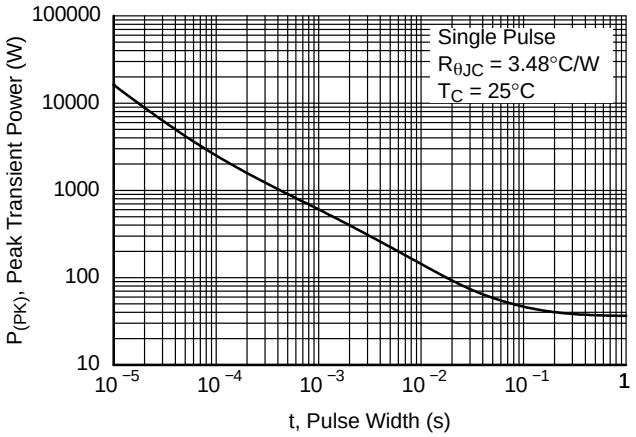


Figure 48. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS (Q1 N−CHANNEL)

(Tj = 25°C unless otherwise noted) (Continued)

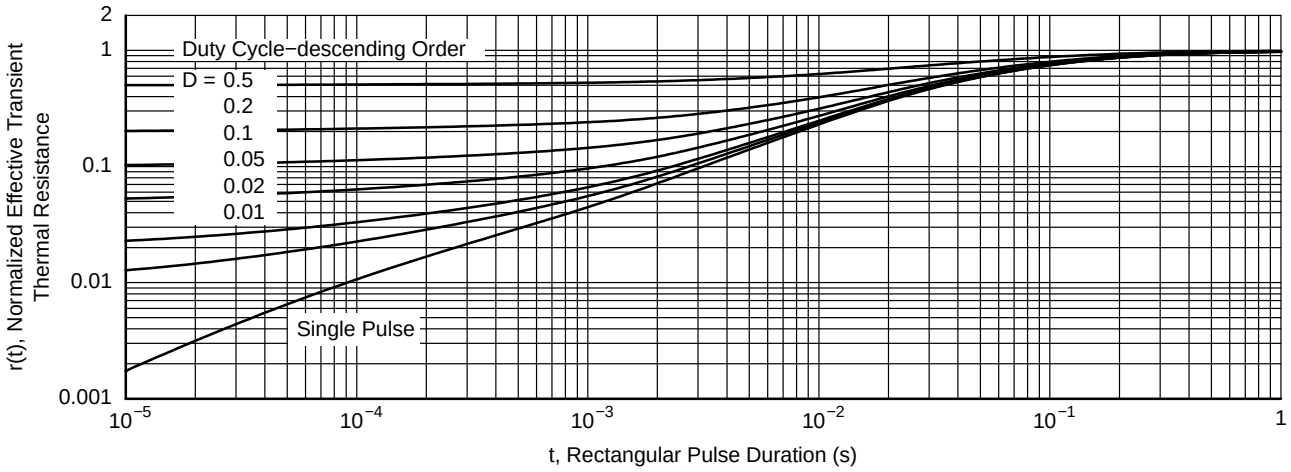


Figure 49. Junction−to−Case Transient Thermal Response Curve

TYPICAL PERFORMANCE CHARACTERISTICS (Q2 N−CHANNEL)

(Tj = 25°C unless otherwise noted)

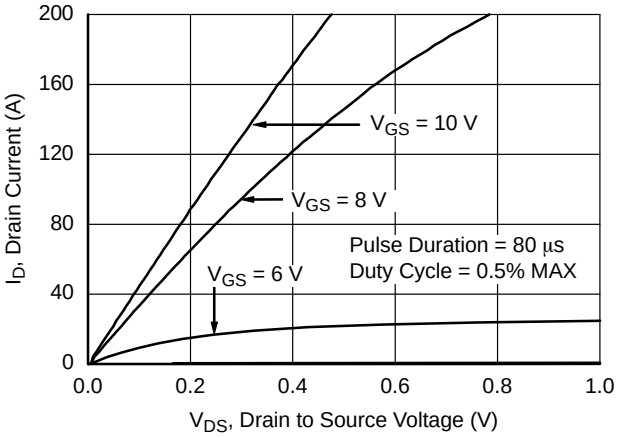


Figure 50. On−Region Characteristics

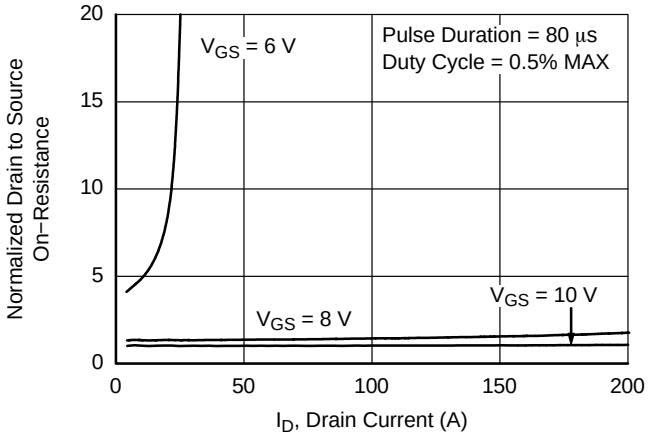


Figure 51. Normalized On−Resistance vs. Drain Current and Gate Voltage

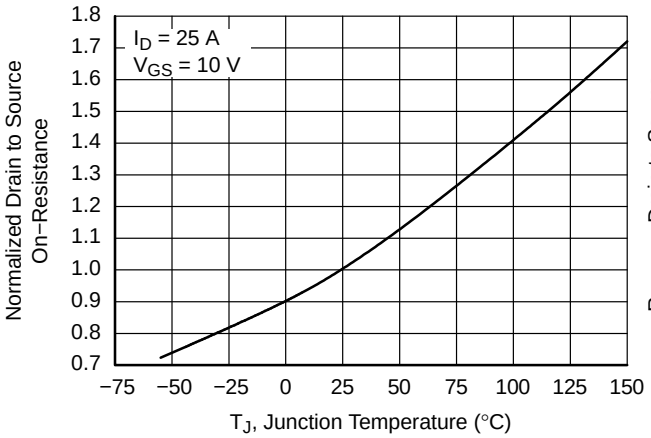


Figure 52. Normalized On Resistance vs. Junction Temperature

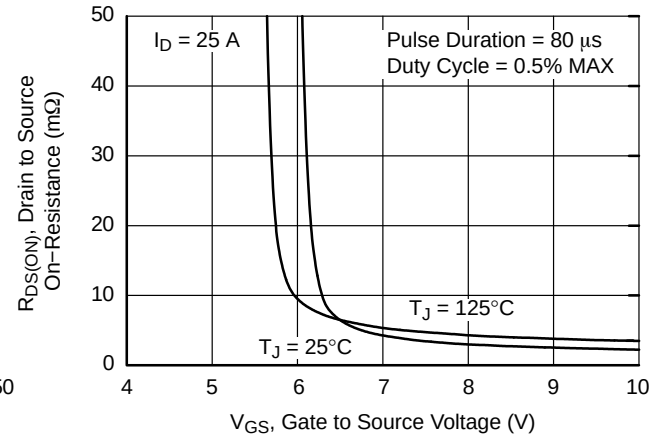


Figure 53. On−Resistance vs. Gate to Source Voltage

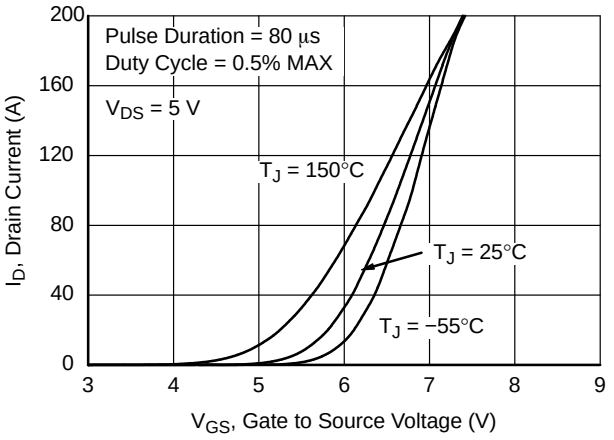


Figure 54. Transfer Characteristics

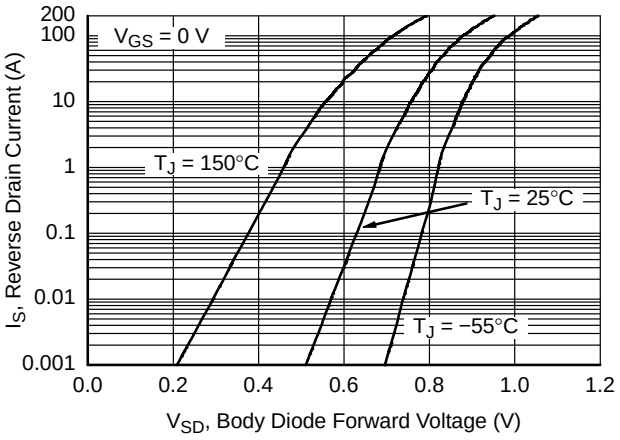


Figure 55. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (Q2 N−CHANNEL)

(Tj = 25°C unless otherwise noted) (Continued)

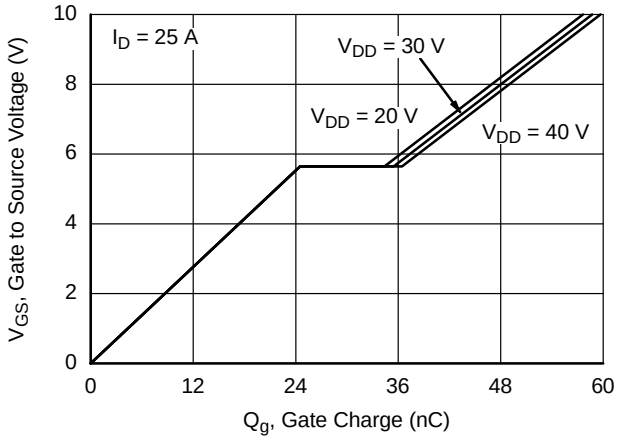


Figure 56. Gate Charge Characteristics

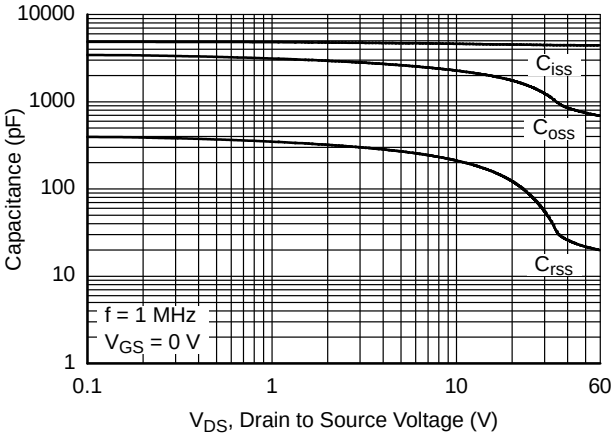


Figure 57. Capacitance vs. Drain to Source Voltage

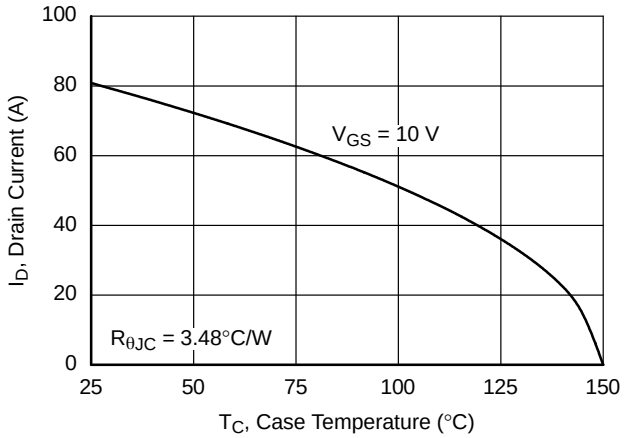


Figure 58. Maximum Continuous Drain Current vs. Case Temperature

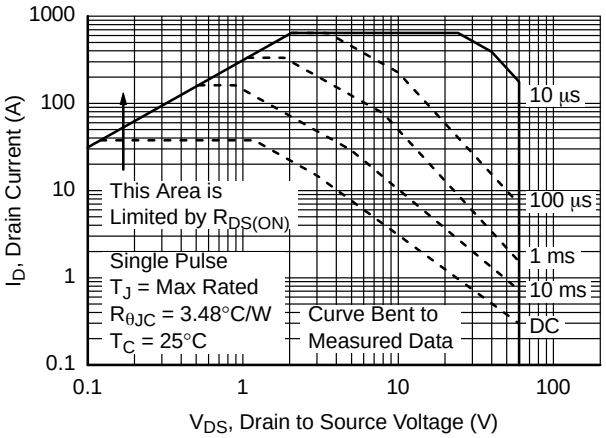


Figure 59. Forward Bias Safe Operating Area

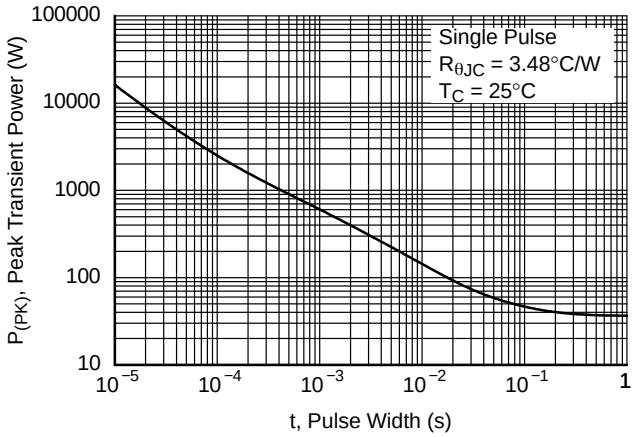


Figure 60. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS (Q2 N−CHANNEL)

(Tj = 25°C unless otherwise noted) (Continued)

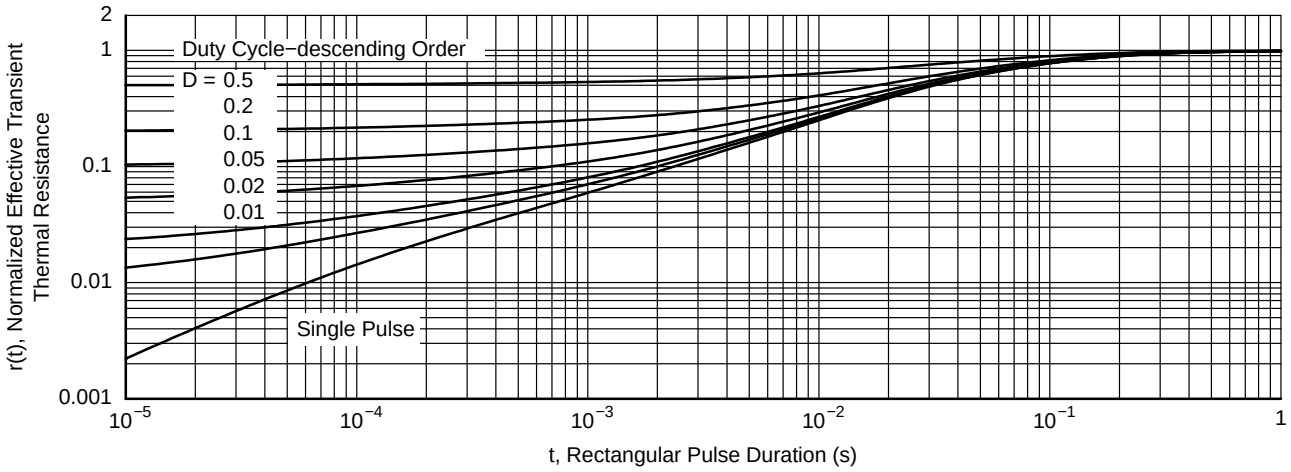


Figure 61. Junction−to−Case Transient Thermal Response Curve

FUNCTIONAL DESCRIPTION

The FDMF4061 is a non−inverting 60 V half−bridge Smart Power Stage (SPS) module. The module packages a driver IC die along with pair of equally sized (matched R_{DSON}) 60 V POWERTRENCH N−Channel MOSFETs (Standard gate thresholds refer to *Table 5*).

The FDMF4061 module provides separate power input pins; the power stage input (VIN) and the gate driver input (VDD). The power stage input (VIN) accepts a wide operating from 3 V to 50 V, while the gate driver input (VDD) requires 10 V to 20 V. The module accepts TTL compatible inputs (HI/LI) along with anti−cross conduction circuitry to protect against over−lapping PWM (HI/LI) pulses. The module (driver IC) also implements UVLO circuitry in both the VDD−VSS and BOOT−PH power domains.

Power−Up and UVLO Operation

UVLO circuits are implemented in both the VDD−VSS and HB−PH power domains. During power−up, the VDD−VSS UVLO circuit forces HO and LO low until the VDD supply voltage exceeds the UVLO rising threshold (9.2 V typ.). The module (driver IC) will begin responding to PWM pulses once VDD exceeds the UVLO threshold. The UVLO circuit does contain hysteresis (~0.6 V) to prevent noise from interfering with normal operation. An additional UVLO circuit is implemented on the HB−PH pins which will hold HO low until HB−PH > (9.2 V typ.). The HB−PH UVLO also incorporates hysteresis (~0.6 V).

Table 6. UVLO TRUTH TABLE

VDD UVLO	BOOT UVLO	Driver State
0	X	Disabled (GH, GL=0)
1	0	GL follows PWM , GH=0)
1	1	Enabled (GH/GL follow PWM)

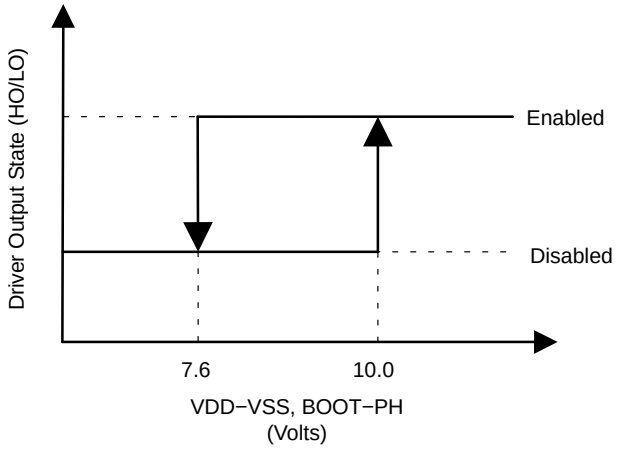


Figure 62. Min/Max UVLO Thresholds

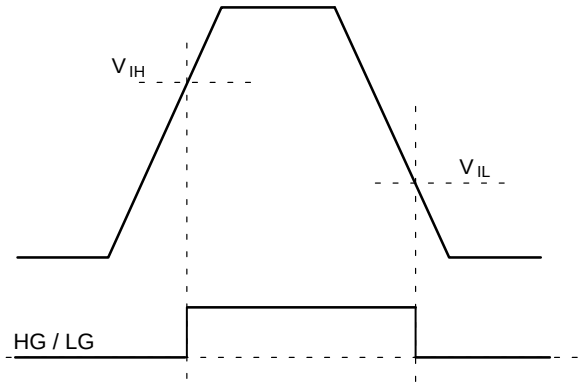


Figure 63. PWM Threshold Definitions

- V_{IH} = PWM trip level to flip state from LOW to HIGH.
- V_{IL} = PWM trip level to flip state from HIGH to LOW.

Driver Output Stage

The driver IC output stage is designed to drive a pair of N−channel MOSFETs. The driver outputs (LO, HO) are non−inverting and will follow the PWM input commands (LI, HI respectively). The LO and HO outputs are capable of sinking and sourcing up to 0.65/0.35 A peak current respectively.

The driver output stage is also capable of providing a rail (VDD) to rail (VSS) output voltage level when driving the Power MOSFETs. Depending on the end application, the output voltage level can be set to aide in optimizing MOSFET and driver IC power losses. The driver output voltage level can also be used to help adjust SW node edge rates.

Timing Diagram

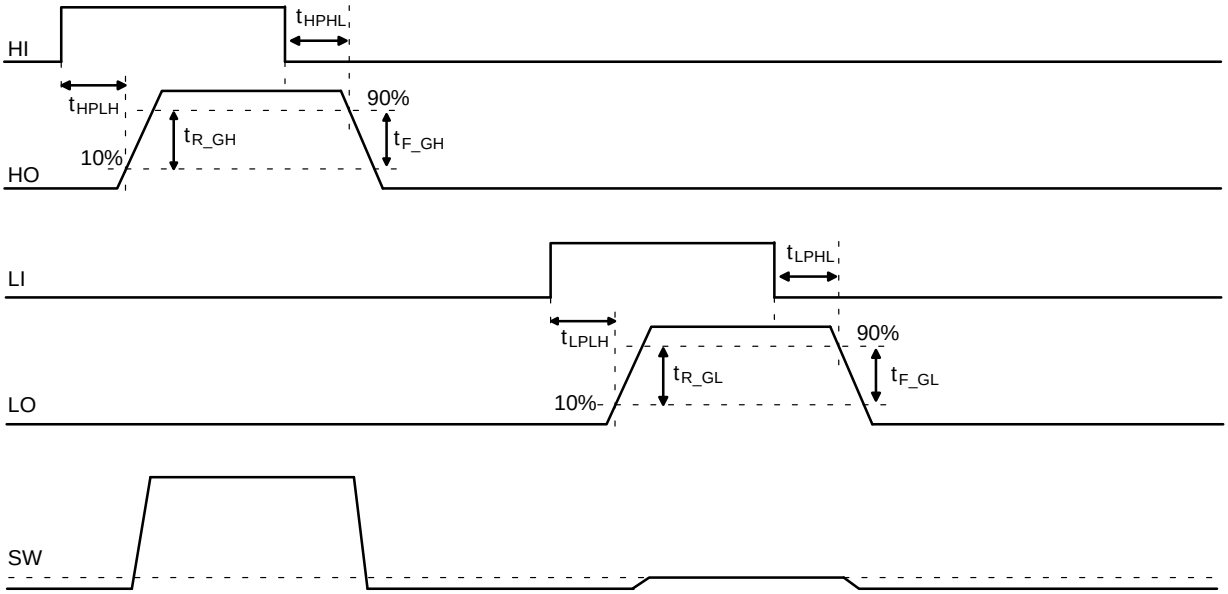


Figure 64. PWM Timing Diagram (LI / HI Signals)

APPLICATION INFORMATION

The FDMF4061 is designed as a non−inverting power stage, where the Power MOSFET response (SW node) is designed to follow to HI/LI commands. The device is well−suited to be used in a wide variety of applications, such as: Half and Full−Bridge DC−DC converters, Active Clamp Forward converters, rectifier circuits, and motor drive power stages. However, various applications and topologies can place unique stresses on the module. There are a few basic power−stage requirements needed to ensure proper operation.

Module Power Dissipation

As previously mentioned, the FDMF4061 is a multi−chip module (MCM). The module consists of three die (HS MOSFET, LS MOSFET and driver IC). Each die dissipates heat in normal operation resulting from power loss. The power MOSFETs can generate power loss from conduction and switching losses while the driver IC dissipated loss from bias, boot diode conduction and from the driver output stage sinking and sourcing power MOSFET gate currents and operating frequency. The amount of heat dissipated by any die is largely dependent on the operating conditions. The close physical placement of the three die inside of the package translates into strong thermal coupling between die. Ideally, a thermal camera should be used to monitor the FDMF4061 during the engineering development phase. This can help ensure the module operates within the absolute maximum ratings specified in this datasheet.

Operating Modes

The FDMF4061 can reliably operate while driving various load impedances. However, the relatively large number of applications can result in the module operating in various modes. Common applications such as switching power converters and motor drives can place the FDMF4061 into different operating modes. The various operating modes will change the response of the MOSFET voltage and current stresses and power losses as well as the gate driver dead time response. A few operating modes are listed below.

H−bridge Motor Drive

In this operating mode, it allows bi−directional current flow through motor by enabling diagonal MOSFETs to make current flow in one or the other direction. Inductor current will not tolerate abrupt changes either when charged or discharged and alternate path is required to protect switches during dead−time. The path can be made either MOSFET body−diode conducting as soon as switches are disabled or enabling opposite high−side or low−side switch to carry the recirculation current while avoiding shoot−through. Utilizing MOSFET channel is often much more efficient way to handle the decaying current due to lower conduction power loss than body−diode forward drop loss.

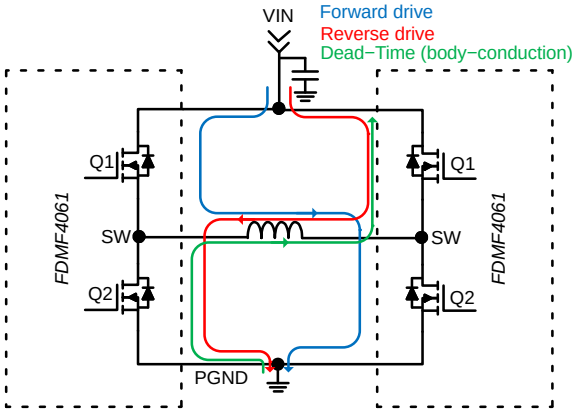


Figure 65. H−bridge Motor Drive

FDMF4061 Power Dissipation

The maximum motor drive current can be obtained from estimating total power dissipation of motor driver. There are a number of factors which limit actual current level such as motor ratting, driver IC, PCB construction, ambient temperature and given application. All of power dissipation components must be considered to get reliable operation at the specific application. There is obvious power dissipations listed below in single H−bridge motor application.

- Conduction loss − Generally biggest power loss which is dissipated due to the $R_{DS(ON)}$ and its temperature coefficient must be considered in the calculation

$$P_{COND} = \left(R_{DS(ON)-HS\_temp} + R_{DS(ON)-LS\_temp}\right) \cdot I_{OUT}^{2} \quad \text{(eq. 1)}$$

- Switching losses − Rising and falling time by parasitic inductance can be measured in the application, listed below assumed zero inductance.

Switching OFF loss

$$P_{SW(OFF)} = \left(\frac{V_{IN} \cdot I_{DS(OFF)} \cdot t_{OFF}}{2}\right) \cdot F_{SW} \quad \text{(eq. 2)}$$

where:

$t_{OFF} = \left(Q_{GS2} + Q_{GD}\right) / i_{G(OFF)}$;

$i_{G(OFF)} = V_{PLATEAU} / \left(R_{GH} + R_{DRV\_OFF}\right)$

Switching ON loss

$$P_{SW(ON)} = \left(\frac{V_{IN} \cdot I_{DS(ON)} \cdot t_{ON}}{2} + \frac{Qoss \cdot V_{IN}}{2}\right) \cdot F_{SW} \quad \text{(eq. 3)}$$

where:

$t_{ON} = \left(Q_{GS2} + Q_{GD}\right) / i_{G(ON)}$;

$i_{G(ON)} = V_{PLATEAU} / \left(R_G + R_{DRV\_ON}\right)$

Qoss = Output Charge

- Gate drive loss

$$P_{GATE} = Q_G \cdot V_{DRV} \cdot F_{SW} \quad \text{(eq. 4)}$$

- Quiescent current power loss − Current is still drawn from the VDD and HB pins for internal and level shifting circuitry without load (R_G = Open). Power loss by quiescent current is

$$P_{Quiescent} = V_{DD} \cdot I_{DDQ} + V_{HB} \cdot I_{HBQ} \quad \text{(eq. 5)}$$

- Supply current power loss (R_G = 0 Ω) is

$$P_{supply} = V_D \cdot I_{DDO} + V_{HB} \cdot I_{HBO} \quad \text{(eq. 6)}$$

- Total power loss in the FDMF4061 is equal to the power dissipation caused by gate driver and Power MOSFETs,

$$P_{total} = P_{Cond} + P_{SW} + P_{Gate} + P_{supply} \quad \text{(eq. 7)}$$

Once the designer estimates power dissipation in the gate driver and MOSFETs, junction temperature can be calculated using thermal resistance (Θ_{JA}) and ambient temperature as followings and also can calculate maximum allowable motor current:

$$T_j = T_A + \left(\Theta_{JA} \cdot P_{total}\right) \quad \text{(eq. 8)}$$

Continuous Current Flowing Out of SW Node

Continuous current flowing out of the module SW node is typical of a heavily loaded switched−mode power stage that is operating in a synchronous buck converter topology. In this mode, the power stage is supplying current from VIN into an inductive load. *Figure 66* shows and example of a synchronous buck convert operating in CCM with positive inductor current.

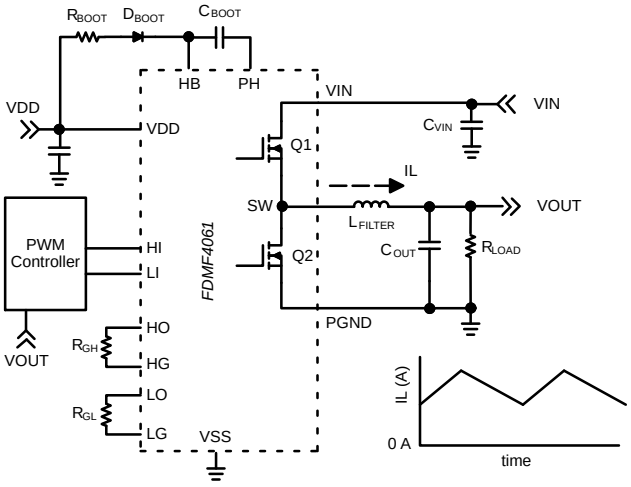


Figure 66. Synchronous Buck Operating in CCM with Positive Inductor Current

During this operating mode, the HS MOSFET (Q1) will undergo hard−switched inductive turn−on and turn−off events, while LS MOSFET (Q2) will undergo soft switching and body diode recovery. Hard−switching often results in large switching spikes on Q1 and Q2 V_{DS} as well as PH to VSS and BOOT to VSS pins. Peak switching spikes are often positively correlated to load current.

Continuous Current Flowing into SW Node

Continuous current flowing into the module SW node is typical of a heavily loaded switched−mode power stage that is operating in a synchronous boost converter topology.

Continuous inductor current flowing in to the module SW node is typical operation of a synchronous boost converter, as shown in *Figure 67*.

However, similar operation can arise when a switching converter (such as a synchronous buck) is pulling energy from the output filter capacitors and delivering the energy back to the input filter capacitors.

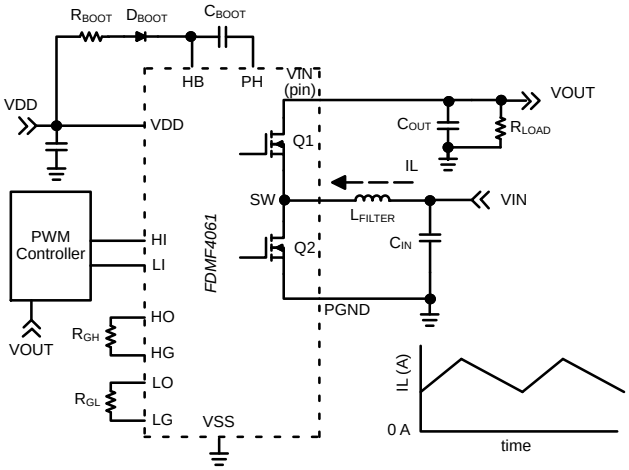


Figure 67. Synchronous Boost Converter Operating in CCM

From a module perspective, the main difference here versus the previous (buck) operating mode is that this situation will cause the LS FET (Q2) to act as the control MOSFET and hard switch while the HS FET (Q1) acts as a synchronous rectifier and undergoes soft switching with body diode recovery. This type of operation can drastically change power losses dissipated in Q1 and Q2 versus buck operating mode.

dV_{DS}/dt Control Using External Gate Resistors

The FDMF4061 also provides module pins for placing external gate resistors. The module provides pins for the HO and LO signals (driver output signals) and the HG and LG (Power MOSFET gate pins). Resistors can be placed in series with the MOSFET gate to control the SW node edge rates.

Independently controlling MOSFET (slower) turn−on and (faster) turn−off slew rates can also be accomplished by using the resistor and diode circuit shown in *Figure 68*.

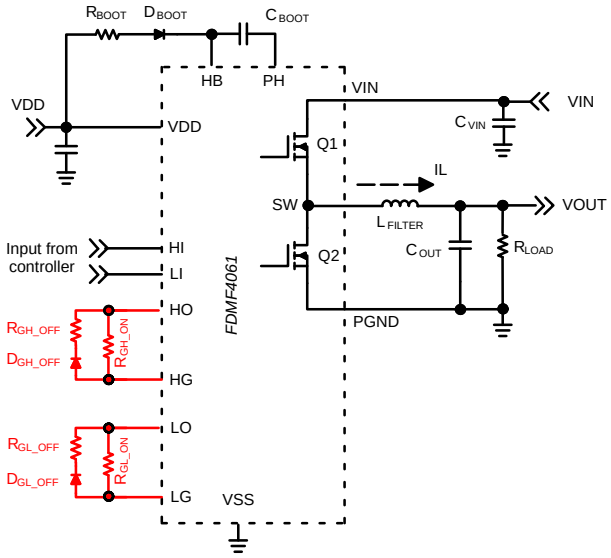


Figure 68. Gate Drive Resistor−Diode Circuit

C_{GD} x dV_{DS}/dt Turn−on

C_{GD} x dV_{DS}/dt turn−on is a false (unwanted) turn−on event that often creates a brief and uncontrolled shoot through current between the HS (Q1) and LS (Q2) MOSFETs.

Typically, a C_{GD} x dV_{DS}/dt "shoot−through" condition arises from capacitive feedback current flowing through C_{GD} into C_{GS} inducing a gate−bounce−induced channel turn−on of the MOSFET. Holding the gate below threshold can become challenging because the high− frequency capacitive displacement current from C_{GD} (due to dV_{DS}/dt) couples back to circuit ground through the gate electrode.

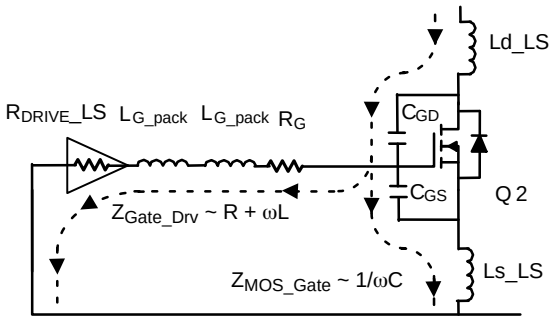


Figure 69. CGD x dV_{DS}/dt Current Flow

The gate−to−ground impedance is the parallel combination of the gate drive (Z_{G_DRV}) and the MOSFET gate−to−source (Z_{MOS_Gate}) paths. As dV_{DS}/dt increases, the more favorable path for displacement current is through the capacitive gate−source (C_{GS}) path versus the highly inductive and resistive gate drive loop. So impedence through gate driver should be minimized. The severity of the shoot through current is difficult to predict.

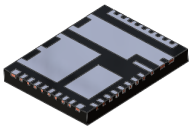
ORDERING INFORMATION

Part Number	Device Marking	Current Rating (A)	Input Voltage (V)	Frequency Max (kHz)	Package Type	Shipping†
FDMF4061	FDMF4061	25	60	200	PQFN36 6X7.5, 0.5P (Pb−Free and Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



PQFN36 6X7.5, 0.5P
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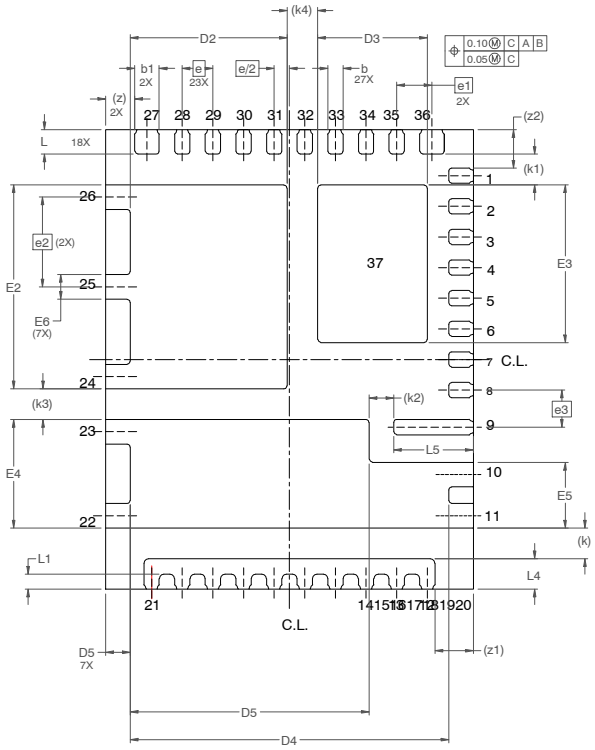
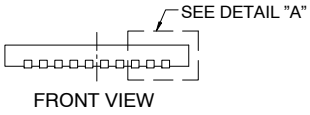
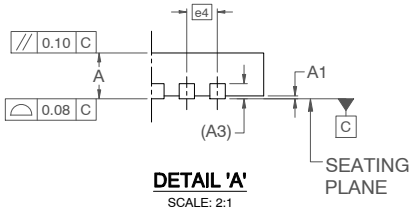
DATE 07 JUN 2021



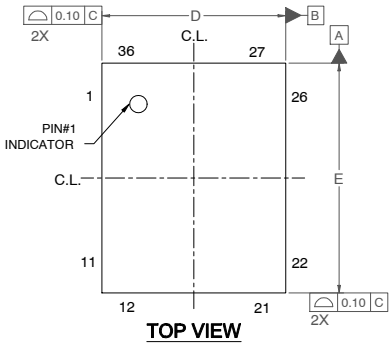
BOTTOM VIEW
SCALE: 2:1



FRONT VIEW



DETAIL 'A'
SCALE: 2:1



TOP VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20 REF	
b	0.20	0.25	0.30
b1	0.20	0.40	0.30
D	5.90	6.00	6.10
D2	2.46	2.56	2.66
D3	1.69	1.79	1.89
D4	5.10	5.20	5.30
D5	3.80	3.90	4.00
D6	0.30	0.40	0.50
E	7.40	7.50	7.60
E2	3.22	3.32	3.42
E3	2.47	2.57	2.67
E4	1.67	1.77	1.87
E5	0.97	1.07	1.17
E6	0.35	0.40	0.45
e		0.50 BSC	
e/2		0.25 BSC	
e1		0.575 BSC	
e2		1.464 BSC	
e3		0.60 BSC	
k		0.50 REF	
k1		0.50 REF	
k2		0.40 REF	
k3		0.50 REF	
k4		0.50 REF	
L	0.30	0.40	0.50
L1	0.14	0.24	0.34
L4	0.40	0.50	0.60
L5	1.20	1.30	1.40
z		0.475 REF	
z1		0.625 REF	
z2		0.625 REF	

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PQFN36 6X7.5, 0.5P
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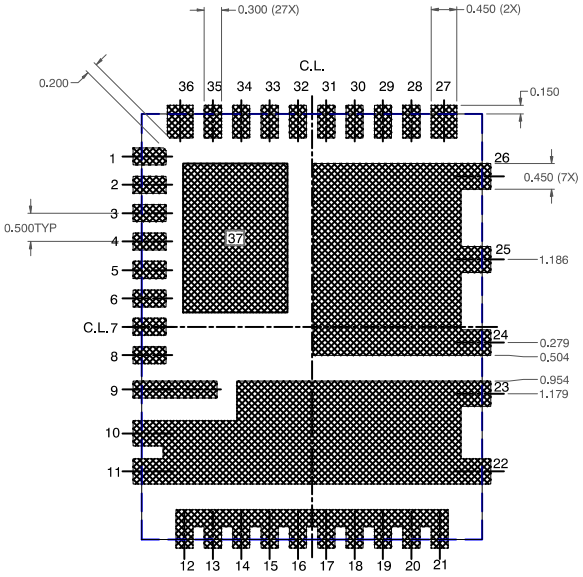

LAND PATTERN RECOMMENDATION
SCALE 2:1

***FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.**

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO JEDEC MO-220, ISSUE K.01, DATED AUG 2011.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

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