

MOSFET – P-Channel, POWERTRENCH®

-150 V, -2.6 A, 1.2 Ω

FDMC86265P

General Description

This P-Channel MOSFET is produced using **onsemi's** advanced POWERTRENCH process that has been optimized for the on-state resistance and yet maintain superior switching performance.

Features

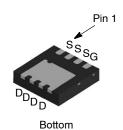
- Max $r_{DS(on)} = 1.2 \Omega$ at $V_{GS} = -10 \text{ V}$, $I_D = -1 \text{ A}$
- Max $r_{DS(on)} = 1.4 \Omega$ at $V_{GS} = -6 \text{ V}$, $I_D = -0.9 \text{ A}$
- Very Low RDS-On Mid Voltage P-Channel Silicon Technology Optimized for Low Qg
- This Product is Optimized for Fast Switching Applications as well as Load Switch Applications
- 100% UIL Tested
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

Applications

- Active Clamp Switch
- Load Switch



Top



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WDFN8 3.3x3.3, 0.65P CASE 511DH

MARKING DIAGRAM



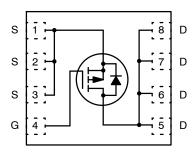
FDMC 86265P

&Z &K

Specific Device CodeSpecific Device CodeAssembly Location

Lot Run Traceability Code
 Date Code (Year and Week)

PIN ASSIGNMENT



P-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

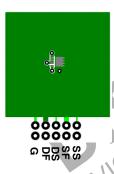
Symbol	Parameter			Rating	Unit
V _{DS}	Drain to Source Voltage			-150	V
V _{GS}	Gate to Source Voltage			±25	V
I _D	Drain Current	Continuous (Note 5)	T _C = 25°C	-2.6	Α
		Continuous (Note 5)	T _C = 100°C	-1.65	
		Continuous (Note 1a)	T _A = 25°C	-1	
		Pulsed (Note 4)	_	-9	
E _{AS}	Single Pulse Avalanche Energy (Note 3)			6	mJ
P_{D}	Power Dissipation $T_C = 25^{\circ}C$			16	W
	Power Dissipation (Note 1a) T _A = 25°C			2.3	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to + 150	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	N	Rating	Unit
Rejc	Thermal Resistance, Junction to Case	NE	7.5	°C/W
RθJA	Thermal Resistance, Junction to Ambient (Note 1a)	JOK N	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in² pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%. 3. Starting T_J = 25°C; P-ch: L = 3 mH, I_{AS} = -2 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% test al L = 0.1 mH, I_{AS} = -9 A. 4. Pulsed Id please refer to Figure 11 and Figure 24 SOA graph for more details.
- 5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARA	ACTERISTICS					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-150	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25°C	-	-125	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -120 \text{ V}, V_{GS} = 0 \text{ V}$	_	-	-1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	_	-	±100	nA
ON CHARA	CTERISTICS					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-2	-3.2	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25°C	-	5	-	mV/°C
r _{DS(on)}	Static Drain to Source	V _{GS} = -10 V, I _D = -1 A		0.86	1.2	Ω
	On Resistance	$V_{GS} = -6 \text{ V}, I_D = -0.9 \text{ A}$		0.95	1.4	
		V _{GS} = -10 V, I _D = -1 A, T _J = 125°C	7-	1.53	2.2	
9FS	Forward Transconductance	$V_{DS} = -10 \text{ V}, I_D = -1 \text{ A}$	1	1.9	_	S
DYNAMIC C	HARACTERISTICS		Nr.			
C _{iss}	Input Capacitance	$V_{DS} = -75 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	105	158	210	pF
C _{oss}	Output Capacitance		50-X	16	25	pF
C _{rss}	Reverse Transfer Capacitance	JOE OF	17/2	0.7	5	pF
Rg	Gate Resistance	WELD THE OLD	0.1	3	7.5	Ω
SWITCHING	CHARACTERISTICS	May 10 Me				
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -75 \text{ V}, I_D = -1 \text{ A}, V_{GS} = -10 \text{ V},$	_	5.8	12	ns
t _r	Rise Time	$R_{GEN} = 6 \Omega$	_	2.2	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{DD} = 73 \text{ V}_{DD} = -1 \text{ A}, V_{GS} = -10 \text{ V},$ $R_{GEN} = 6 \Omega$	_	8	16	ns
t _f	Fall Time	E	_	6.4	13	ns
Q _{g(TOT)}	Total Gate Charge	$V_{DD} = -75 \text{ V}, I_D = -1 \text{ A}, V_{GS} = 0 \text{ V to } -10 \text{ V}$	_	2.8	4	nC
Q_{gs}	Total Gate Charge	V _{DD} = -75 V, I _D = -1 A	_	0.8	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	,	_	0.7	-	nC
DRAIN-SOL	JRCE DIODE CHARACTERISTICS					
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1 \text{ A} \text{ (Note 2)}$	_	-0.87	-1.3	V
t _{rr}	Reverse Recovery Time	I _F = -1 A, di/dt = 100 A/μs		50	80	ns
Q _{rr}	Reverse Recovery Charge		_	78	124	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

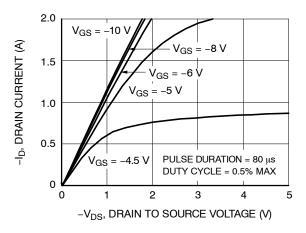


Figure 1. On Region Characteristics

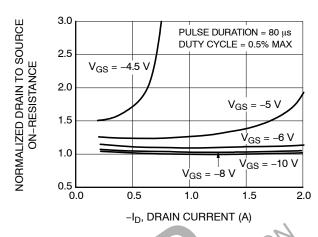


Figure 2. Normalized On–Resistance vs.

Drain Current and Gate Voltage

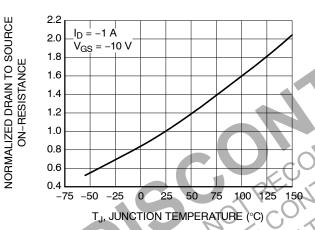


Figure 3. Normalized On Resistance vs. Junction Temperature

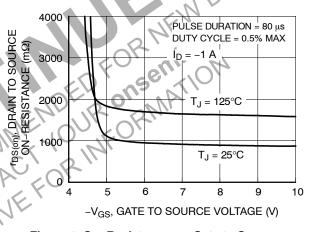


Figure 4. On-Resistance vs. Gate to Source Voltage

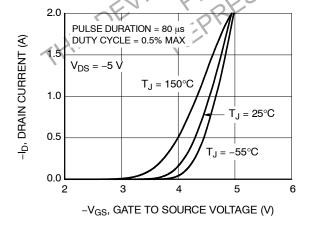


Figure 5. Transfer Characteristics

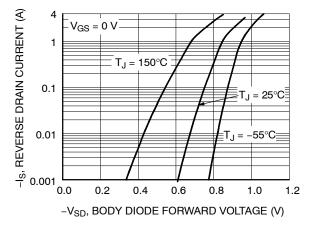


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

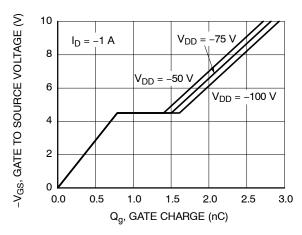


Figure 7. Gate Charge Characteristics

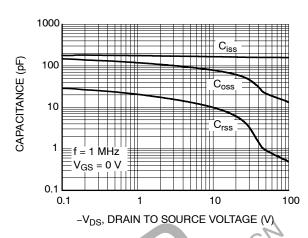


Figure 8. Capacitance vs. Drain to Source Voltage

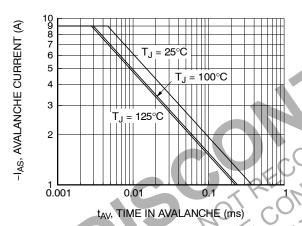


Figure 9. Unclamped Inductive Switching Capability

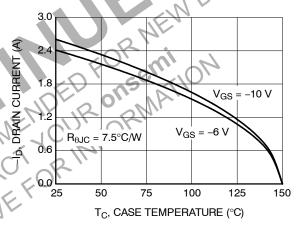


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

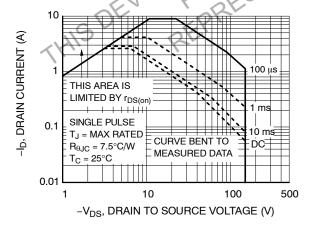


Figure 11. Forward Bias Safe Operating Area

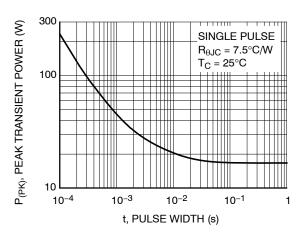


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_{.1} = 25°C unless otherwise noted) (continued)

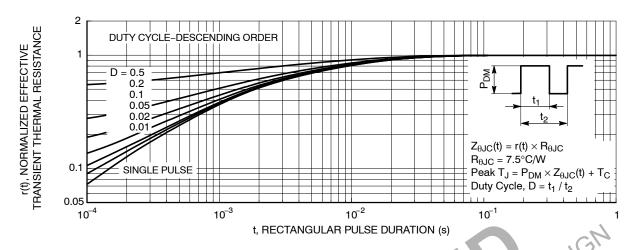


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device Device Marking	Package Type	Shipping [†]
DMC86265P FDMC86265P	WDFN8 3.3x3.3, 0.65P (Pb-Free)	3000 / Tape & Reel
For information on tape and reel specifications, including part oriental especifications Brochure, BRD8011/D.	ion and tape sizes, please refe	r to our Tape and Reel Packaging

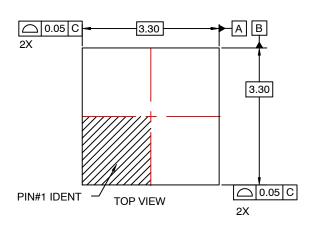
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

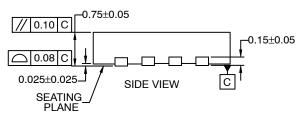
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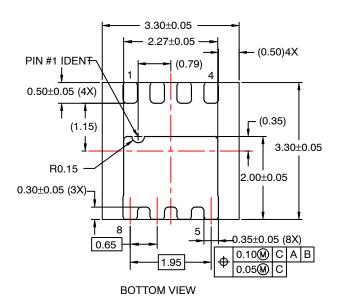


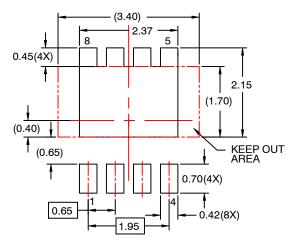
WDFN8 3.3x3.3, 0.65P CASE 511DH ISSUE O

DATE 31 JUL 2016









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P		PAGE 1 OF 1		

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