

MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

100 V, 18 A, 23 mΩ

FDMC86102L

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 23 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 7\text{ A}$
- Max $R_{DS(on)}$ = 34 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 5.5\text{ A}$
- Low Profile – 1 mm Max in Power 33
- Pb-Free, Halide Free and RoHS Compliant

Applications

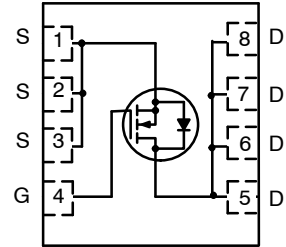
- DC-DC Conversion

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

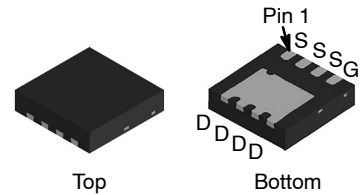
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current:		A
	Continuous, $T_C = 25^\circ\text{C}$	18	
	Continuous, $T_A = 25^\circ\text{C}$ (Note 1a)	7	
	Pulsed	30	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	63	mJ
P_D	Power Dissipation:		W
	$T_C = 25^\circ\text{C}$	41	
	$T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
100 V	23 mΩ @ 10 V	18 A
	34 mΩ @ 4.5 V	

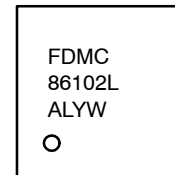


N-CHANNEL MOSFET



WDFN8 3.3 x 3.3, 0.65P
CASE 511DH

MARKING DIAGRAM



FDMC86102L = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
FDMC86102L	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}$	100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	–	71	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{V}, V_{GS} = 0 \text{V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{V}, V_{DS} = 0 \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1	1.8	3	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	–	–6	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{V}, I_D = 7 \text{A}$	–	18.9	23	m Ω
		$V_{GS} = 4.5 \text{V}, I_D = 5.5 \text{A}$	–	24.9	34	
		$V_{GS} = 10 \text{V}, I_D = 7 \text{A}, T_J = 125^\circ\text{C}$	–	31.9	39	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{V}, I_D = 7 \text{A}$	–	26	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{V}, V_{GS} = 0 \text{V}, f = 1 \text{MHz}$	–	999	1330	pF
C_{oss}	Output Capacitance		–	178	240	pF
C_{rss}	Reverse Transfer Capacitance		–	7.6	15	pF
R_g	Gate Resistance		–	0.5	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{V}, I_D = 7 \text{A}, V_{GS} = 10 \text{V}, R_{GEN} = 6 \Omega$	–	7.7	16	ns
t_r	Rise Time		–	2.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	19	34	ns
t_f	Fall Time		–	2.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{V to } 10 \text{V}, V_{DD} = 50 \text{V}, I_D = 7 \text{A}$	–	15	22	nC
		$V_{GS} = 0 \text{V to } 4.5 \text{V}, V_{DD} = 50 \text{V}, I_D = 7 \text{A}$	–	7.3	11	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 50 \text{V}, I_D = 7 \text{A}$	–	2.7	–	nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{DD} = 50 \text{V}, I_D = 7 \text{A}$	–	2.3	–	nC

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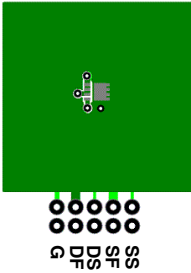
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 7\text{ A}$ (Note 2)	–	0.81	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	–	0.74	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	–	45	72	ns
Q_{rr}	Reverse Recovery Charge		–	45	72	nC

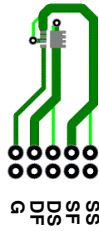
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



- b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- Starting $T_J = 25^\circ\text{C}$; N-ch: $L = 1\text{ mH}$, $I_{AS} = 11.3\text{ A}$, $V_{DD} = 90\text{ V}$, $V_{GS} = 10\text{ V}$.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

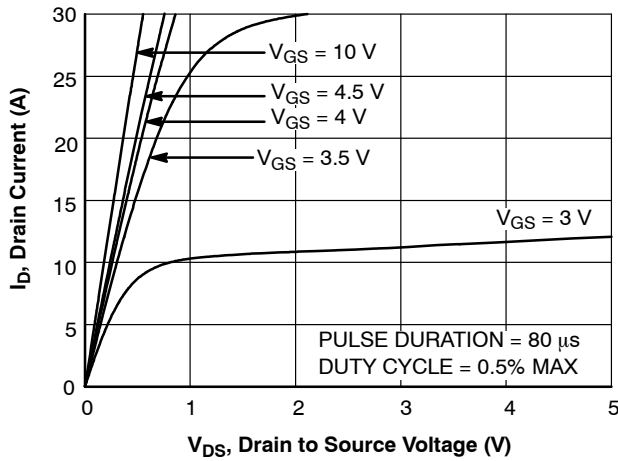


Figure 1. On-Region Characteristics

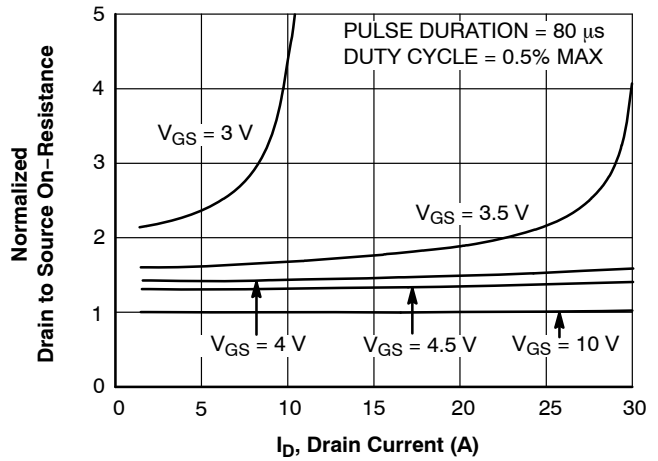


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

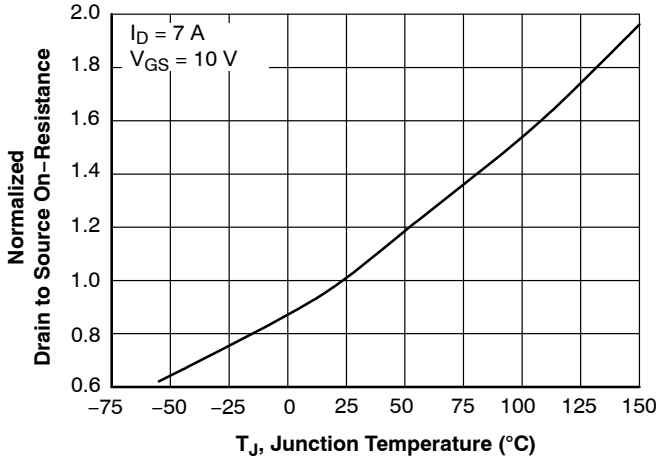


Figure 3. Normalized On-Resistance vs. Junction Temperature

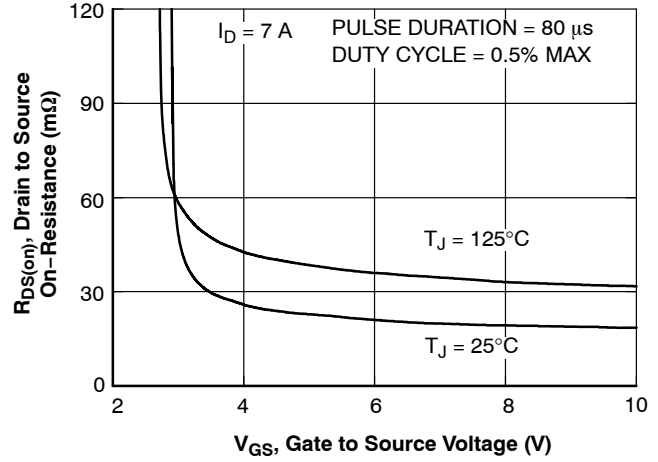


Figure 4. On-Resistance vs. Gate to Source Voltage

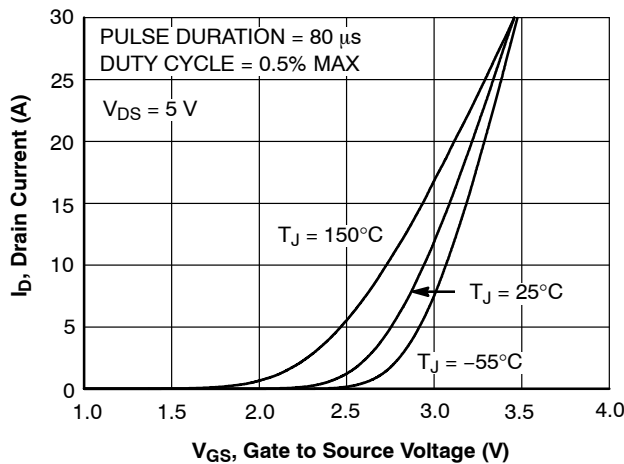


Figure 5. Transfer Characteristics

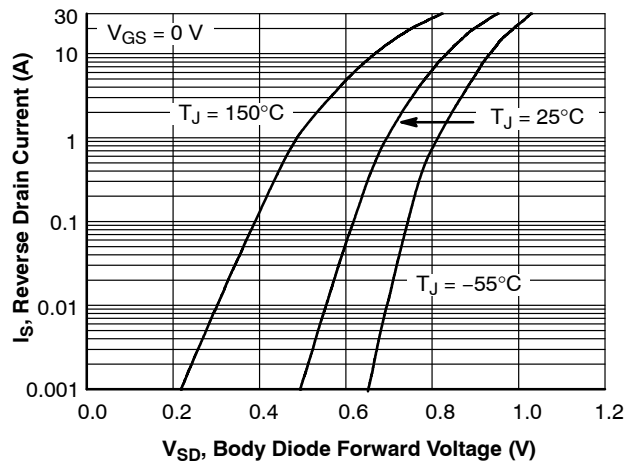


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

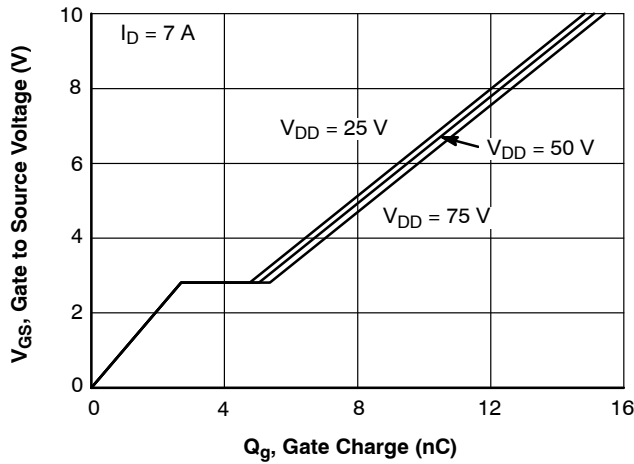


Figure 7. Gate Charge Characteristics

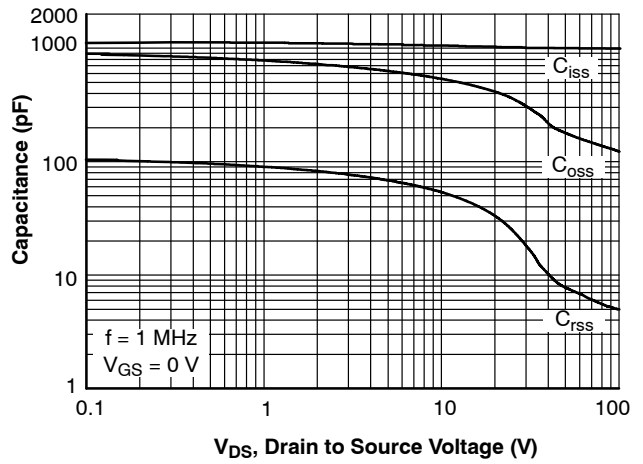


Figure 8. Capacitance vs. Drain to Source Voltage

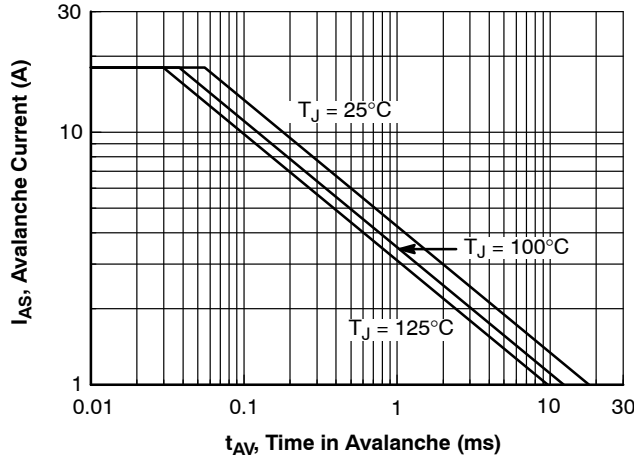


Figure 9. Unclamped Inductive Switching Capability

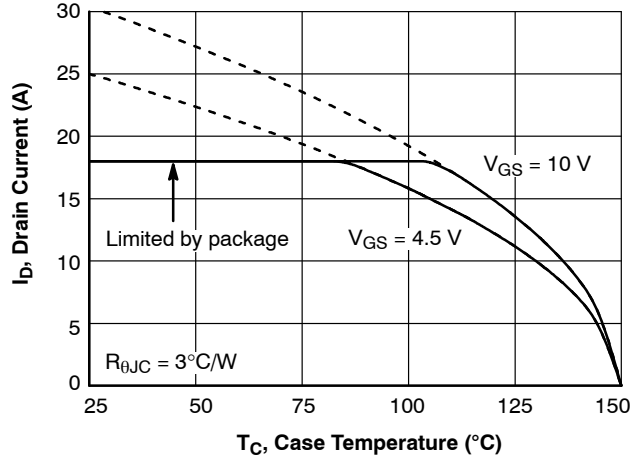


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

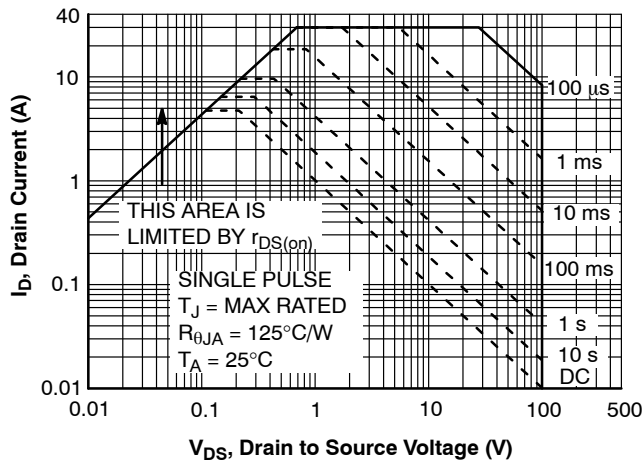


Figure 11. Forward Bias Safe Operating Area

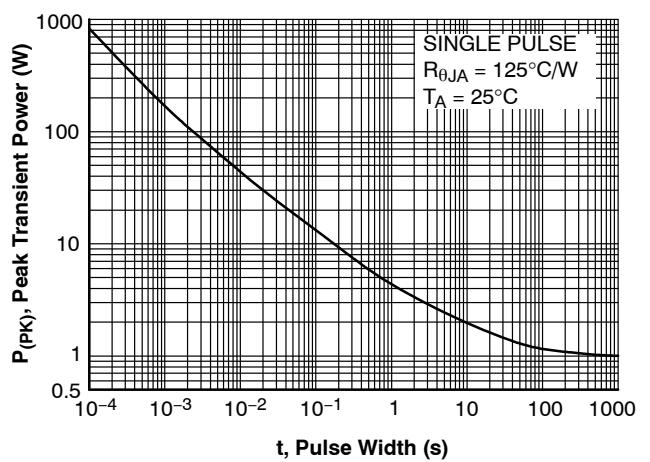


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

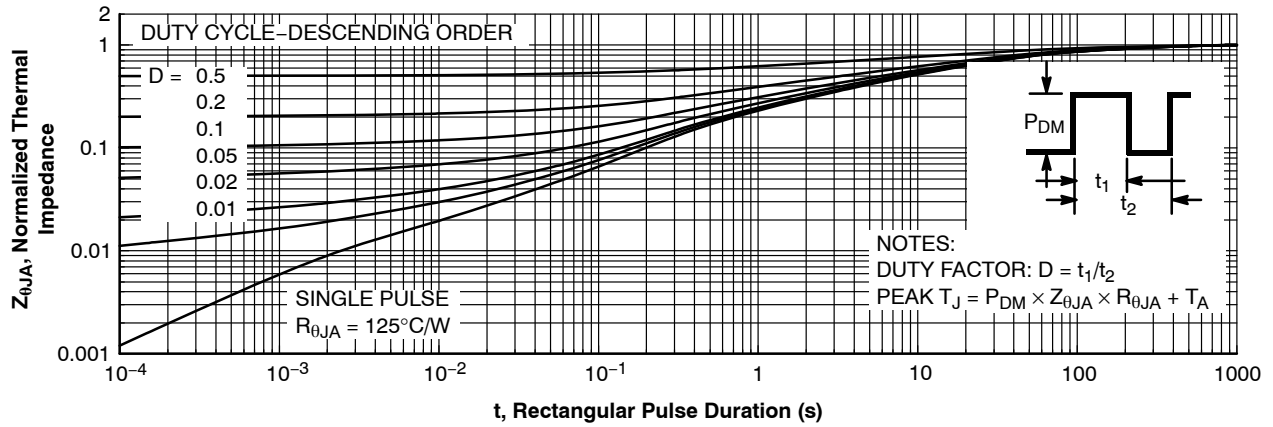


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

MECHANICAL CASE OUTLINE

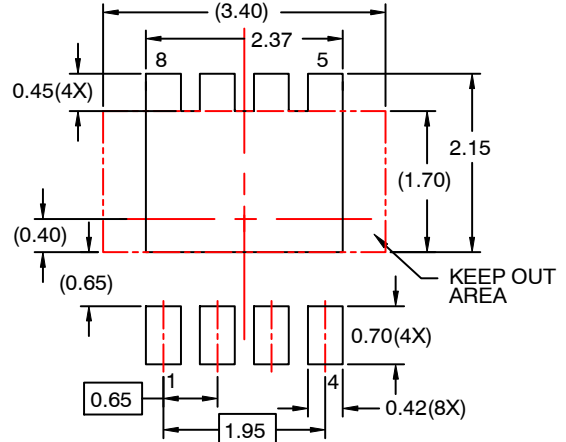
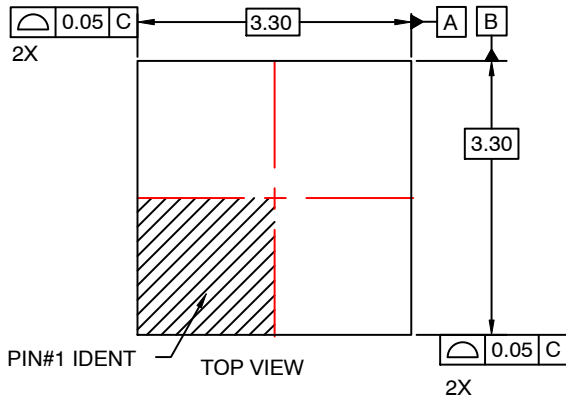
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

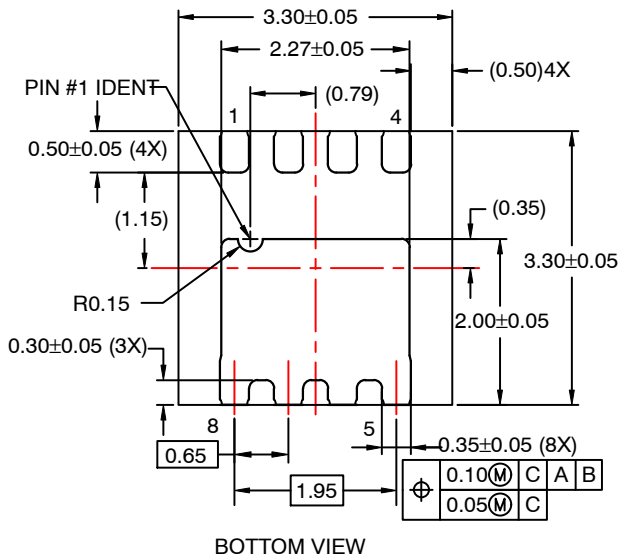
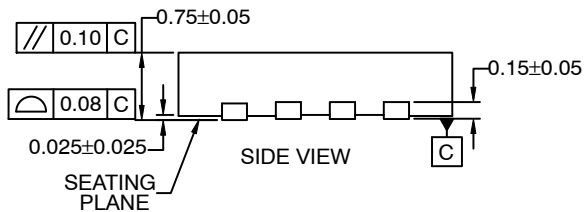
DATE 31 JUL 2016



RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW

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