

# MOSFET – N-Channel, POWERTRENCH®

**30 V, 88 A, 2.7 mΩ**

## FDMC86012

### General Description

This device has been designed specifically to improve the efficiency of DC/DC converters. Using new techniques in MOSFET construction, the various components of gate charge and capacitance have been optimized to reduce switching losses. Low gate resistance and very low Miller charge enable excellent performance with both adaptive and fixed dead time gate drive circuits. Very low  $r_{DS(on)}$  has been maintained to provide a sub logic-level device.

### Features

- Max  $R_{DS(on)}$  = 2.7 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 23$  A
- Max  $R_{DS(on)}$  = 4.7 mΩ at  $V_{GS} = 2.5$  V,  $I_D = 17.5$  A
- High Performance Technology for Extremely low  $R_{DS(on)}$
- Termination is Lead-free
- 100% UIL Tested
- Pb-Free, Halide Free and RoHS Compliant

### Applications

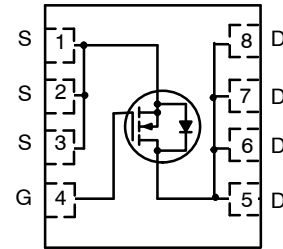
- 3.3 V Input Synchronous Buck Switch
- Synchronous Rectifier

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

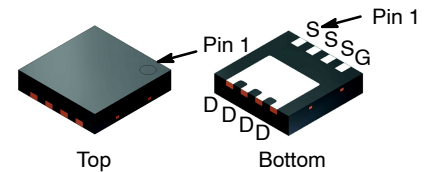
Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_D$	Drain Current: Continuous, $T_C = 25^\circ\text{C}$ Continuous, $T_A = 25^\circ\text{C}$ (Note 1a) Pulsed (Note 4)	88 23 230	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	337	mJ
$P_D$	Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	54 2.3	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	2.7 mΩ @ 4.5 V	88 A
	4.7 mΩ @ 2.5 V	

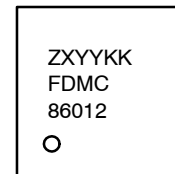


N-CHANNEL MOSFET



WDFN8 3.3 × 3.3, 0.65P  
CASE 483AW

### MARKING DIAGRAM



- Z = Assembly Plant Code
- XYY = 3-Digit Date Code Format
- KK = 2-Alphanumeric Lot Run Traceability Code
- FDMC86012 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
FDMC86012	WDFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMC86012

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	30	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	–	43	–	mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	0.8	1.0	1.5	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	–	–4	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 23 \text{ A}$	–	2.2	2.7	m $\Omega$
		$V_{GS} = 2.5 \text{ V}, I_D = 17.5 \text{ A}$	–	3.4	4.7	
		$V_{GS} = 4.5 \text{ V}, I_D = 23 \text{ A}, T_J = 125^\circ\text{C}$	–	3.5	4.3	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 23 \text{ A}$	–	144	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	–	3625	5075	pF
$C_{oss}$	Output Capacitance		–	1230	1725	pF
$C_{rss}$	Reverse Transfer Capacitance		–	185	260	pF
$R_g$	Gate Resistance		0.1	0.9	3.0	$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, I_D = 23 \text{ A}, V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$	–	20	32	ns
$t_r$	Rise Time		–	11	20	ns
$t_{d(off)}$	Turn-Off Delay Time		–	43	69	ns
$t_f$	Fall Time		–	8	16	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}, V_{DD} = 15 \text{ V}, I_D = 23 \text{ A}$	–	27	38	nC
		$V_{GS} = 0 \text{ V to } 2.5 \text{ V}, V_{DD} = 15 \text{ V}, I_D = 23 \text{ A}$	–	16	23	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 15 \text{ V}, I_D = 23 \text{ A}$	–	5.8	–	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$V_{DD} = 15 \text{ V}, I_D = 23 \text{ A}$	–	5.4	–	nC

# FDMC86012

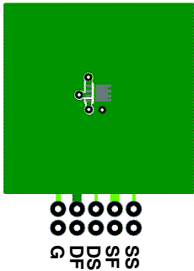
## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 23\text{ A}$ (Note 2)	–	0.8	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 1.9\text{ A}$ (Note 2)	–	0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 23\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	–	40	64	ns
$Q_{rr}$	Reverse Recovery Charge		–	23	37	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**NOTES:**

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- $E_{AS}$  of 337 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 3\text{ mH}, I_{AS} = 15\text{ A}, V_{DD} = 30\text{ V}, V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}, I_{AS} = 33\text{ A}$ .
- Pulsed  $I_d$  limited by junction temperature,  $t_d \leq 100\ \mu\text{s}$ , please refer to SOA curve for more details.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

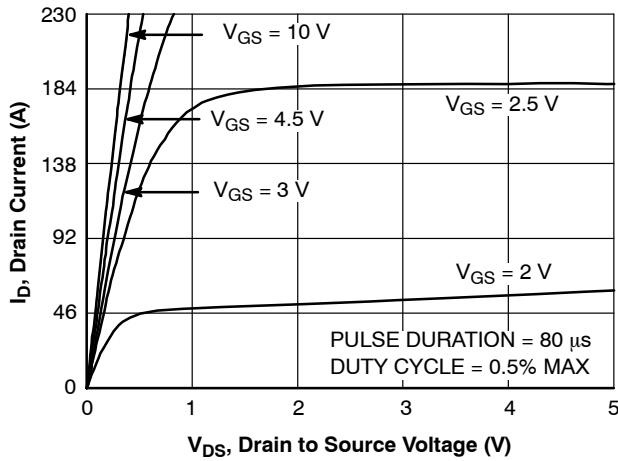


Figure 1. On-Region Characteristics

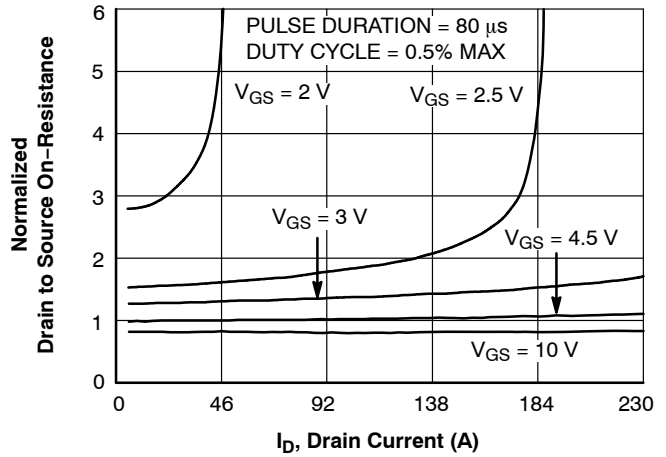


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

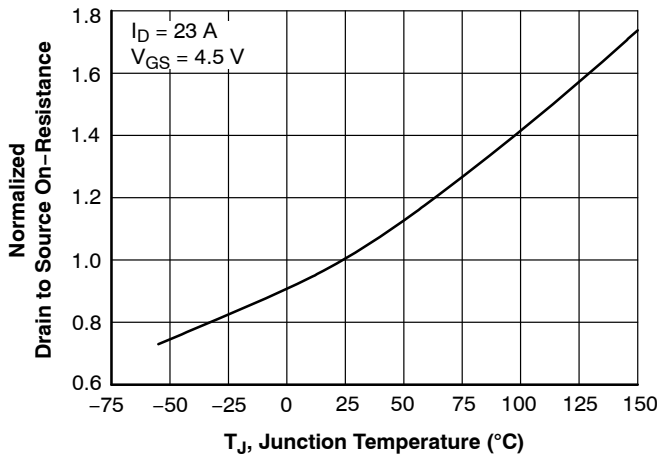


Figure 3. Normalized On-Resistance vs. Junction Temperature

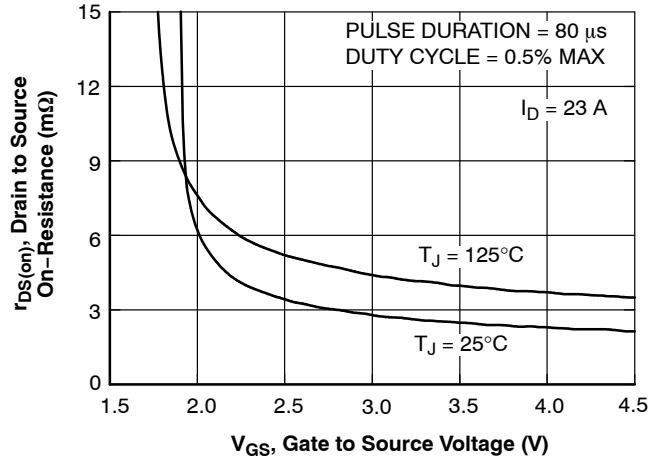


Figure 4. On-Resistance vs. Gate to Source Voltage

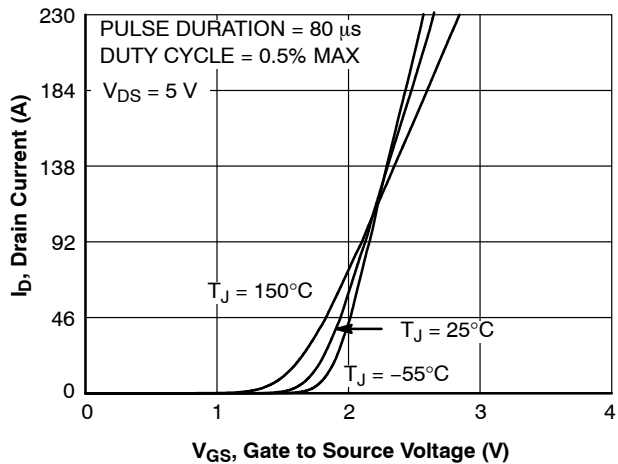


Figure 5. Transfer Characteristics

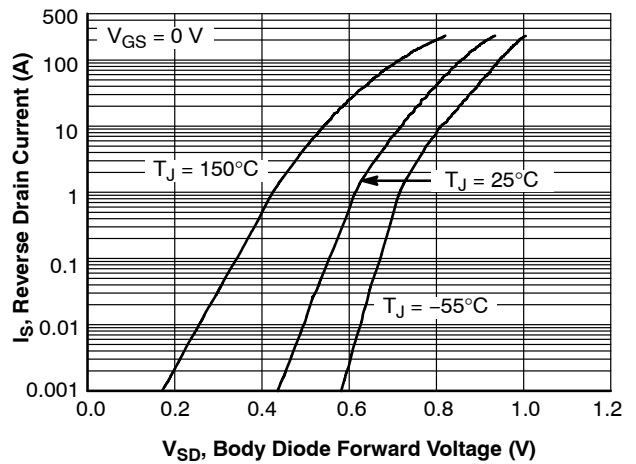


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

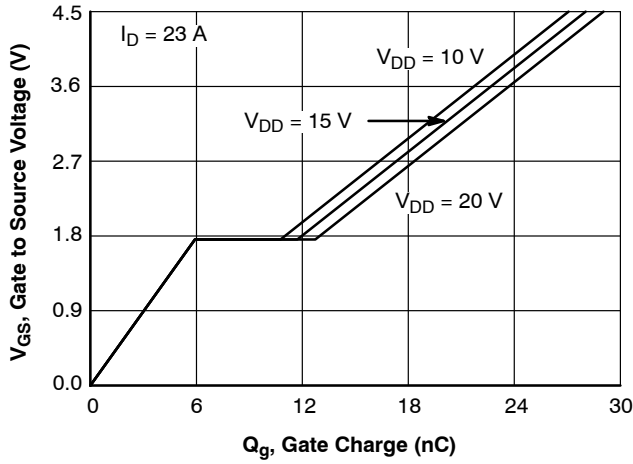


Figure 7. Gate Charge Characteristics

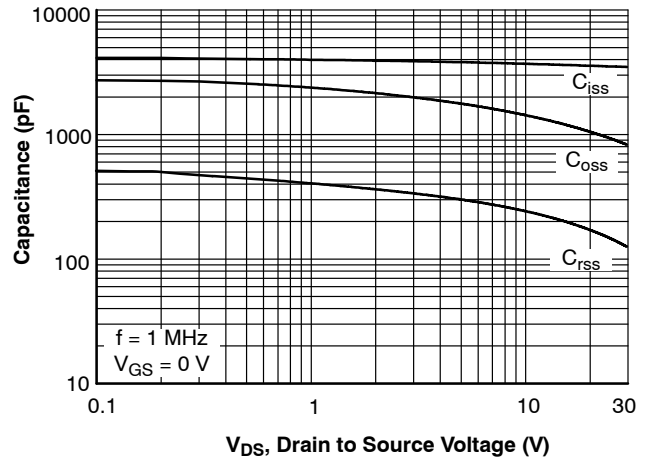


Figure 8. Capacitance vs. Drain to Source Voltage

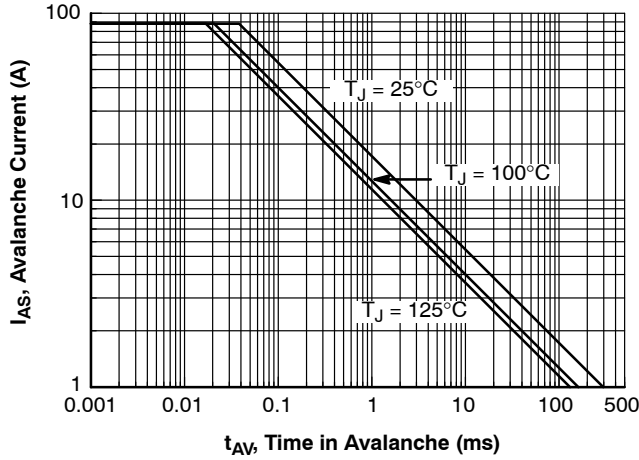


Figure 9. Unclamped Inductive Switching Capability

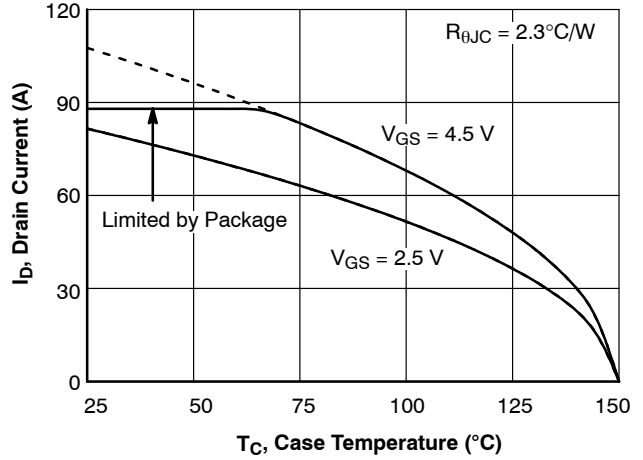


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

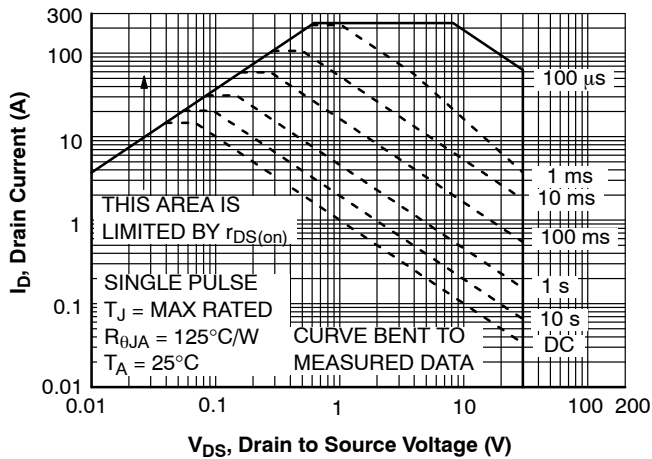


Figure 11. Forward Bias Safe Operating Area

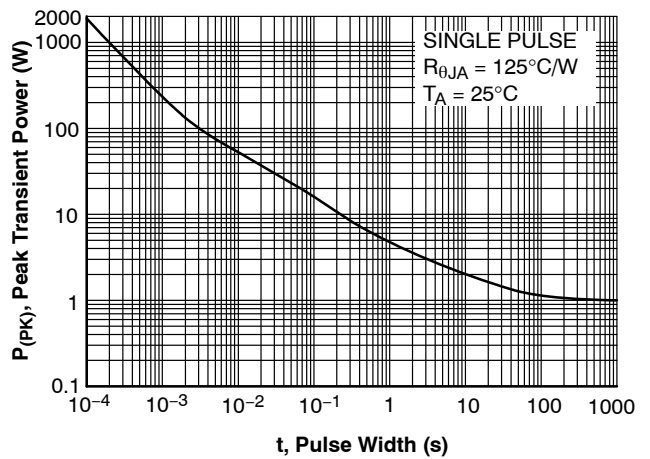


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

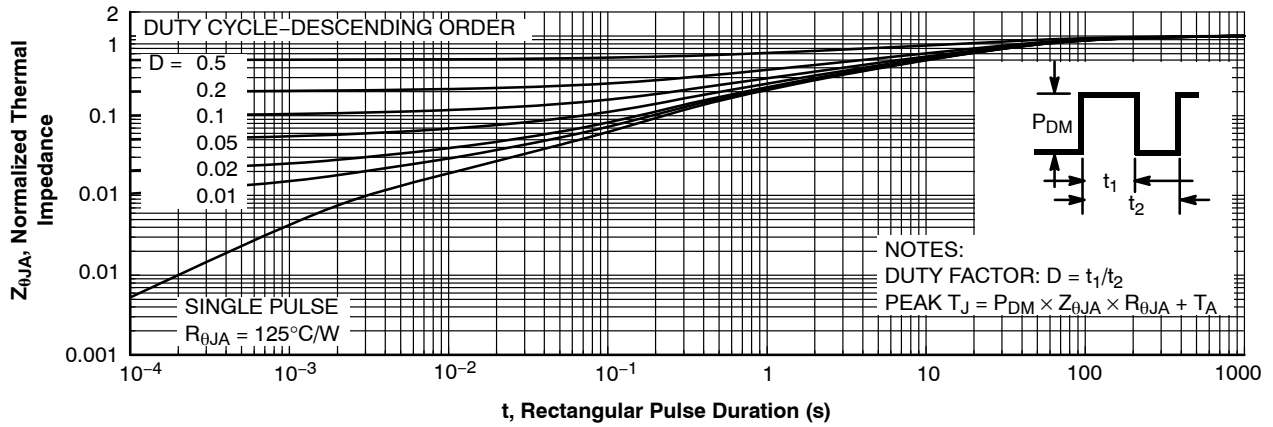
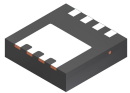


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

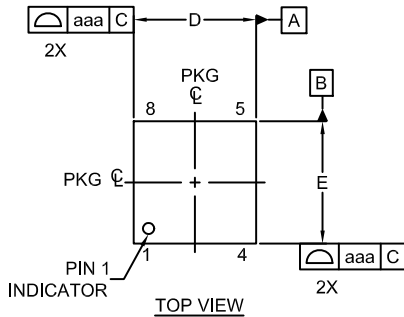
## PACKAGE DIMENSIONS

ON Semiconductor®

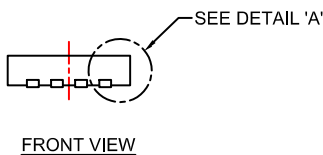


**WDFN8 3.3X3.3, 0.65P**  
**CASE 483AW**  
**ISSUE A**

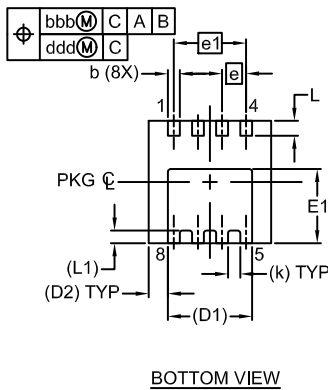
DATE 10 SEP 2019



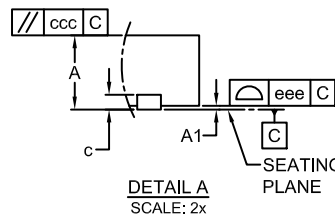
TOP VIEW



FRONT VIEW

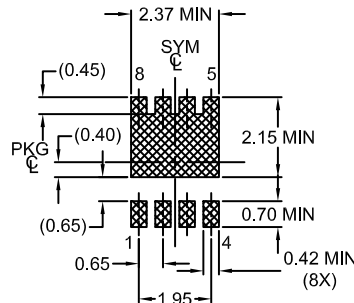


BOTTOM VIEW



DETAIL A  
SCALE: 2x

### LAND PATTERN RECOMMENDATION\*



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	-	0.05
b	0.27	0.32	0.37
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.27 REF		
D2	0.52 REF		
E	3.20	3.30	3.40
E1	1.85	1.95	2.05
e	0.65 BSC		
e1	1.95 BSC		
k	0.33 REF		
L	0.30	0.40	0.50
L1	0.34 REF		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

<b>DOCUMENT NUMBER:</b>	<b>98AON13672G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WDFN8 3.3X3.3, 0.65P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative