

# MOSFET – N-Channel, POWERTRENCH®

**30 V, 13.3 A, 8.5 mΩ**

**FDMC7692**

## General Description

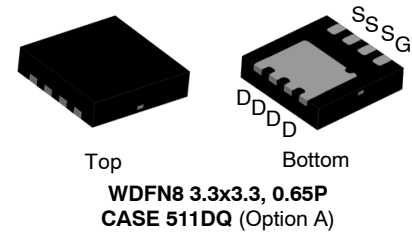
This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

## Features

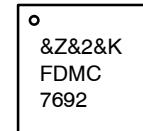
- Max  $r_{DS(on)}$  = 8.5 mΩ at  $V_{GS} = 10$  V,  $I_D = 13.3$  A
- Max  $r_{DS(on)}$  = 11.5 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 10.6$  A
- High Performance Technology for Extremely Low  $r_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

## Applications

- DC – DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook

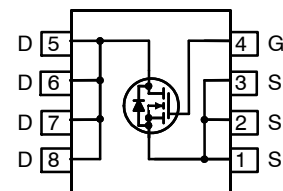


## MARKING DIAGRAM



&Z = Assembly Plant Code  
 &2 = 2-Digit Date Code  
 &K = 2-Digit Lot Code  
 FDMC7692 = Device Code

## PIN ASSIGNMENT



## ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

**MOSFET MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

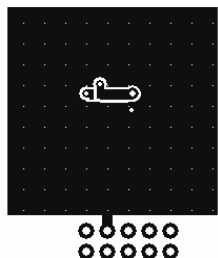
Symbol	Parameter			Rating	Unit
$V_{DS}$	Drain to Source Voltage			30	V
$V_{GS}$	Gate to Source Voltage			$\pm 20$	V
$I_D$	Drain Current	Continuous (Package limited)	$T_C = 25^\circ\text{C}$	16	A
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	13.3	
		Pulsed		40	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)			58	mJ
$P_D$	Power Dissipation		$T_C = 25^\circ\text{C}$	29	W
	Power Dissipation (Note 1a)		$T_A = 25^\circ\text{C}$	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range			$-55$ to $150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS**

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a.  $53^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



- b.  $125^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2.  $E_{AS}$  of 58 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 1$  mH,  $I_{AS} = 10.8$  A,  $V_{DD} = 27$  V,  $V_{GS} = 10$  V. 100% test at  $L = 0.1$  mH,  $I_{AS} = 21$  A.

# FDMC7692

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	30	–	–	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	16	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	–	–	1	μA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C	–	–	250	
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	–	–	100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.2	1.9	3.0	V
ΔV <sub>GS(th)</sub> / ΔT <sub>J</sub>	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	–6	–	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.3 A	–	7.2	8.5	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10.6 A	–	9.5	11.5	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 13.3 A, T <sub>J</sub> = 125°C	–	9.5	12.0	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 5 V, I <sub>D</sub> = 13.3 A	–	60	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	1260	1680	pF
C <sub>oss</sub>	Output Capacitance		–	480	635	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	65	100	pF
R <sub>g</sub>	Gate Resistance	f = 1 MHz	–	0.9	2.4	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 13.3 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	9	18	ns
t <sub>r</sub>	Rise Time		–	4	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	21	33	ns
t <sub>f</sub>	Fall Time		–	3	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 13.3 A	–	21	29	nC
		V <sub>GS</sub> = 0 V to 4.5 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 13.3 A	–	10	14	nC
Q <sub>gs</sub>	Total Gate Charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 13.3 A	–	5	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge		–	3	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 13.3 A (Note 3)	–	0.86	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.9 A (Note 3)	–	0.75	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 13.3 A, di/dt = 100 A/μs	–	24	38	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	7	14	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

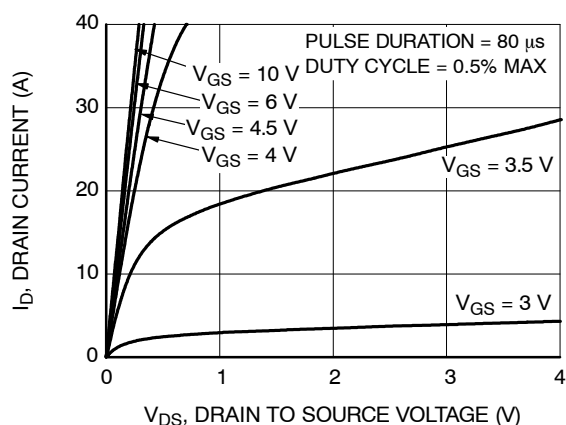
TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Figure 1. On Region Characteristics

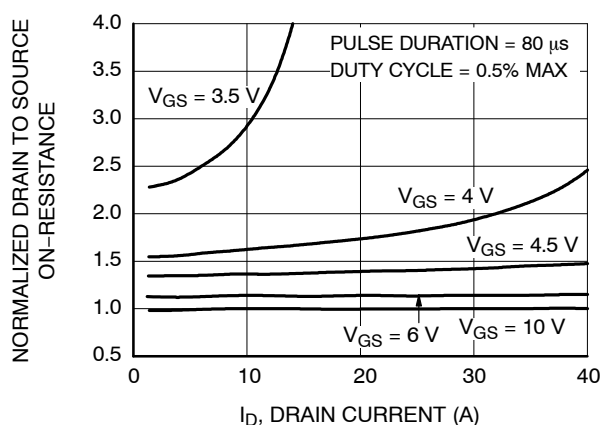


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

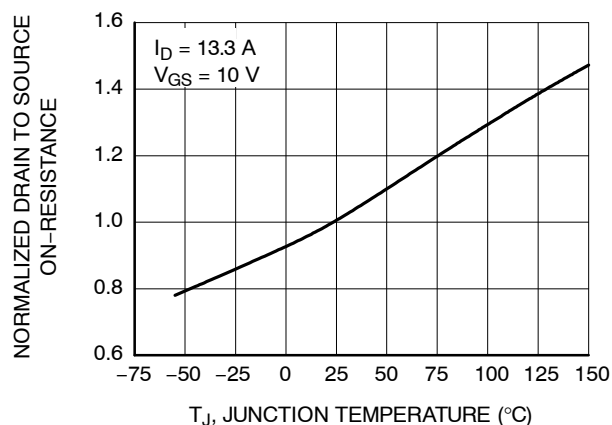


Figure 3. Normalized On Resistance vs. Junction Temperature

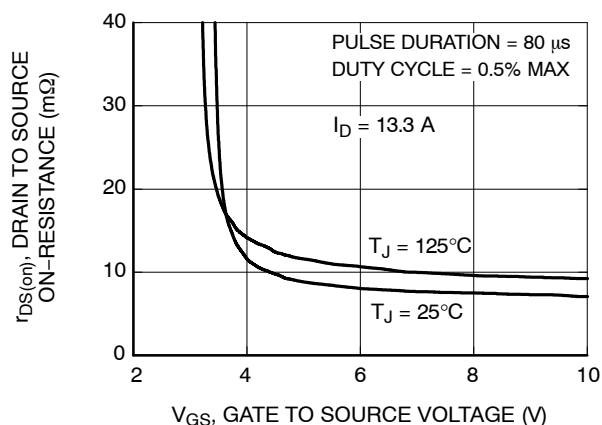


Figure 4. On-Resistance vs. Gate to Source Voltage

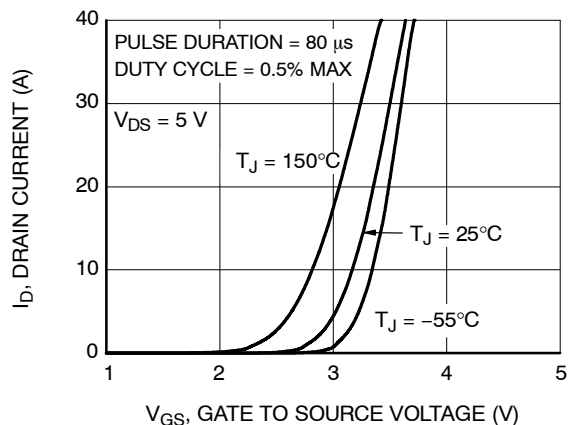


Figure 5. Transfer Characteristics

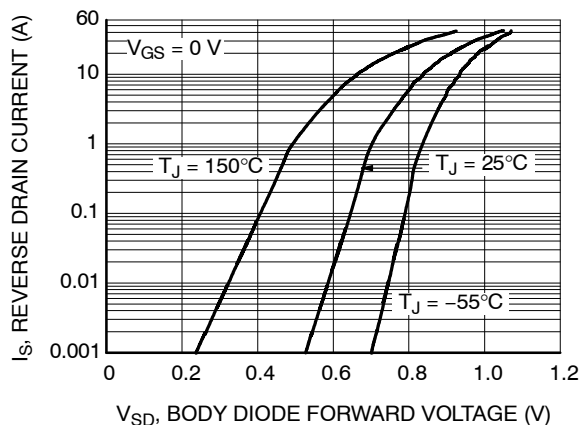


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

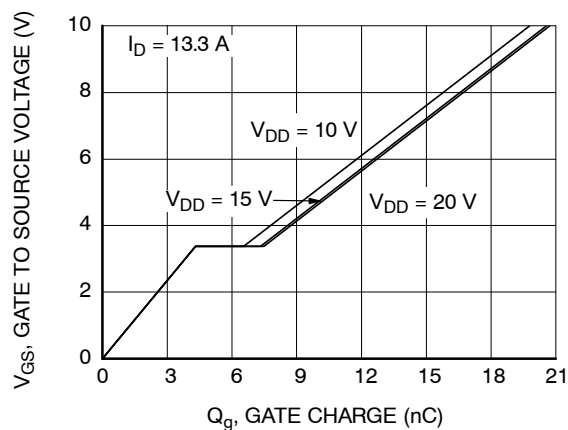
TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

Figure 7. Gate Charge Characteristics

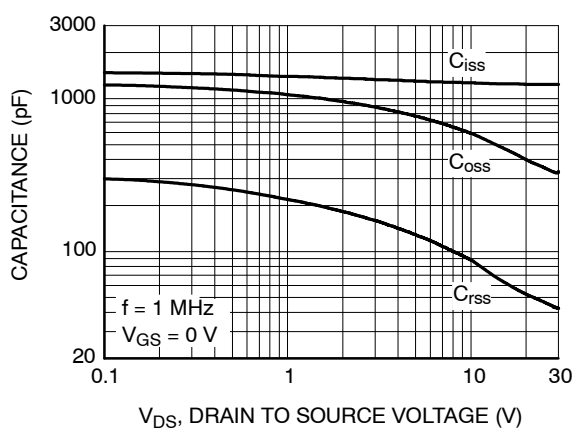


Figure 8. Capacitance vs. Drain to Source Voltage

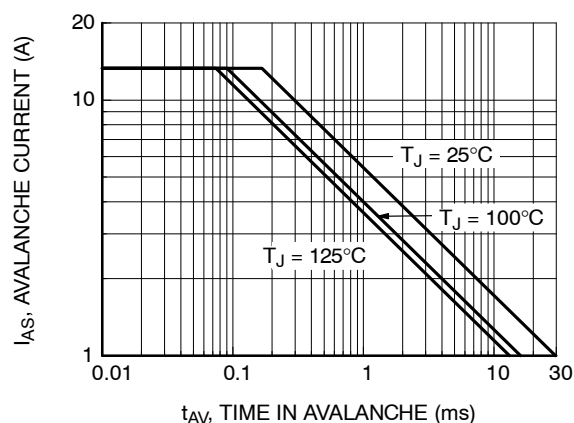


Figure 9. Unclamped Inductive Switching Capability

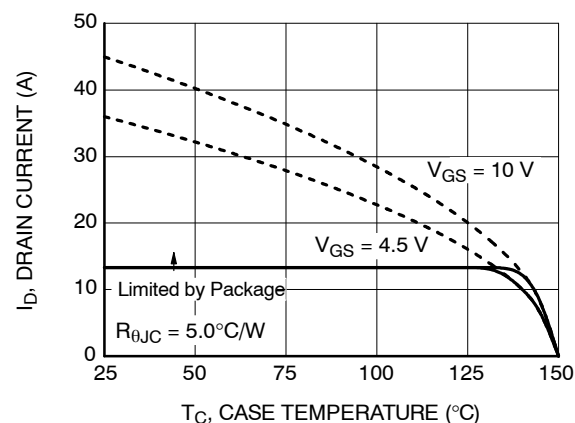


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

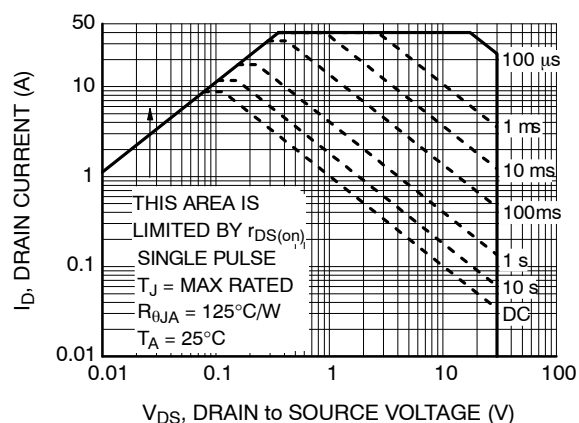


Figure 11. Forward Bias Safe Operating Area

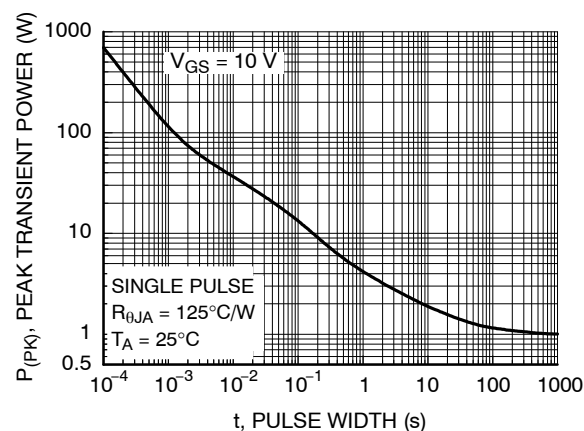


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

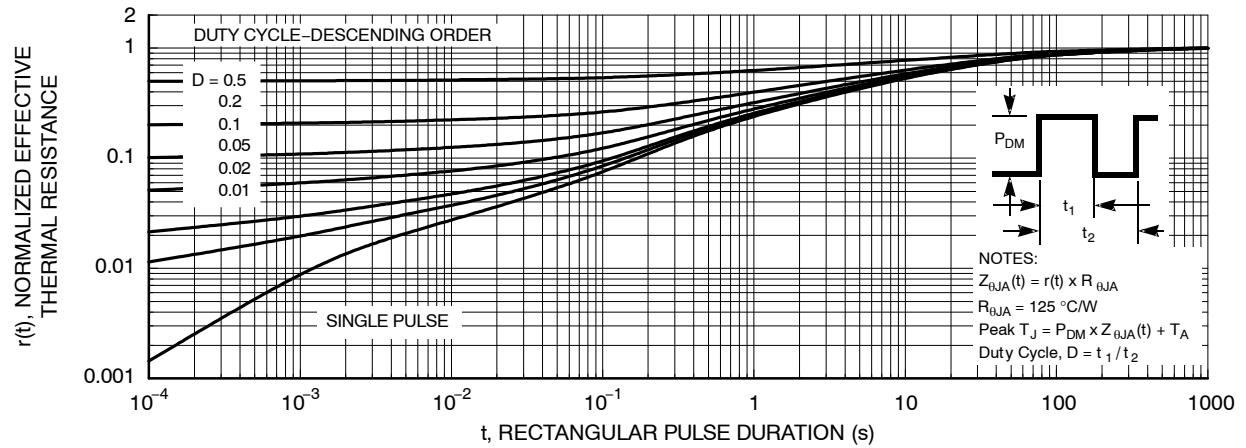


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

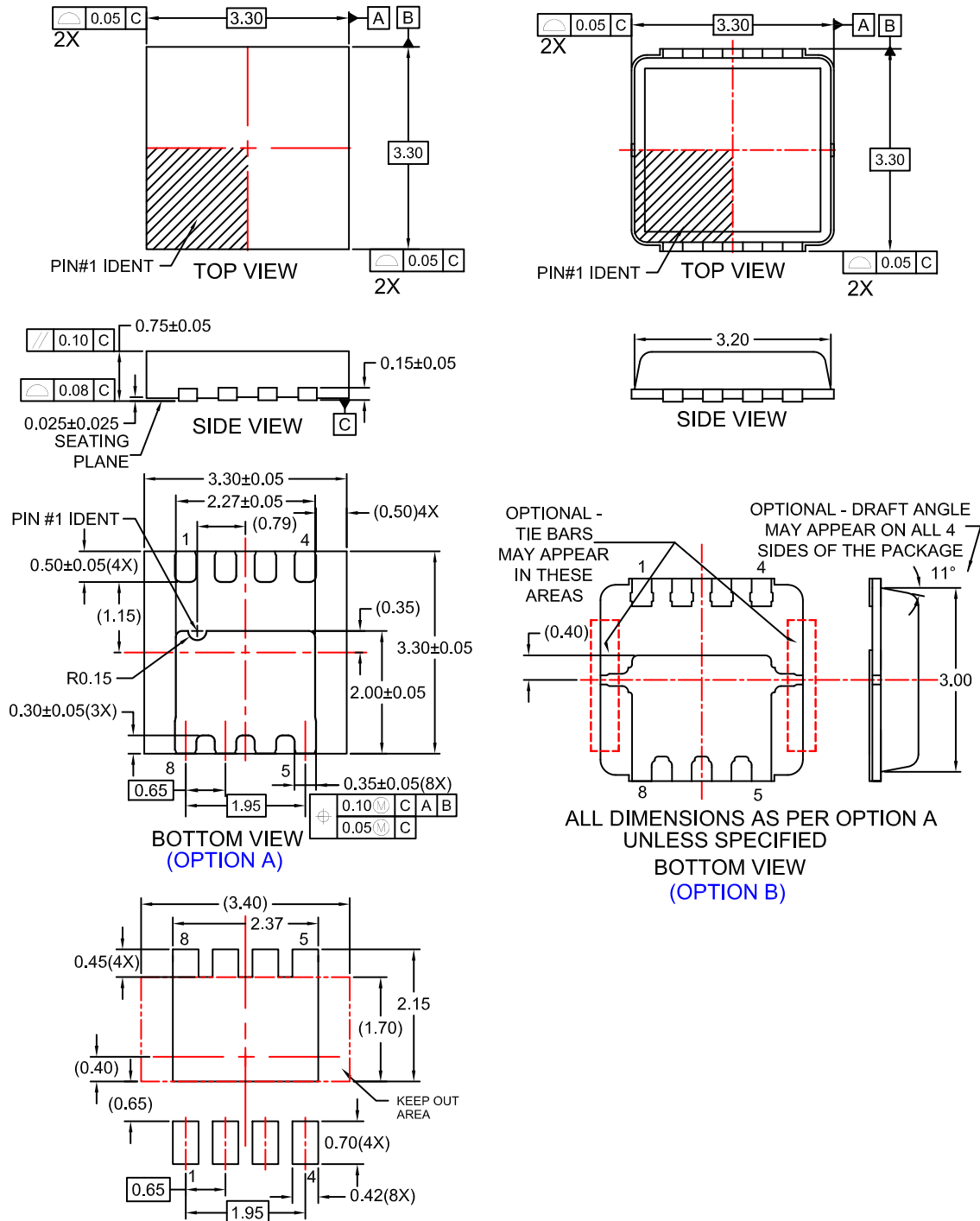
ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping <sup>†</sup>
FDMC7692	FDMC7692	WDFN8 3.3x3.3, 0.65P case 511DQ (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**WDFN8 3.3x3.3, 0.65P**  
**CASE 511DQ**  
**ISSUE O**

DATE 31 OCT 2016



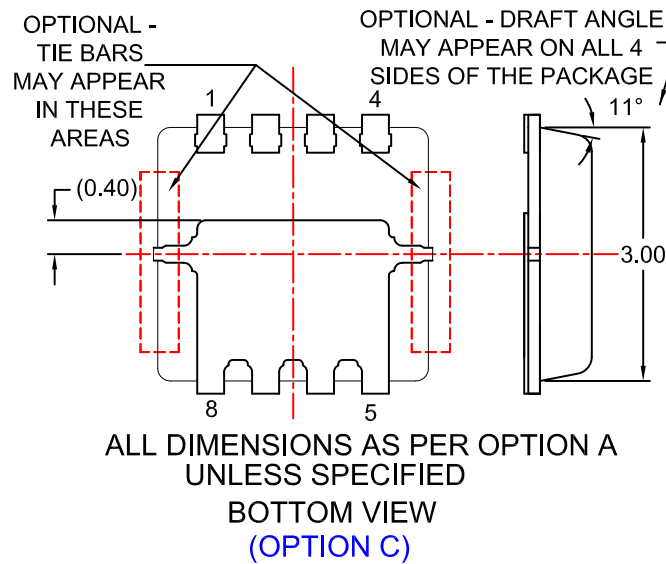
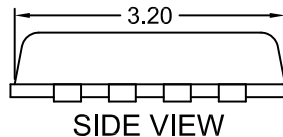
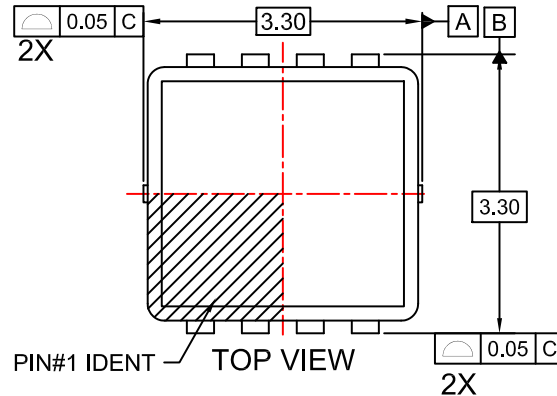
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ISSUE O

DATE 31 OCT 2016



**NOTES:**

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
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