

MOSFET – Dual N-Channel, POWERTRENCH®

Q1: 30 V, 12 A, 9.0 mΩ

Q2: 30 V, 16 A, 6.4 mΩ

FDMC7208S

General Description

This device includes two 30 V N-Channel MOSFETs in a dual Power 33 (3 mm x 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

Features

Q1: N-Channel

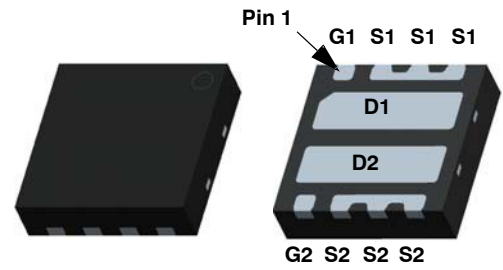
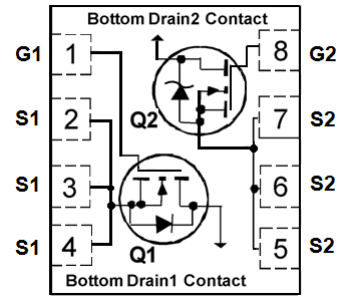
- Max $r_{DS(on)}$ = 9.0 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}$
- Max $r_{DS(on)}$ = 11.0 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 11\text{ A}$

Q2: N-Channel

- Max $r_{DS(on)}$ = 6.4 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 16\text{ A}$
- Max $r_{DS(on)}$ = 7.5 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 13.5\text{ A}$
- This Device is Pb-Free and is RoHS Compliant

Applications

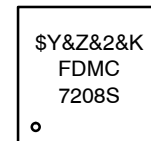
- Computing
- Communications
- General Purpose Point of Load
- Notebook System



Power 33

WDFN8 3x3, 0.65P
CASE 511DG

MARKING DIAGRAM



- | | |
|-----------|------------------------|
| \$Y | = onsemi Logo |
| &Z | = Assembly Plant Code |
| &2 | = Numeric Date Code |
| &K | = Lot Code |
| FDMC7208S | = Specific Device Code |

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMC7208S

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Rating		Value		Unit	
			Q1	Q2		
V_{DS}	Drain to Source Voltage		30	30	V	
V_{GS}	Gate to Source Voltage (Note 4)		± 20	± 12	V	
I_D	Drain Current	Continuous (Package limited) $T_C = 25^\circ\text{C}$	22	26	A	
		Continuous $T_A = 25^\circ\text{C}$	12 (Note 1a)	16 (Note 1b)		
		Pulsed	60	80		
E_{AS}	Single Pulse Avalanche Energy (Note 3)		21	21	mJ	
P_D	Power Dissipation for Single Operation		$T_A = 25^\circ\text{C}$	1.9 (Note 1a)	1.9 (Note 1b)	W
			$T_A = 25^\circ\text{C}$	0.8 (Note 1c)	0.8 (Note 1d)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value		Unit
		Q1	Q2	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	65 (Note 1a)	65 (Note 1b)	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	155 (Note 1c)	155 (Note 1d)	

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
FDMC7208S	FDMC7208S	WDFN8 3x3, 0.65P, Power 33 (Pb-Free)	3000 units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V I _D = 1 mA, V _{GS} = 0 V	Q1 Q2	30 30	– –	– –	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 10 mA, referenced to 25°C	Q1 Q2	– –	27 21	– –	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = ±20 V, V _{DS} = 0 V V _{GS} = ±12 V, V _{DS} = 0 V	Q1 Q2	– –	– –	100 100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	I _D = 250 μA, V _{GS} = 0 V I _D = 1 mA, V _{GS} = 0 V	Q1 Q2	1.2 1.2	1.7 1.6	3.0 3.0	V
ΔV _{GS(th)} / ΔT _J	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C I _D = 1 mA, referenced to 25°C	Q1 Q2	– –	–5 –3	– –	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 12 A V _{GS} = 4.5 V, I _D = 11 A V _{GS} = 10 V, I _D = 12 A, T _J = 125°C	Q1	– – –	6.7 8.8 9.2	9.0 11.0 12.4	mΩ
		V _{GS} = 10 V, I _D = 16 A V _{GS} = 4.5 V, I _D = 13.5 A V _{GS} = 10 V, I _D = 16 A, T _J = 125°C	Q2	– – –	4.7 5.3 6.4	6.4 7.5 6.8	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 12 A V _{DD} = 5 V, I _D = 16 A	Q1 Q2	– –	53 80	– –	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	Q1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz Q2 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	848 1685	1130 2245	pF
C _{oss}	Output Capacitance		Q1 Q2	– –	270 432	360 575	pF
C _{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	36 42	55 65	pF
R _g	Gate Resistance		Q1 Q2	0.1 0.1	1.1 1.0	2.5 2.5	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	Q1 V _{DD} = 15 V, I _D = 12 A, R _{GEN} = 6 Ω Q2 V _{DD} = 15 V, I _D = 16 A, R _{GEN} = 6 Ω	Q1 Q2	– –	6 7	12 14	ns
t _r	Rise Time		Q1 Q2	– –	2 3	10 10	ns
t _{d(off)}	Turn-Off Delay Time		Q1 Q2	– –	16 23	29 36	ns
t _f	Fall Time		Q1 Q2	– –	2 2	10 10	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V	Q1 Q2	– –	13 26	18 36	nC
		V _{GS} = 0 V to 5 V	Q1 Q2	– –	6.7 14	9.4 20	nC
Q _{gs}	Gate to Source Charge	Q1 V _{DD} = 15 V, I _D = 12 A	Q1 Q2	– –	2.3 3.9	– –	nC
Q _{gd}	Gate to Drain "Miller" Charge	Q2 V _{DD} = 15 V I _D = 16 A	Q1 Q2	– –	1.8 2.7	– –	nC

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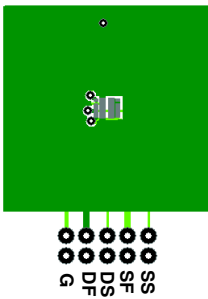
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	Q1	-	0.72	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$ (Note 2)	Q1	-	0.82	1.2	
		$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	Q2	-	0.70	1.2	
		$V_{GS} = 0\text{ V}, I_S = 16\text{ A}$ (Note 2)	Q2	-	0.82	1.2	
t_{rr}	Reverse Recovery Time	Q1 $I_F = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1	-	21	34	ns
			Q2	-	21	33	
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = 16\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1	-	6	12	nC
			Q2	-	16	28	

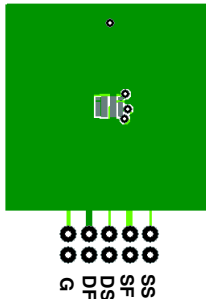
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

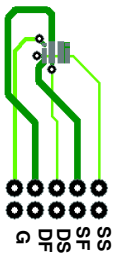
- $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



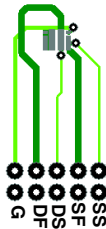
a) 65°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 65°C/W when mounted on a 1 in² pad of 2 oz copper.



c) 155°C/W when mounted on a minimum pad of 2 oz copper.



d) 155°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- Q1: E_{AS} of 21 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 12\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 3\text{ mH}$, $I_{AS} = 5.2\text{ A}$.
Q2: E_{AS} of 21 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 12\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 3\text{ mH}$, $I_{AS} = 5.4\text{ A}$.
- As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

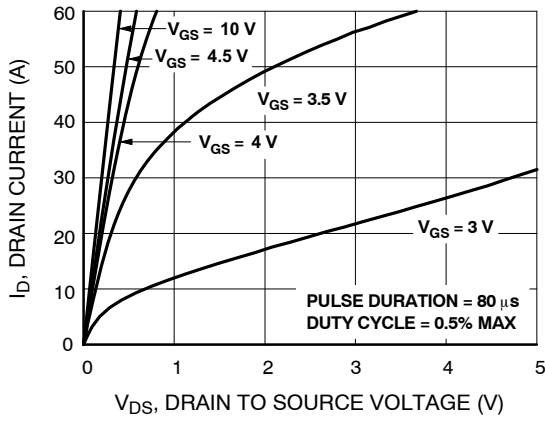


Figure 1. On-Region Characteristics

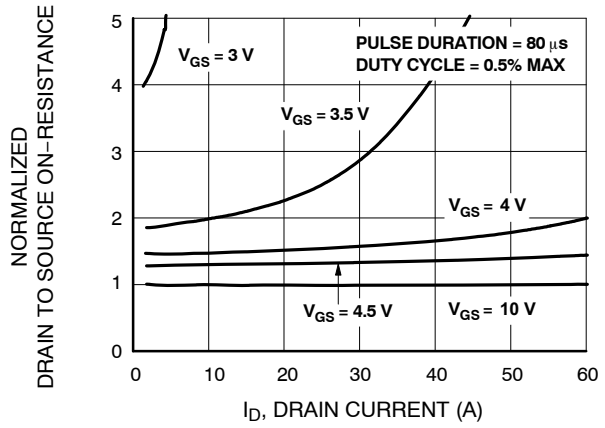


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

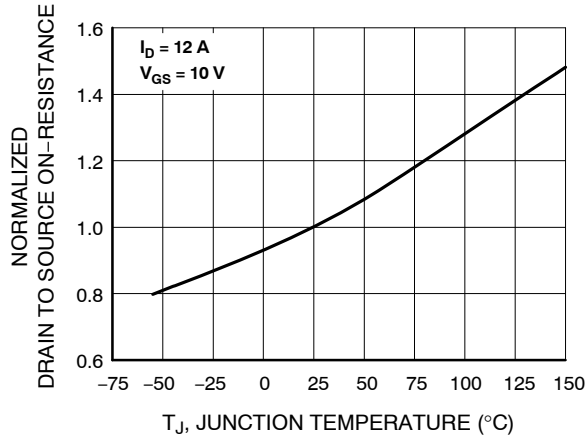


Figure 3. Normalized On-Resistance vs Junction Temperature

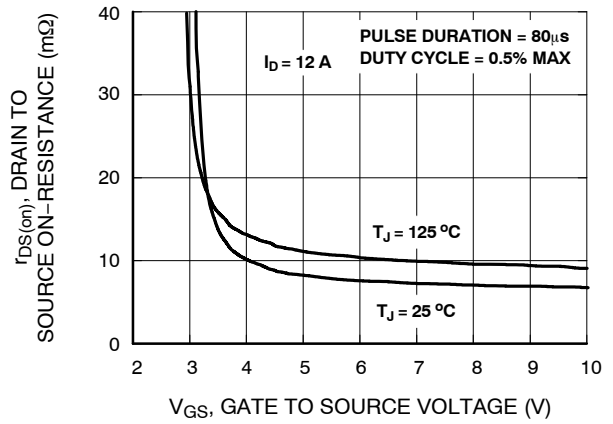


Figure 4. On-Resistance vs Gate to Source Voltage

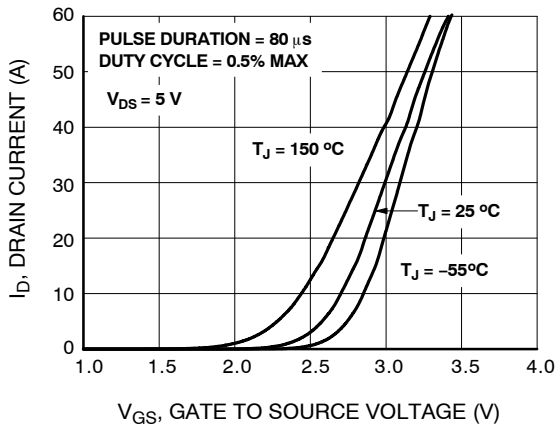


Figure 5. Transfer Characteristics

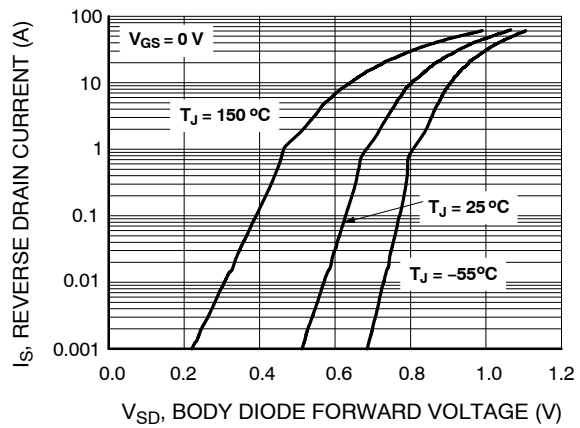


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

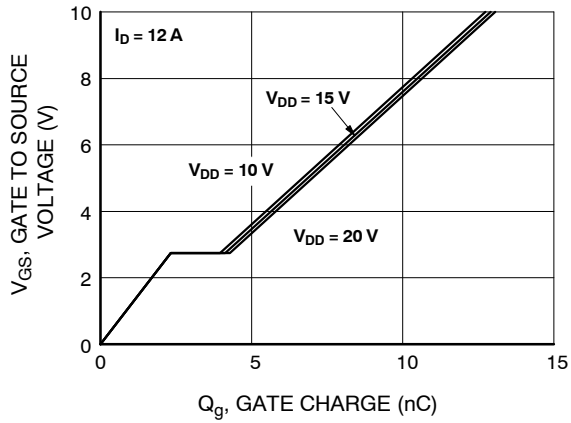


Figure 7. Gate Charge Characteristics

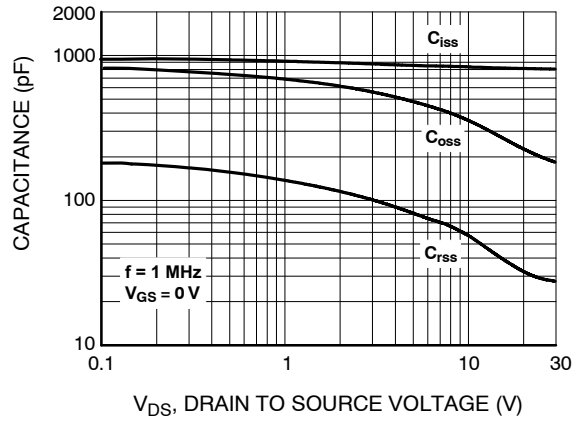


Figure 8. Capacitance vs Drain to Source Voltage

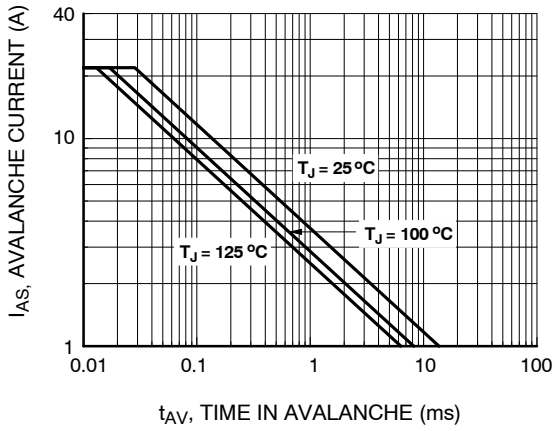


Figure 9. Unclamped Inductive Switching Capability

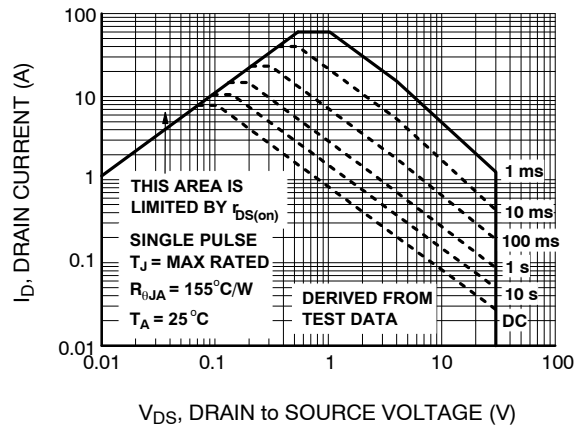


Figure 10. Forward Bias Safe Operating Area

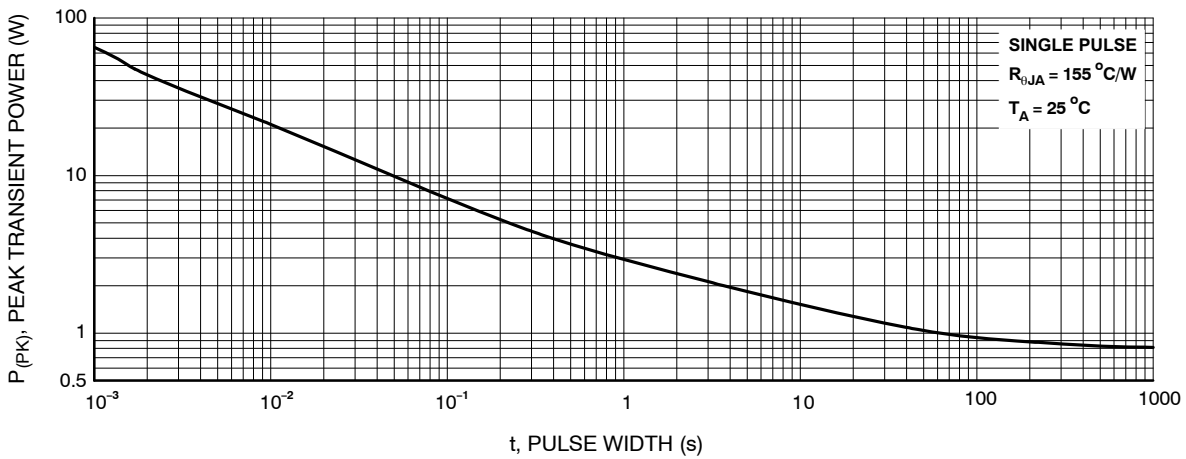


Figure 11. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

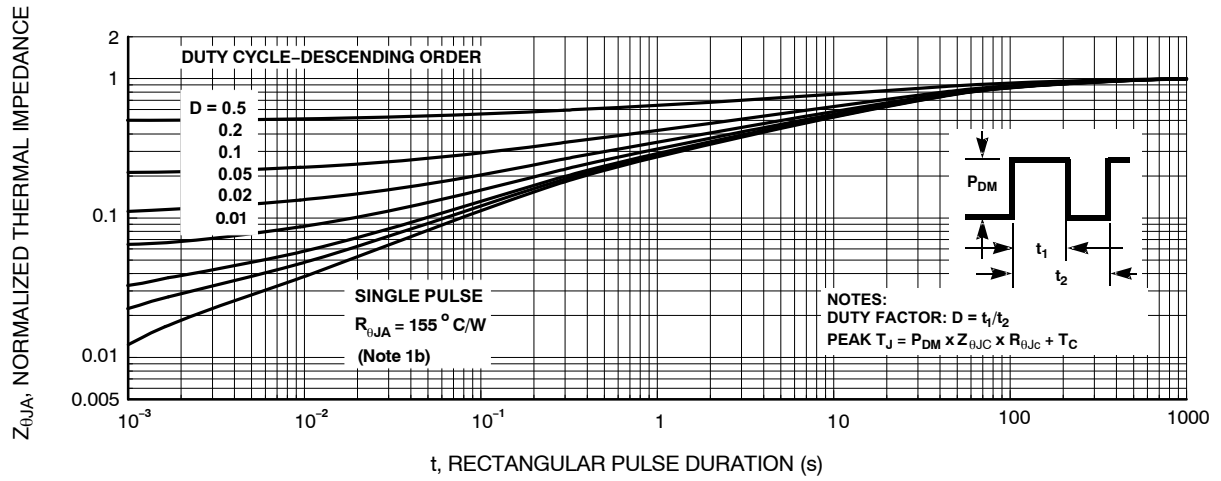


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

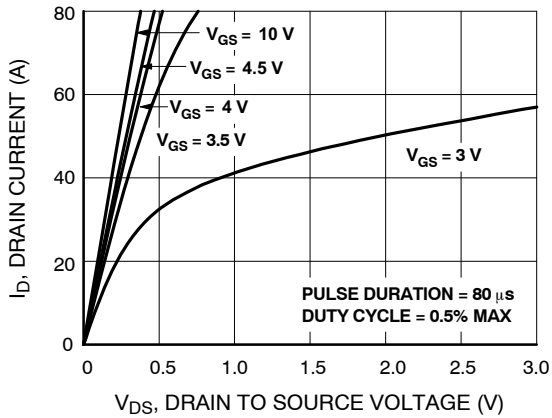


Figure 13. On-Region Characteristics

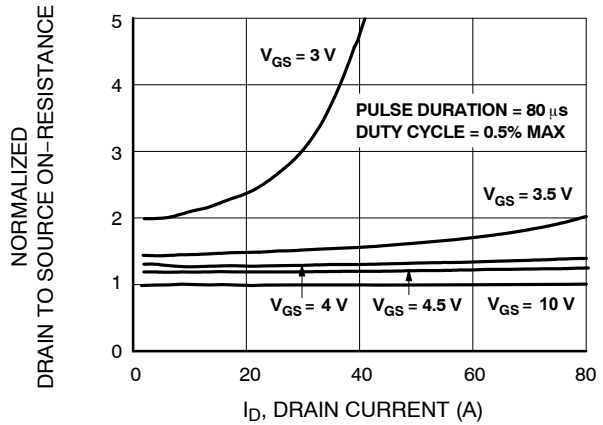


Figure 14. Normalized On-Resistance vs Drain Current and Gate Voltage

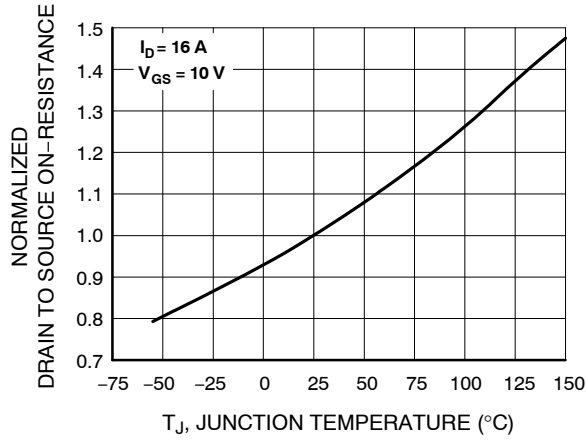


Figure 15. Normalized On-Resistance vs Junction Temperature

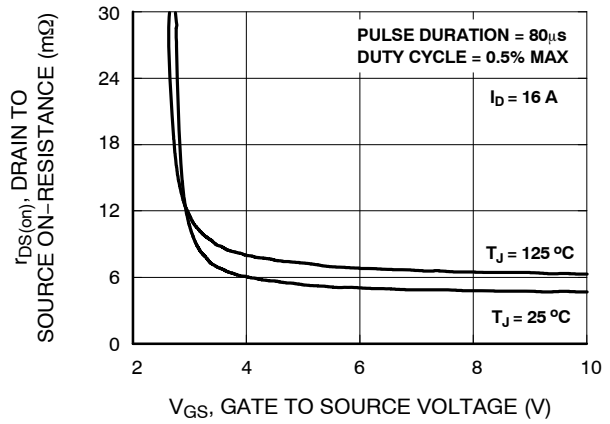


Figure 16. On-Resistance vs Gate to Source Voltage

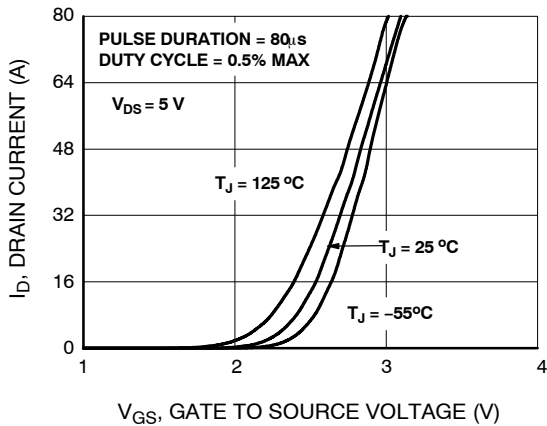


Figure 17. Transfer Characteristics

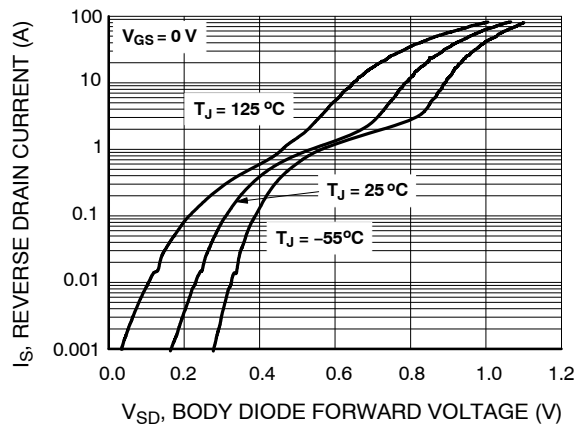


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

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TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

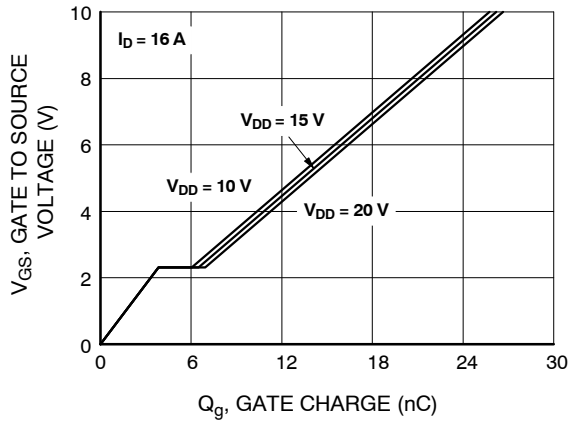


Figure 19. Gate Charge Characteristics

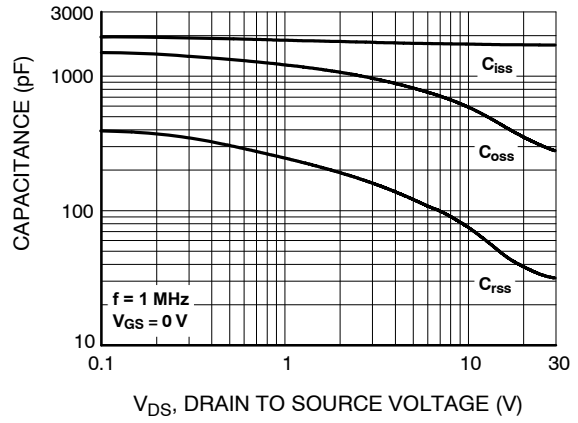


Figure 20. Capacitance vs Drain to Source Voltage

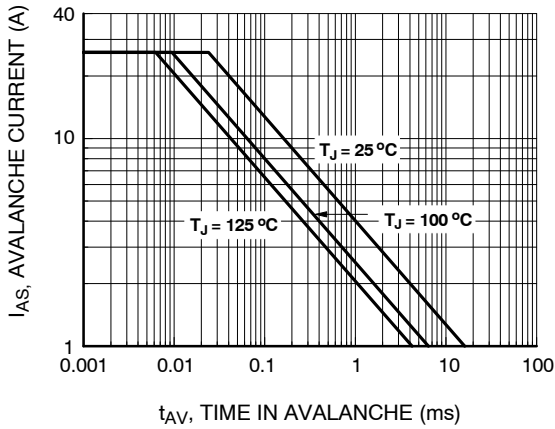


Figure 21. Unclamped Inductive Switching Capability

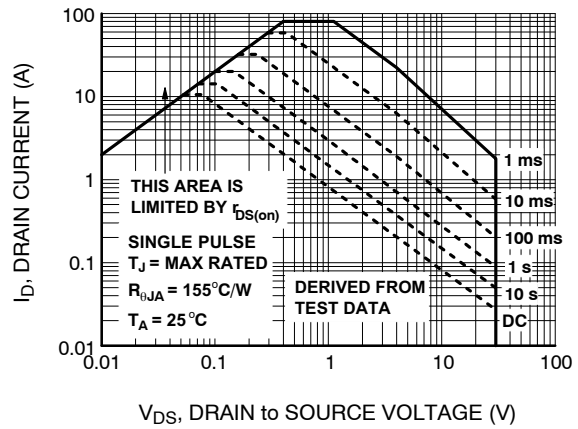


Figure 22. Forward Bias Safe Operating Area

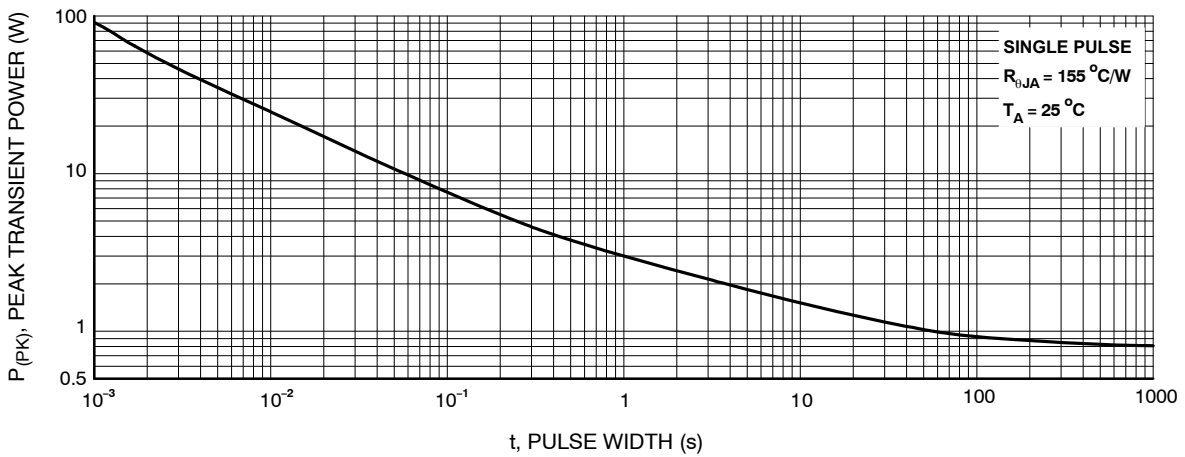


Figure 23. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

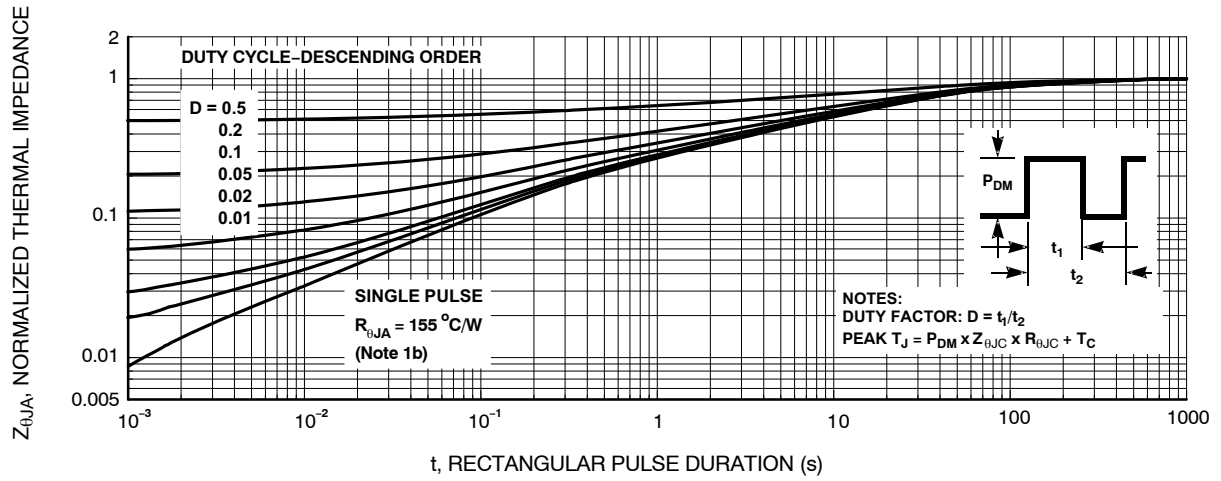
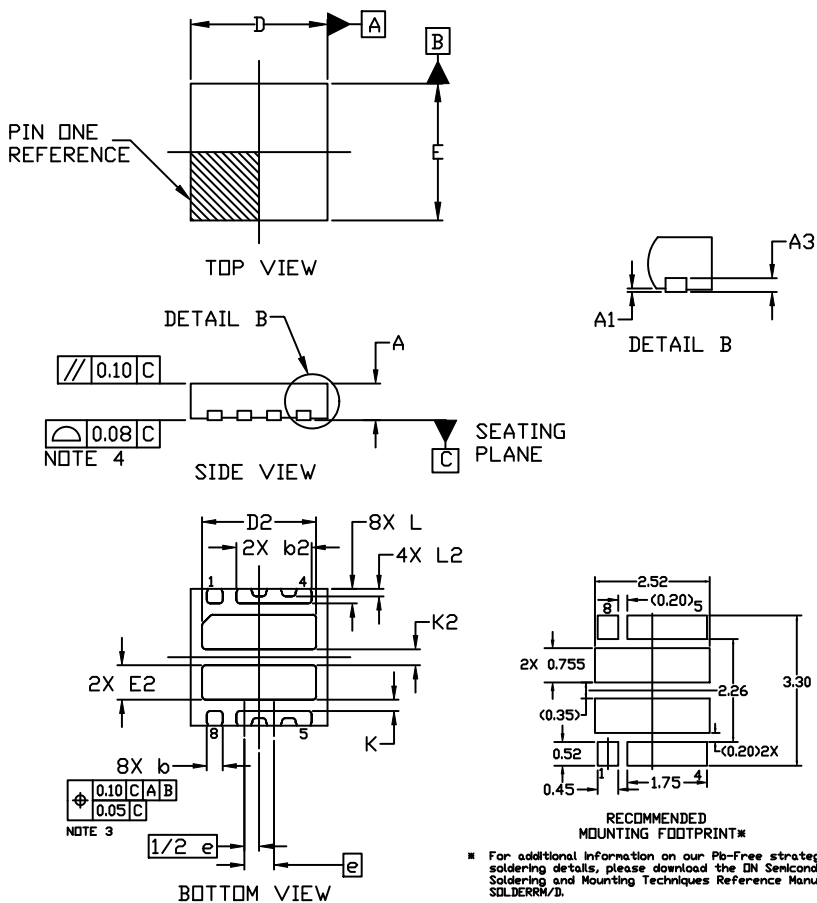


Figure 24. Transient Thermal Response Curve

WDFN8 3x3, 0.65P
CASE 511DG
ISSUE A

DATE 12 FEB 2019

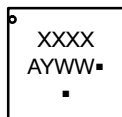


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
<i>b</i>	0.30	0.35	0.40
<i>b</i> 2	1.65 REF		
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
<i>e</i>	0.65 BSC		
K	0.25	---	---
K2	0.35 REF		
L	0.27	0.32	0.37
L2	0.163 REF		

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SLD166RM/D.

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DESCRIPTION:	WDFN8 3x3, 0.65P	PAGE 1 OF 1

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