

MOSFET – N-Channel, Shielded Gate POWERTRENCH®

80 V, 66 A, 7 mΩ

FDMC007N08LC

General Description

This N-Channel MV MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 7.0 mΩ at $V_{GS} = 10$ V, $I_D = 21$ A
- Max $R_{DS(on)}$ = 10.4 mΩ at $V_{GS} = 4.5$ V, $I_D = 17$ A
- 5 V Drive Capable
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and RoHS Compliant

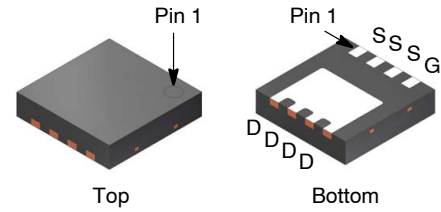
Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

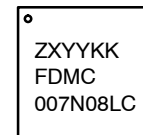
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		A
	– Continuous (Note 5)	$T_C = 25^\circ\text{C}$	66
	– Continuous (Note 5)	$T_C = 100^\circ\text{C}$	42
	– Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	14
	– Pulsed (Note 4)		330
E_{AS}	Single Pulse Avalanche Energy (Note 3)	150	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	57
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.4
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



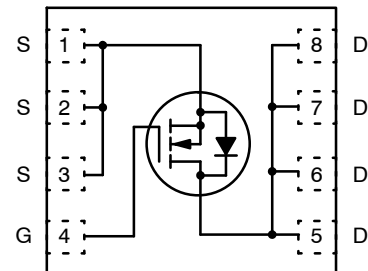
WDFN8 3.3x3.3, 0.65P
(Power 33)
CASE 483AW

MARKING DIAGRAM



- Z = Assembly Plant Code
- X = Year Code
- YY = Two-digit Weekly Numeric Code
- KK = Two-digit Alphanumeric Lot Code
- FDMC = Specific Device Code
- 007N08LC = Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMC007N08LC

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.2	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}$	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	–	45	–	$\text{mV}/^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{V}, V_{GS} = 0 \text{V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{V}, V_{DS} = 0 \text{V}$	–	–	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 120 \mu\text{A}$	1.0	1.5	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 120 \mu\text{A}$, referenced to 25°C	–	–5.4	–	$\text{mV}/^{\circ}\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{V}, I_D = 21 \text{A}$	–	5.7	7.0	m Ω
		$V_{GS} = 4.5 \text{V}, I_D = 17 \text{A}$	–	8.3	10.4	
		$V_{GS} = 10 \text{V}, I_D = 21 \text{A}, T_J = 125^{\circ}\text{C}$	–	9.9	12.2	
g_{FS}	Forward Transconductance	$V_{DD} = 5 \text{V}, I_D = 21 \text{A}$	–	80	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 40 \text{V}, V_{GS} = 0 \text{V}, f = 1 \text{MHz}$	–	2100	2940	pF
C_{oss}	Output Capacitance		–	506	710	pF
C_{rss}	Reverse Transfer Capacitance		–	18	30	pF
R_g	Gate Resistance		0.1	0.4	0.8	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40 \text{V}, I_D = 21 \text{A}, V_{GS} = 10 \text{V}, R_{GEN} = 6 \Omega$	–	10	20	ns
t_r	Rise Time		–	2.4	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	24	39	ns
t_f	Fall Time		–	2.1	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0 \text{V to } 10 \text{V}, V_{DD} = 40 \text{V}, I_D = 21 \text{A}$	–	29	41	nC
		$V_{GS} = 0 \text{V to } 4.5 \text{V}, V_{DD} = 40 \text{V}, I_D = 21 \text{A}$	–	14	19	
Q_{gs}	Gate to Source Charge	$V_{DD} = 40 \text{V}, I_D = 21 \text{A}$	–	5	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	3	–	nC
Q_{oss}	Output Charge	$V_{DD} = 40 \text{V}, V_{GS} = 0 \text{V}$	–	30	–	nC
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0 \text{V}, I_D = 21 \text{A}$	–	27	–	nC

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

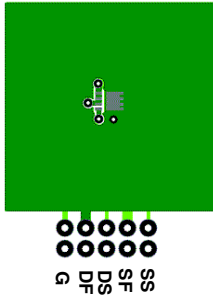
DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2 A (Note 2)	0.1	0.7	1.2	V
		V _{GS} = 0 V, I _S = 21 A (Note 2)	0.1	0.8	1.3	
t _{rr}	Reverse Recovery Time	I _F = 10 A, di/dt = 300 A/μs	–	20	32	ns
Q _{rr}	Reverse Recovery Charge		–	27	43	nC
t _{rr}	Reverse Recovery Time	I _F = 10 A, di/dt = 1000 A/μs	–	14	22	ns
Q _{rr}	Reverse Recovery Charge		–	62	99	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θCA} is determined by the user's board design.



a) 53°C/W when mounted on a 1 in² pad of 2 oz copper



b) 125°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.
- E_{AS} of 150 mJ is based on starting T_J = 25°C, L = 3 mH, I_{AS} = 10 A, V_{DD} = 80 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 33 A.
- Pulsed Id please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

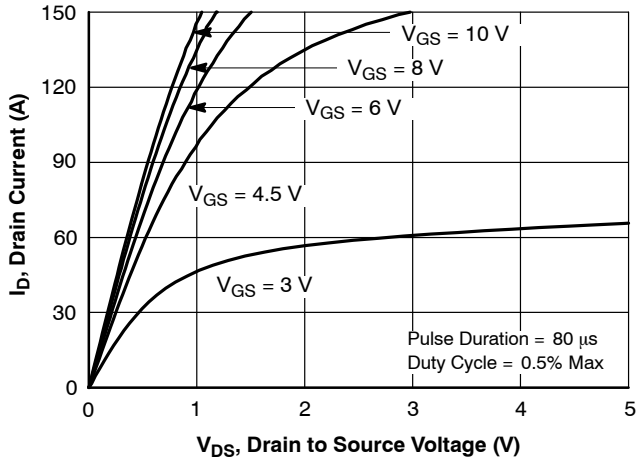


Figure 1. On Region Characteristics

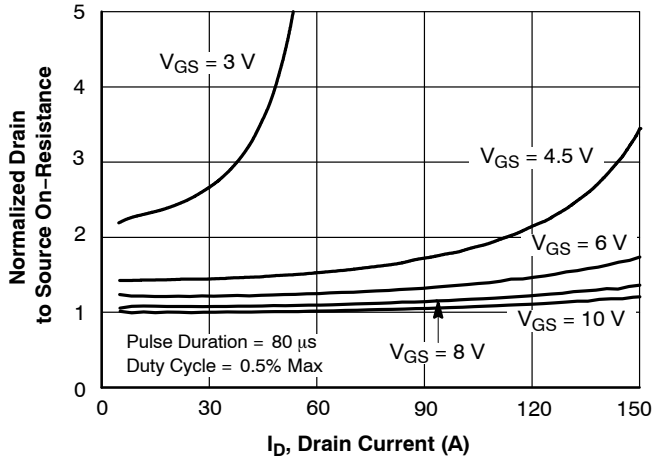


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

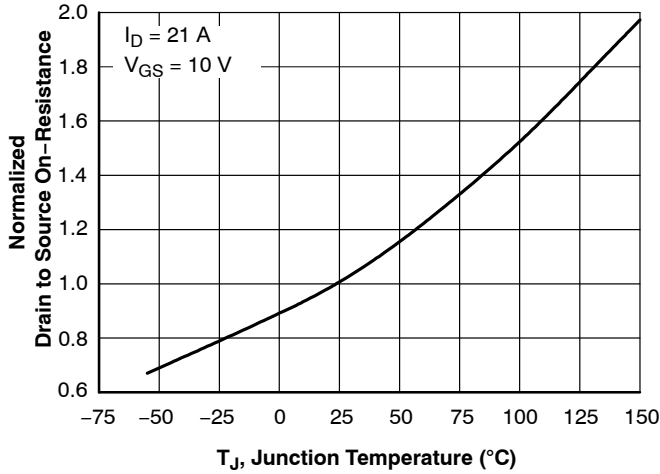


Figure 3. Normalized On Resistance vs. Junction Temperature

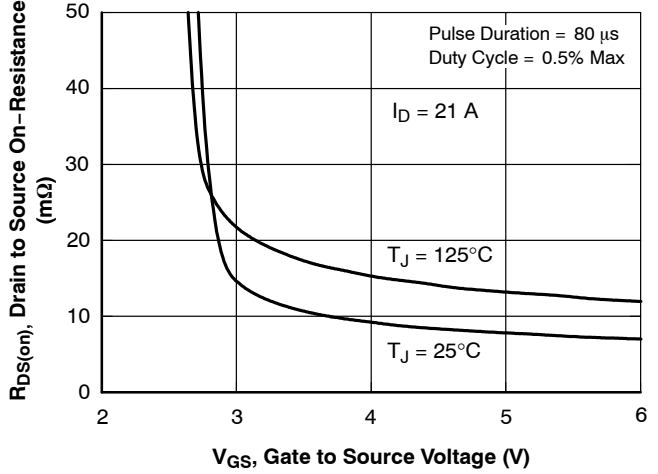


Figure 4. On-Resistance vs. Gate to Source Voltage

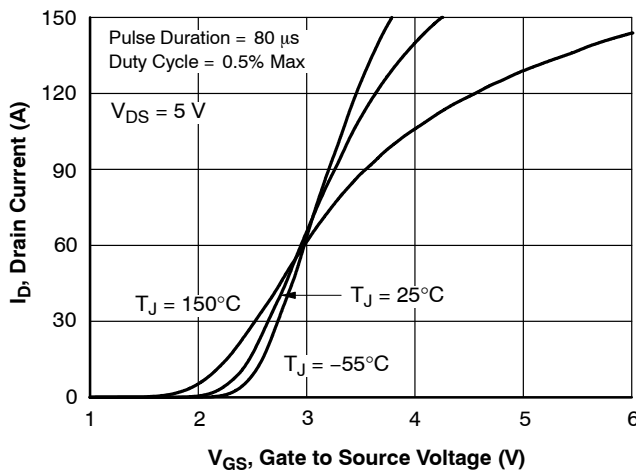


Figure 5. Transfer Characteristics

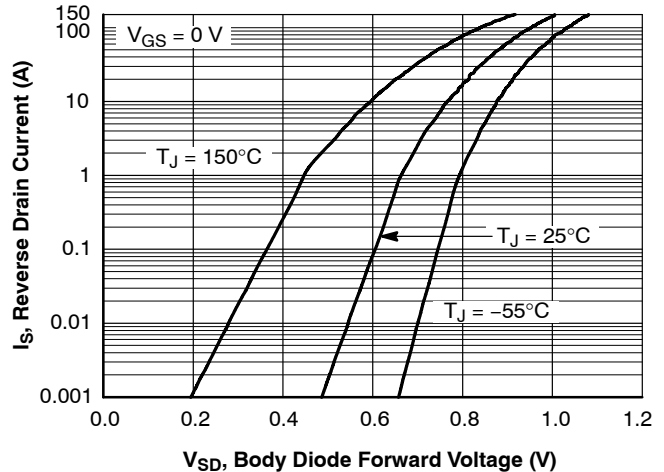


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

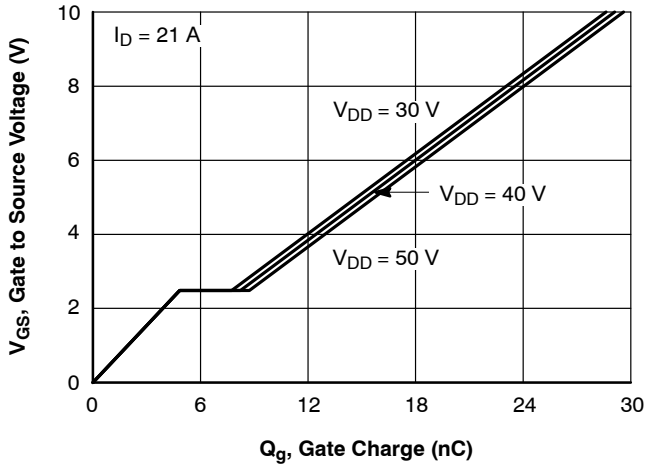


Figure 7. Gate Charge Characteristics

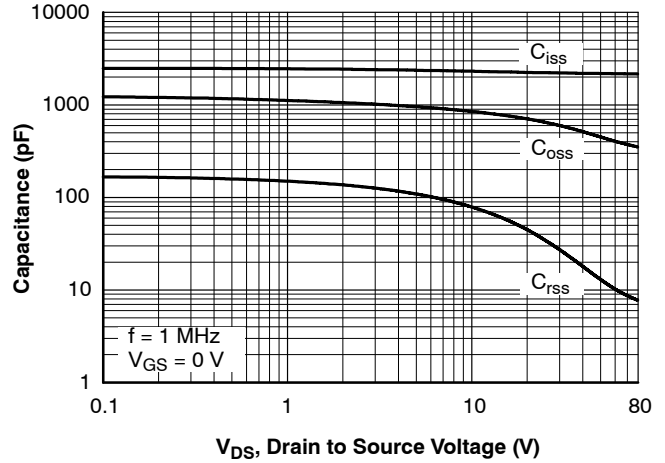


Figure 8. Capacitance vs. Drain to Source Voltage

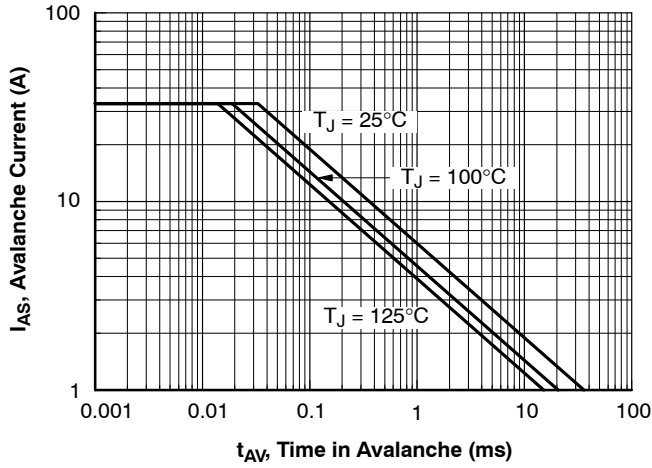


Figure 9. Unclamped Inductive Switching Capability

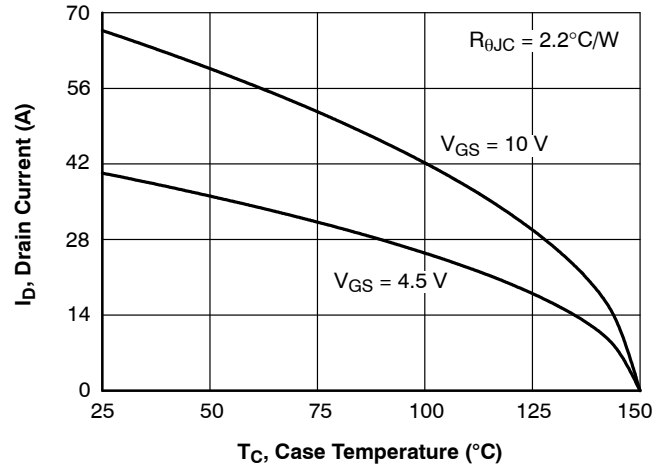


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

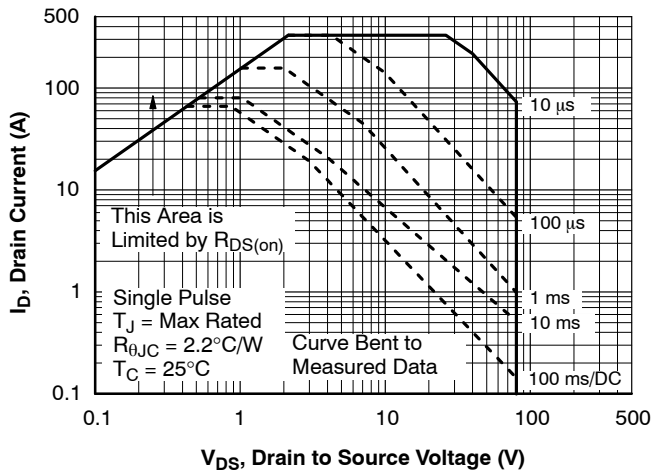


Figure 11. Forward Bias Safe Operating Area

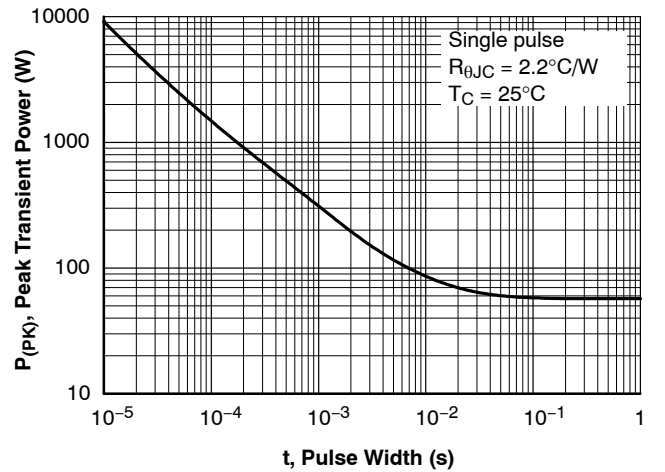


Figure 12. Single Pulse Maximum Power Dissipation

FDMC007N08LC

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

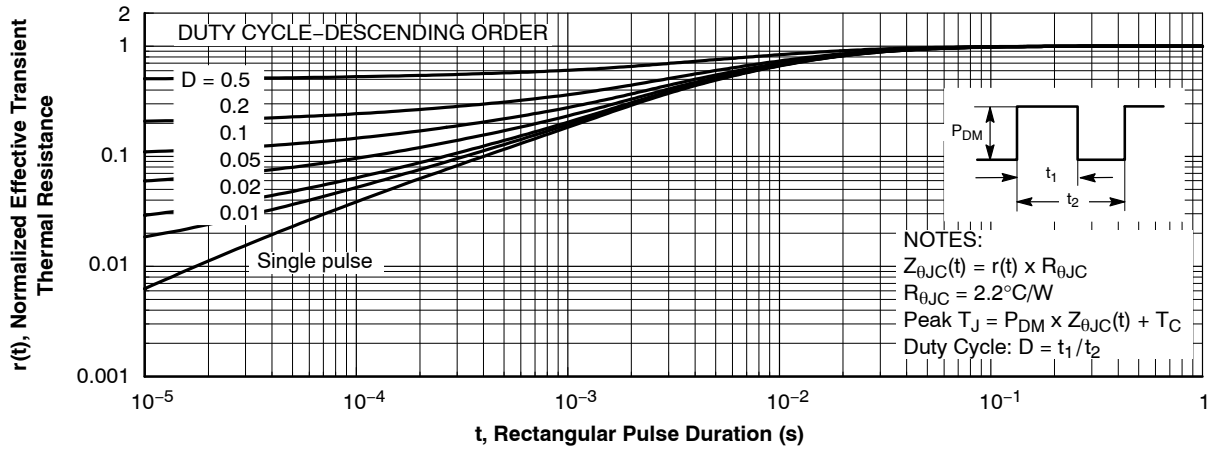


Figure 13. Junction-to-Case Transient Thermal Response Curve

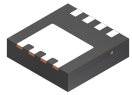
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC007N08LC	FDMC007N08LC	WDFN8 3.3x3.3, 0.65P (Power 33) (Pb-Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

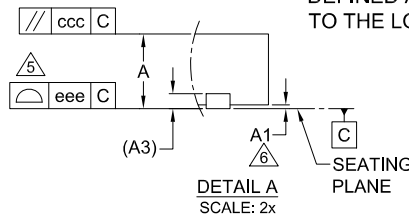
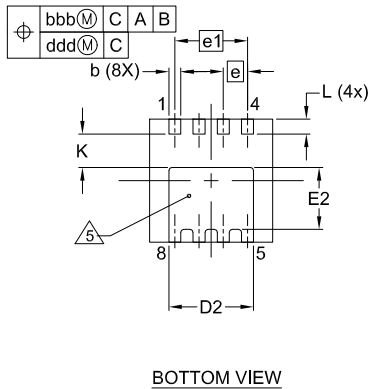
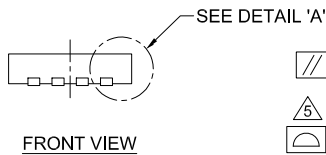
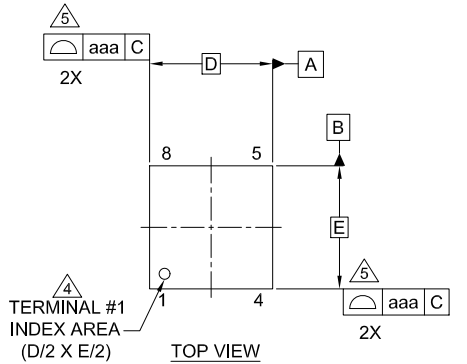
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

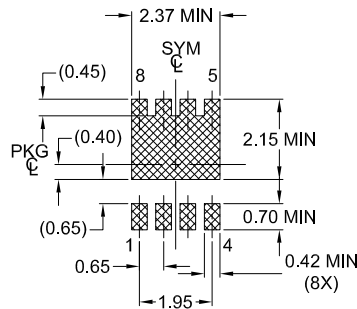


WDFN8 3.30x3.30x0.75, 0.65P
CASE 483AW
ISSUE B

DATE 22 MAR 2024



LAND PATTERN RECOMMENDATION



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.30 BSC		
D2	2.17	2.27	2.37
E	3.30 BSC		
E2	1.56	1.66	1.76
e	0.65 BSC		
e1	1.95 BSC		
K	0.90	--	--
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN8 3.30x3.30x0.75, 0.65P	PAGE 1 OF 1

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