# <u>MOSFET</u> – Power, N-Channel, UltraFET

55 V, 75 A, 7 m $\Omega$ 

# FDH5500-F085

## Features

- Typ  $R_{DS(on)} = 5.2 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 75 \text{ A}$
- Typ  $Q_{g(10)} = 118 \text{ nC}$  at  $V_{GS} = 10 \text{ V}$
- Simulation Models -Temperature Compensated PSPICE<sup>™</sup> and Saber<sup>®</sup> Models
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

## Applications

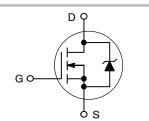
- DC Linear Mode Control
- Solenoid and Motor Control
- Switching Regulators
- Automotive Systems

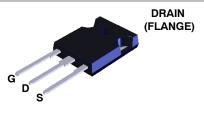


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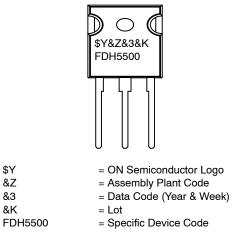
V <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
55 V	$7 \text{ m}\Omega$	75 A





JEDEC TO-247 CASE 340CK

# MARKING DIAGRAM



## **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

Symbol		Parameter	Value	Unit
V <sub>DSS</sub>	Drain to Source Voltage (	55	V	
V <sub>DGR</sub>	Gate to Gate Voltage (RG	<sub>S</sub> = 20 kΩ) (Note 1)	55	V
V <sub>GS</sub>	Gate to Source Voltage	±20	V	
I <sub>D</sub>	Drain Current Continuous	75	А	
	Pulsed		Figure 4	
E <sub>AS</sub>	Single Pulse Avalanche E	Single Pulse Avalanche Energy (Note 2)		mJ
PD	Power Dissipation	(T <sub>C</sub> = 25°C)	375	W
		– Derate Above 25°C	2.5	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Te	Operating and Storage Temperature		
ΤL	Max. Lead Temp. for Solo	Max. Lead Temp. for Soldering (at 1.6 mm from case for 10 sec)		
T <sub>pkg</sub>	Max. Package Temp. for	Soldering (Package Body for 10 sec)	260	°C

#### MOSFET MAXIMUM RATINGS (T<sub>C</sub> = 25°C, Unless otherwise noted)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Starting  $T_J = 25^{\circ}C$  to  $175^{\circ}C$ . 2. Starting  $TJ = 25^{\circ}C$ , L = 0.48 mH,  $I_{AS} = 60$  A

#### **THERMAL CHARACTERISTICS**

Symbol	Parameter	Value	Unit
$R_{\thetaJC}$	Thermal Resistance Junction to Case	0.4	°C/W
$R_{\thetaJA}$	Thermal Resistance Junction to Ambient TO-247, 1in <sup>2</sup> copper pad area	30	°C/W

#### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDH5500	FDH5500-F085	TO-247	Tube	N/A	30 Units

### **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
	TERISTICS					
B <sub>VDSS</sub>	Drain to Source Breakdown Voltage	$I_D$ = 250 $\mu$ A, $V_{GS}$ = 0 V	55			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS}$ = 50 V, $V_{GS}$ = 0 V, $V_{DS}$ = 45 V			1	μA
		$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, V_{DS} = 45 \text{ V}, T_{C} = 150^{\circ}\text{C}$			250	
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$			±100	nA

#### ON CHARACTERISTICS

V <sub>GS(TH)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, \ I_D = 250 \ \mu A$	2.0	2.9	4.0	V
R <sub>DS(ON)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 75 A, V <sub>GS</sub> = 10 V		5.2	7	mΩ

#### DYNAMIC CHARACTERISTICS

C <sub>ISS</sub>	Input Capacitance	$V_{DS}$ = 25 V, $V_{GS}$ =	$V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1 MHz		3565		pF
C <sub>OSS</sub>	Output Capacitance		Ī		1310		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance				395		pF
Q <sub>g(TOT)</sub>	Total Gate Charge at 20 V	$V_{GS}$ = 0 V to 20 V	$V_{DD} = 30 V$		206	268	nC
Q <sub>g(10)</sub>	Total Gate Charge 10 V	$V_{GS} = 0 V$ to 10 V	14 - 0.1 22		118	153	nC
Q <sub>g(TH)</sub>	Threshold Gate Charge	$V_{GS}$ = 0 V to 2 V	l <sub>g</sub> = 1.0 mA		6.2	8.1	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	$V_{DD} = 30 \text{ V}, \text{ I}_{D} = 75$			17.8		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	$R_{L} = 0.4 \Omega, I_{g} = 1.0$	) mA		51		nC

#### SWITCHING CHARACTERISTICS

t <sub>on</sub>	Turn-On Time	$V_{DD} = 30 V$		185	ns
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 30 V$ $I_{D} = 75 A$ $R_{L} = 0.4 \Omega$ $V_{GS} = 10 V$ $R_{GS} = 2.5 \Omega$	13.7		ns
tr	Rise Time	V <sub>GS</sub> = 10 V R <sub>GS</sub> = 2.5 Ω	102		ns
t <sub>d(off)</sub>	Turn-Off Delay Time		34		ns
t <sub>f</sub>	Fall Time		22		ns
t <sub>off</sub>	Turn-Off Time			91	ns

#### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Voltage	I <sub>SD</sub> = 75 A	1	1.25	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 75 A, dI <sub>SD</sub> /dt = 100 A/μs	60	78	ns
Q <sub>rr</sub>	Reverse Recovery Charge		77	100	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## **TYPICAL CHARACTERISTICS**

(T<sub>C</sub> =  $25^{\circ}$ C unless otherwise noted)

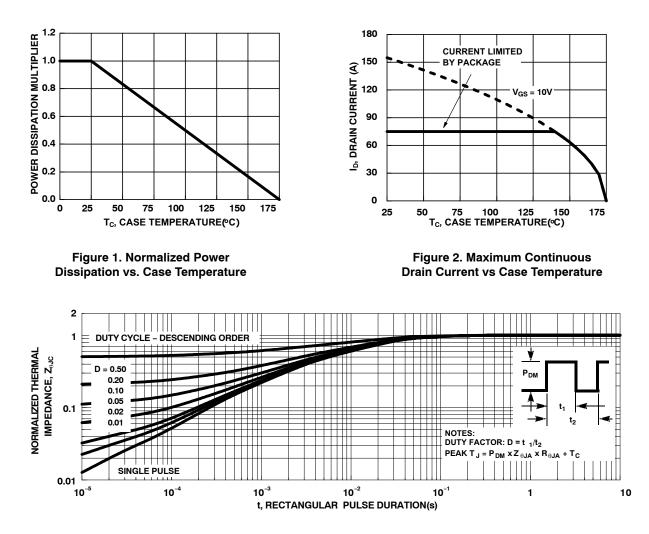


Figure 3. Normalized Maximum Transient Thermal Impedance

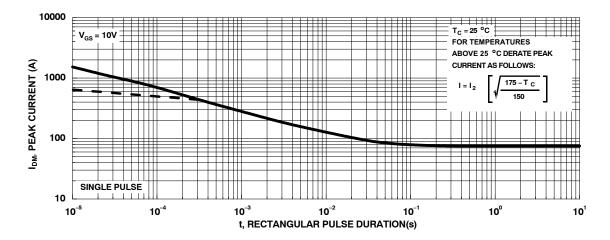


Figure 4. Peak Current Capability

### TYPICAL CHARACTERISTICS (Continued)

(T<sub>C</sub> = 25°C unless otherwise noted)

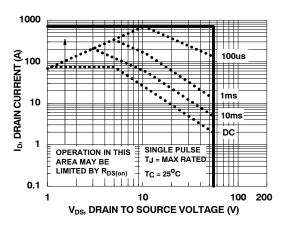


Figure 5. Forward Bias Safe Operating Area

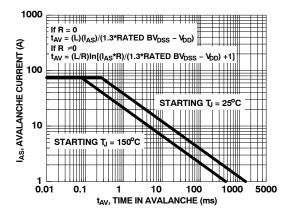


Figure 6. Unclamped Inductive Switching Capability

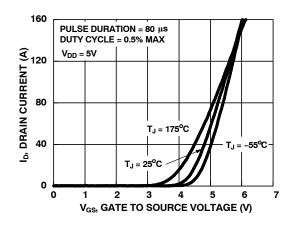
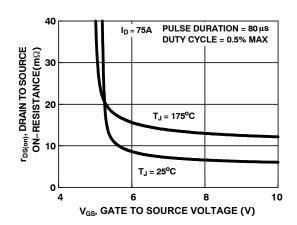
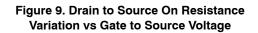
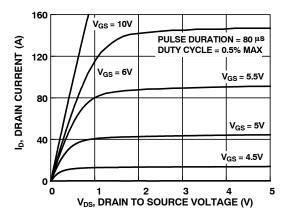


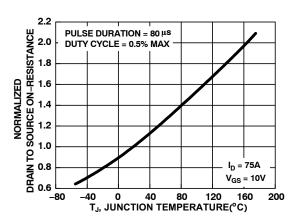
Figure 7. Transfer Characteristics







**Figure 8. Saturation Characteristics** 





#### TYPICAL CHARACTERISTICS (Continued)

(T<sub>C</sub> = 25°C unless otherwise noted)

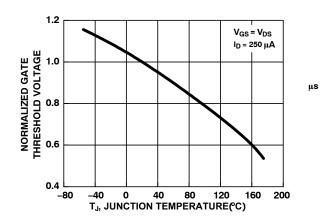


Figure 11. Normalized Gate Threshold Voltage vs. Junction Temperature

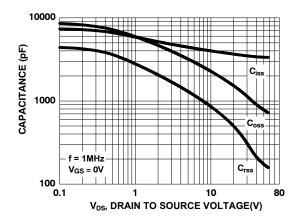


Figure 13. Capacitance vs. Drain to Source Voltage

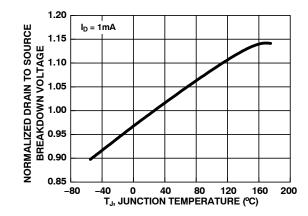


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

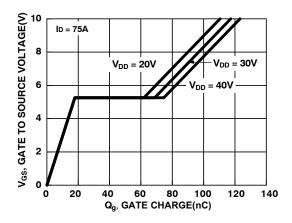


Figure 14. Gate Charge vs. Gate to Source Voltage

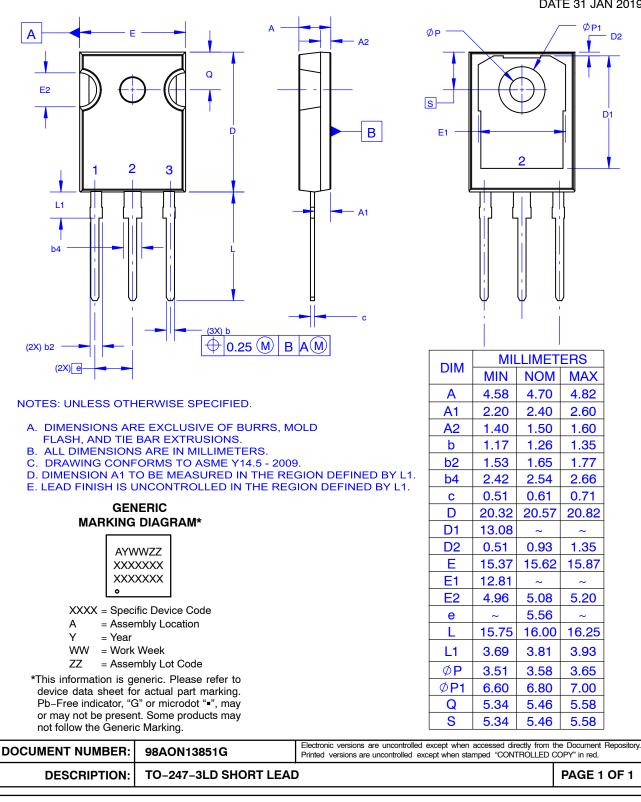
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