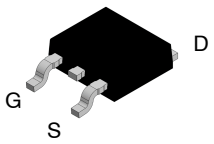
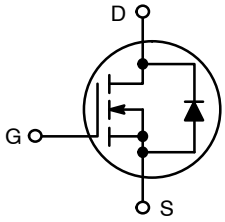
# MOSFET – N-Channel, POWERTRENCH®

## 60 V, 50 A, 12.3 mΩ

# FDD5353




**DPAK3**
**CASE 369AS**




**N-Channel MOSFET**

### General Description

This N-Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Features

- Max $R_{DS(on)}$ = 12.3 mΩ at $V_{GS}$ = 10 V, $I_D$ = 10.7 A
- Max $R_{DS(on)}$ = 15.4 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 9.5 A
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and RoHS Compliant

### Applications

- Inverter
- Synchronous Rectifier
- Primary Switch

### MARKING DIAGRAM


| | |
|---|---|
| &Z | = Assembly Plant Code |
| &3 | = Date Code (Year & Week) |
| &K | = 2 Digit Lot Run Traceability Code |
| FDD5353 | = Specific Device Code |

### MOSFET MAXIMUM RATINGS ($T_C$ = 25°C unless otherwise noted)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 60 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current<br>–Continuous $T_C$ = 25°C<br>–Continuous $T_A$ = 25°C (Note 1a)<br>–Pulsed | <br>50<br>11.5<br>100 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | 253 | mJ |
| $P_D$ | Power Dissipation<br>$T_C$ = 25°C<br>$T_A$ = 25°C (Note 1a) | <br>69<br>3.1 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | –55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Maximum Resistance, Junction to Case | 1.8 | °C/W |
| $R_{\theta JA}$ | Maximum Resistance, Junction to Ambient (Note 1a) | 40 | |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDD5353 | DPAK3 | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

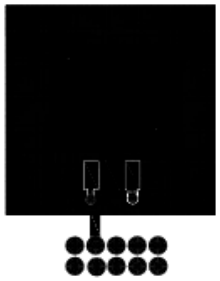
**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise d)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 60 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | 77 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{GS}$ = 0 V, $V_{DS}$ = 48 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.0 | 1.8 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | –8 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 10.7 A | – | 10.1 | 12.3 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 9.5 A | – | 12.1 | 15.4 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 10.7 A, $T_J$ = 125°C | – | 16.7 | 20.3 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5 V, $I_D$ = 10.7 A | – | 41 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 2420 | 3215 | pF |
| $C_{oss}$ | Output Capacitance | | – | 215 | 285 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 120 | 180 | pF |
| $R_g$ | Gate Resistance | f = 1 MHz | – | 1.7 | – | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 30 V, $I_D$ = 10.7 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 11 | 20 | ns |
| $t_r$ | Rise Time | | – | 6 | 11 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | – | 36 | 58 | ns |
| $t_f$ | Fall Time | | – | 4 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V<br>$V_{DD}$ = 30 V, $I_D$ = 10.7 A | – | 46 | 65 | nC |
| | | $V_{GS}$ = 0 V to 4.5 V<br>$V_{DD}$ = 30 V, $I_D$ = 10.7 A | – | 23 | 32 | nC |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 30 V, $I_D$ = 10.7 A | – | 7 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 30 V, $I_D$ = 10.7 A | – | 9 | – | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 10.7 A (Note 2) | – | 0.8 | 1.3 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 2.6 A (Note 2) | – | 0.7 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 10.7 A, di/dt = 100 A/μs | – | 28 | 45 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 21 | 34 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 40 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.

b) 96 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. $E_{AS}$ of 253 mJ is based on starting $T_J$ = 25°C, L = 3 mH, $I_{AS}$ = 13 A, $V_{DD}$ = 60 V, $V_{GS}$ = 10 V. 100% test at L = 0.1 mH, $I_{AS}$ = 41 A.

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise noted)

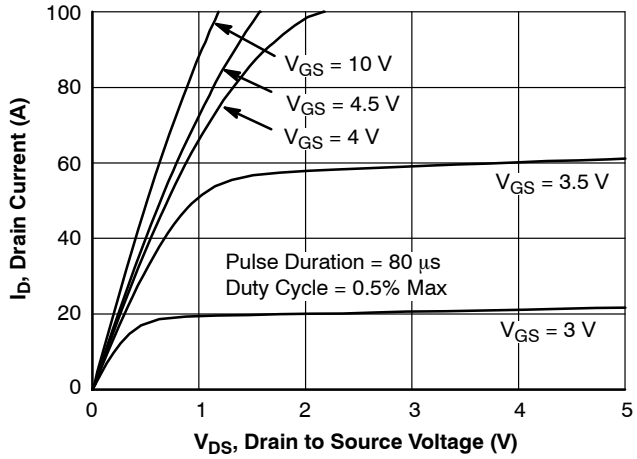



**Figure 1. On-Region Characteristics**

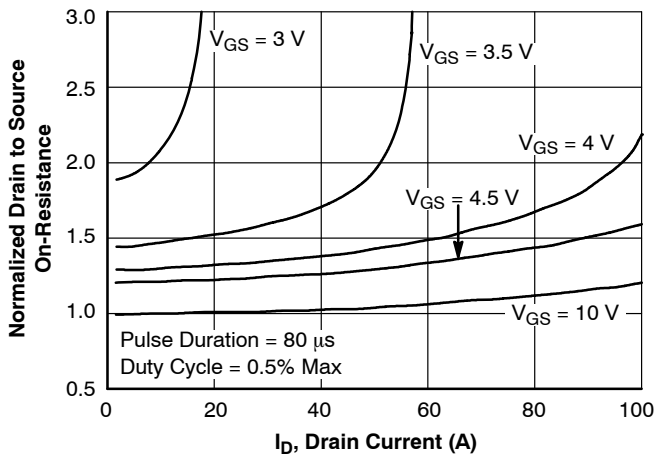



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

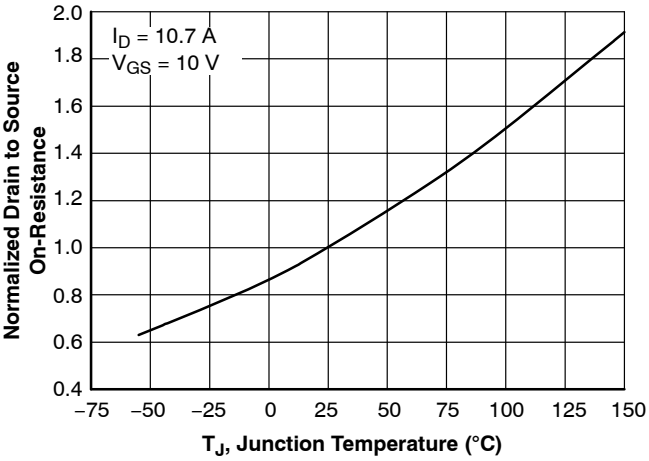



**Figure 3. Normalized On-Resistance vs Junction Temperature**

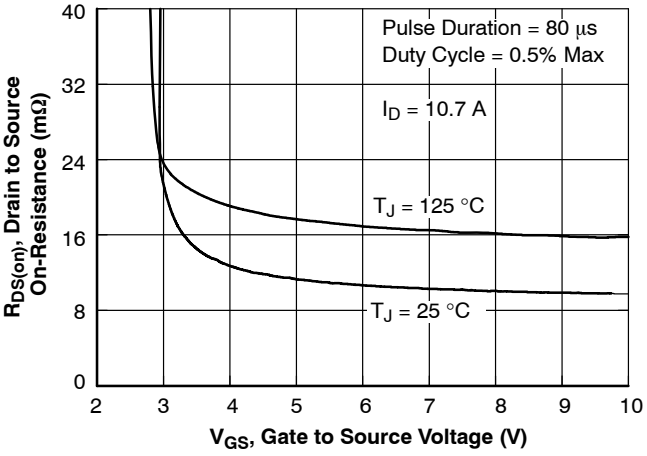



**Figure 4. On-Resistance vs Gate to Source Voltage**

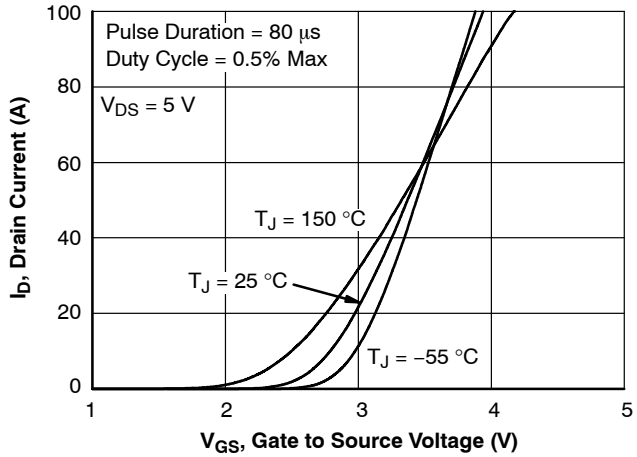



**Figure 5. Transfer Characteristics**

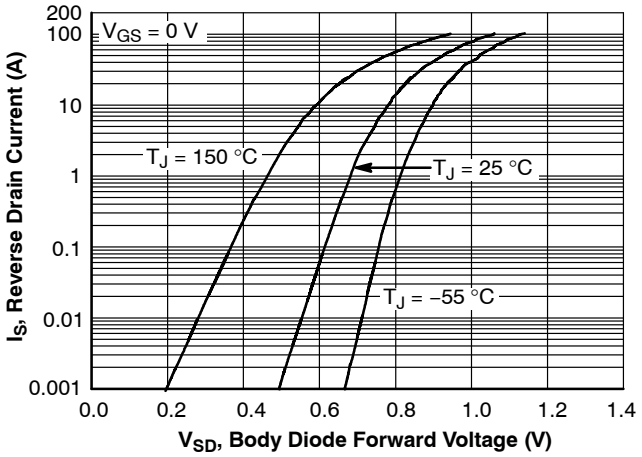



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## TYPICAL CHARACTERISTICS (continued)

($T_J$ = 25°C unless otherwise noted)

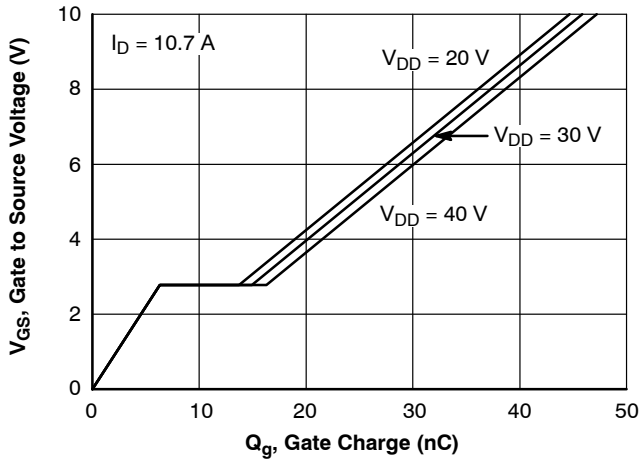



**Figure 7. Gate Charge Characteristics**

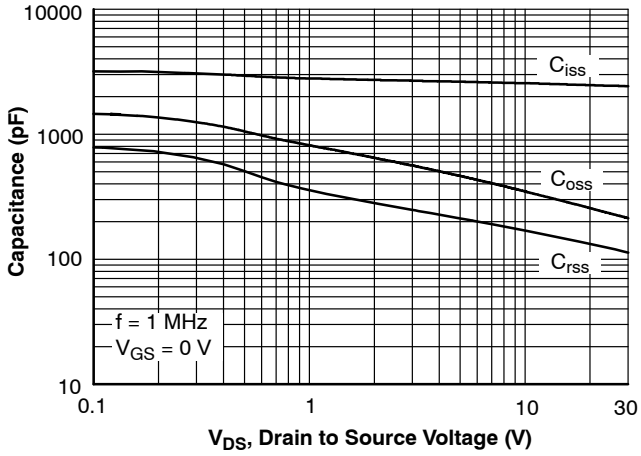



**Figure 8. Capacitance vs Drain to Source Voltage**

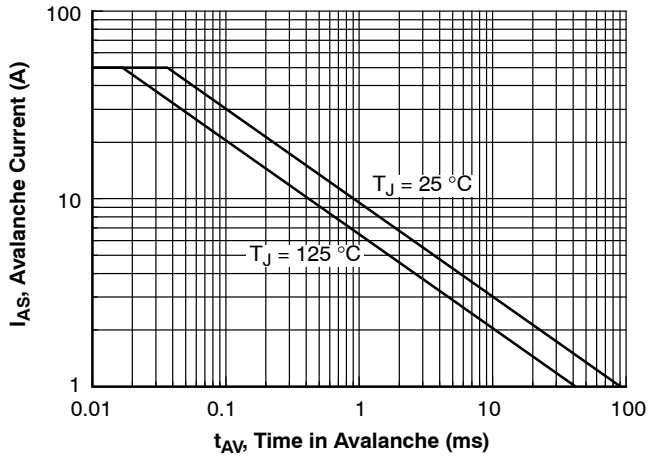



**Figure 9. Unclamped Inductive Switching Capability**

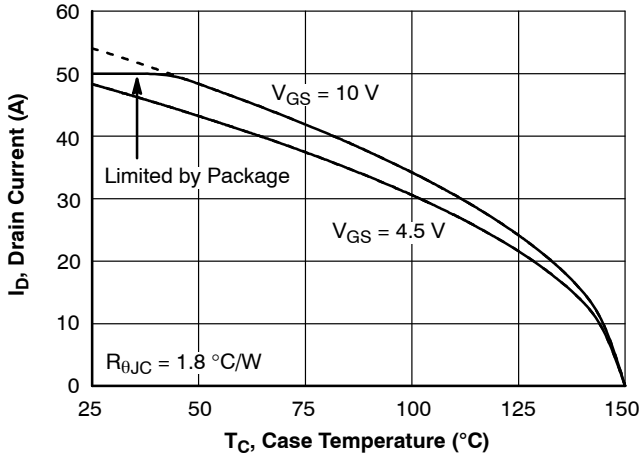



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

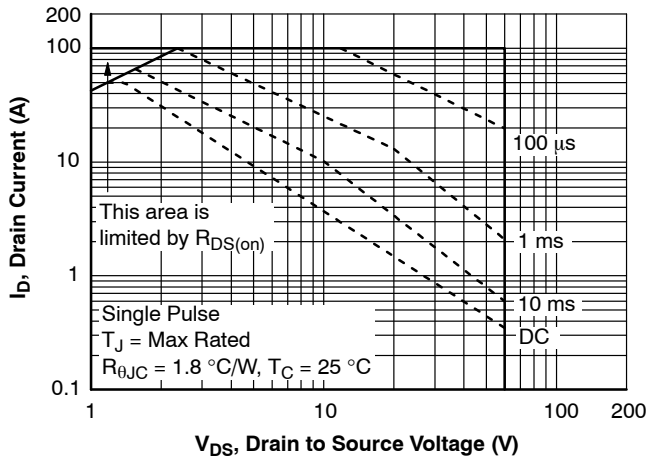



**Figure 11. Forward Bias Safe Operating Area**

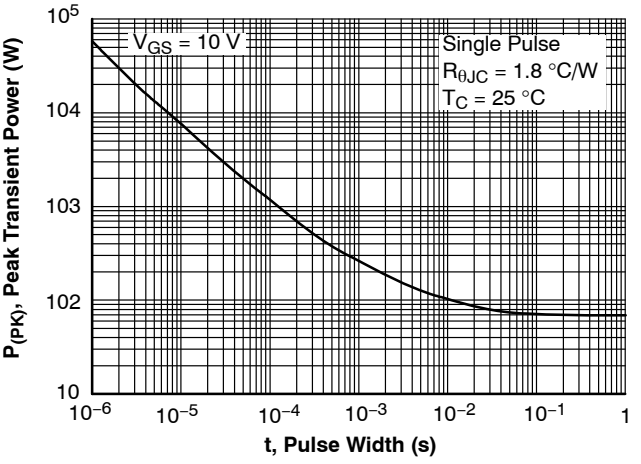



**Figure 12. Single Pulse Maximum Power Dissipation**

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise noted)

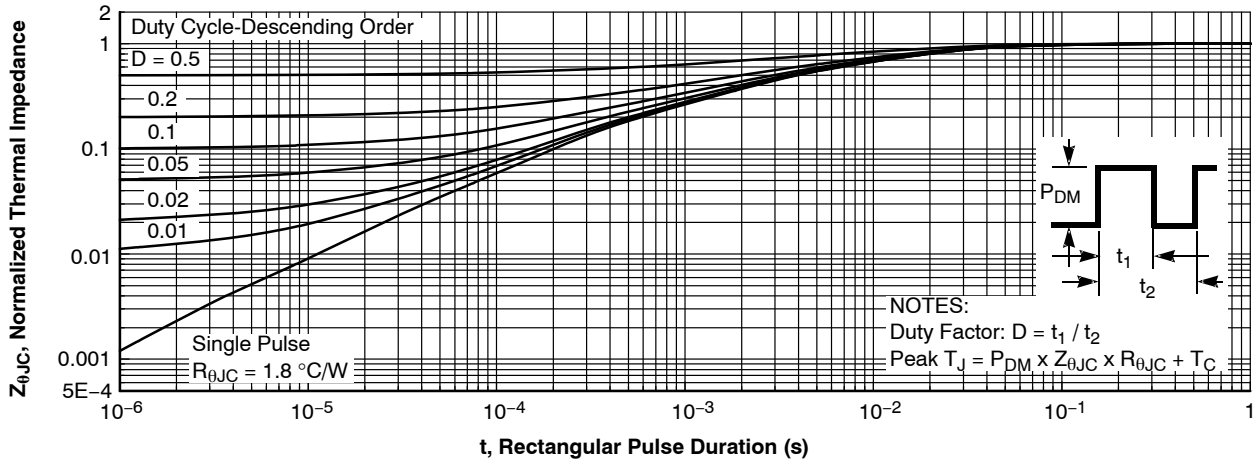



**Figure 13. Transient Thermal Response Curve**

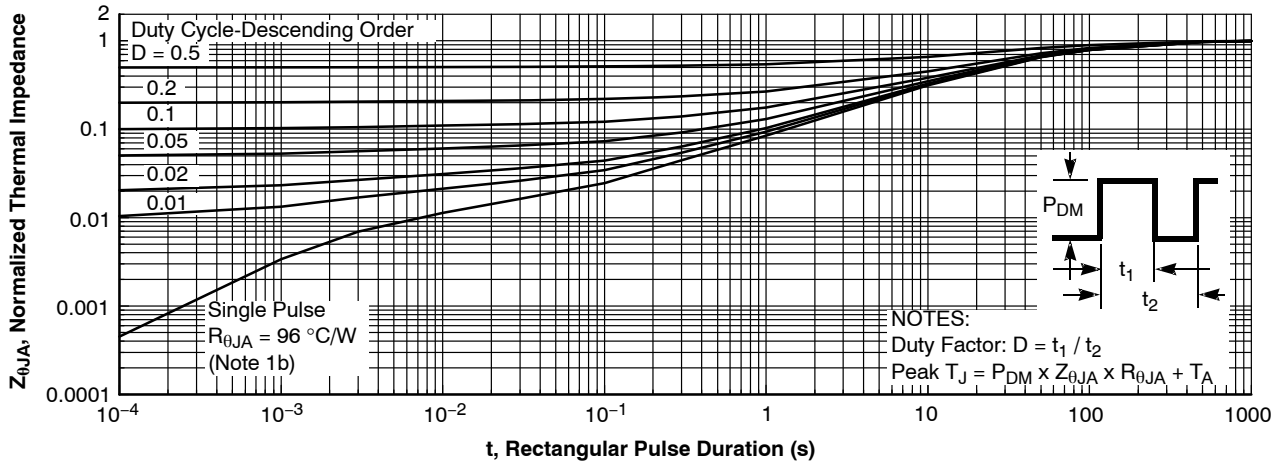
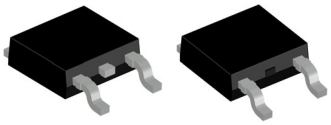
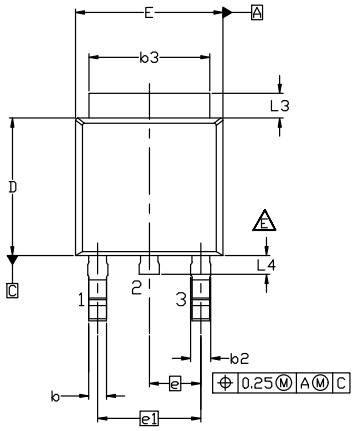



**Figure 14. Transient Thermal Response Curve**

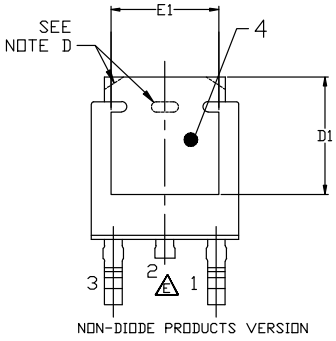


**DPAK3 6.10x6.54x2.29, 4.57P**
CASE 369AS
ISSUE B

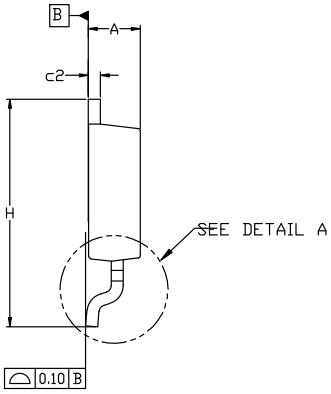
DATE 20 DEC 2023



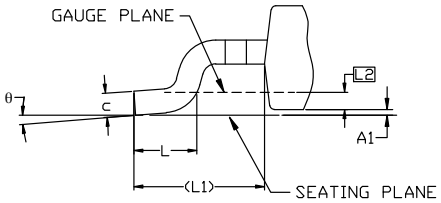

NON-DIODE PRODUCTS VERSION




NON-DIODE PRODUCTS VERSION

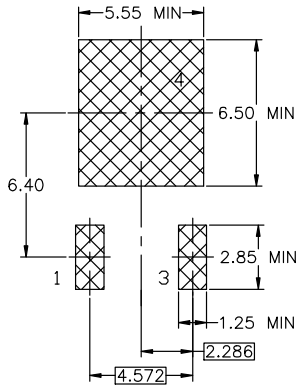



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.




DETAIL A
(ROTATED -90°)
SCALE: 12X

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 2.18 | 2.29 | 2.39 |
| A1 | 0.00 | – | 0.127 |
| b | 0.64 | 0.77 | 0.89 |
| b2 | 0.76 | 0.95 | 1.14 |
| b3 | 5.21 | 5.34 | 5.46 |
| c | 0.45 | 0.53 | 0.61 |
| c2 | 0.45 | 0.52 | 0.58 |
| D | 5.97 | 6.10 | 6.22 |
| D1 | 5.21 | --- | --- |
| E | 6.35 | 6.54 | 6.73 |
| E1 | 4.32 | --- | --- |
| e | 2.286 BSC | | |
| e1 | 4.572 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | 1.08 | 1.27 |
| L4 | --- | --- | 1.02 |
| θ | 0° | --- | 10° |




LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***


*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON13810G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **DPAK3 6.10x6.54x2.29, 4.57P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales