

# MOSFET – N-Channel, POWERTRENCH®

60 V, 50 A, 12.3 mΩ

**FDD5353**

## General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

## Features

- Max  $R_{DS(on)}$  = 12.3 mΩ at  $V_{GS} = 10$  V,  $I_D = 10.7$  A
- Max  $R_{DS(on)}$  = 15.4 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 9.5$  A
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and RoHS Compliant

## Applications

- Inverter
- Synchronous Rectifier
- Primary Switch

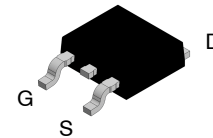
## MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current –Continuous $T_C = 25^\circ\text{C}$ –Continuous $T_A = 25^\circ\text{C}$ (Note 1a) –Pulsed	50 11.5 100	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	253	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	69 3.1	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+150$	$^\circ\text{C}$

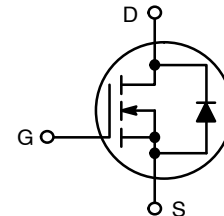
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Maximum Resistance, Junction to Case	1.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Resistance, Junction to Ambient (Note 1a)	40	

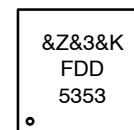


DPAK3  
CASE 369AS



N-Channel MOSFET

## MARKING DIAGRAM



&Z = Assembly Plant Code  
 &3 = Date Code (Year & Week)  
 &K = 2 Digit Lot Run Traceability Code  
 FDD5353 = Specific Device Code

## ORDERING INFORMATION

Device	Package	Shipping†
FDD5353	DPAK3	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://BRD8011/D).

# FDD5353

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise d)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 $\mu$ A, V <sub>GS</sub> = 0 V	60	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 $\mu$ A, referenced to 25°C	–	77	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 48 V	–	–	1	$\mu$ A
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = $\pm$ 20 V, V <sub>DS</sub> = 0 V	–	–	$\pm$ 100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 $\mu$ A	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 $\mu$ A, referenced to 25°C	–	–8	–	mV/°C
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10.7 A	–	10.1	12.3	m $\Omega$
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.5 A	–	12.1	15.4	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10.7 A, T <sub>J</sub> = 125°C	–	16.7	20.3	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 5 V, I <sub>D</sub> = 10.7 A	–	41	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	2420	3215	pF
C <sub>oss</sub>	Output Capacitance		–	215	285	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	120	180	pF
R <sub>g</sub>	Gate Resistance	f = 1 MHz	–	1.7	–	$\Omega$

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 10.7 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 $\Omega$	–	11	20	ns
t <sub>r</sub>	Rise Time		–	6	11	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	36	58	ns
t <sub>f</sub>	Fall Time		–	4	10	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V V <sub>DD</sub> = 30 V, I <sub>D</sub> = 10.7 A	–	46	65	nC
		V <sub>GS</sub> = 0 V to 4.5 V V <sub>DD</sub> = 30 V, I <sub>D</sub> = 10.7 A	–	23	32	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 10.7 A	–	7	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 10.7 A	–	9	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

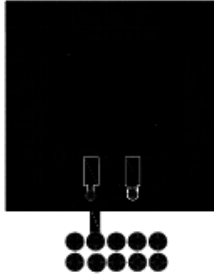
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10.7 A (Note 2)	–	0.8	1.3	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.6 A (Note 2)	–	0.7	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 10.7 A, di/dt = 100 A/ $\mu$ s	–	28	45	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	21	34	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## FDD5353

### NOTES:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



- a) 40 °C/W when mounted on  
a 1 in² pad of 2 oz copper.



- b) 96 °C/W when mounted on  
a minimum pad.

2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
3.  $E_{AS}$  of 253 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3$  mH,  $I_{AS} = 13$  A,  $V_{DD} = 60$  V,  $V_{GS} = 10$  V. 100% test at  $L = 0.1$  mH,  $I_{AS} = 41$  A.

## TYPICAL CHARACTERISTICS

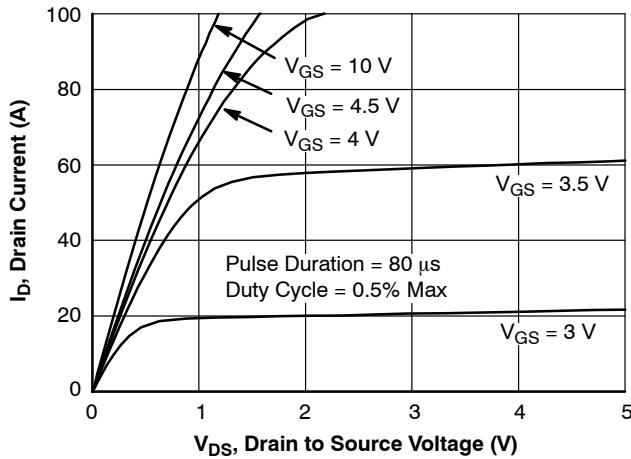
(T<sub>J</sub> = 25°C unless otherwise noted)

Figure 1. On-Region Characteristics

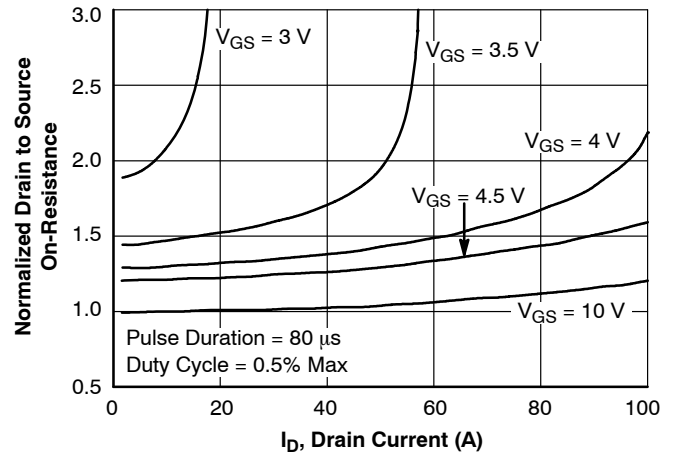


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

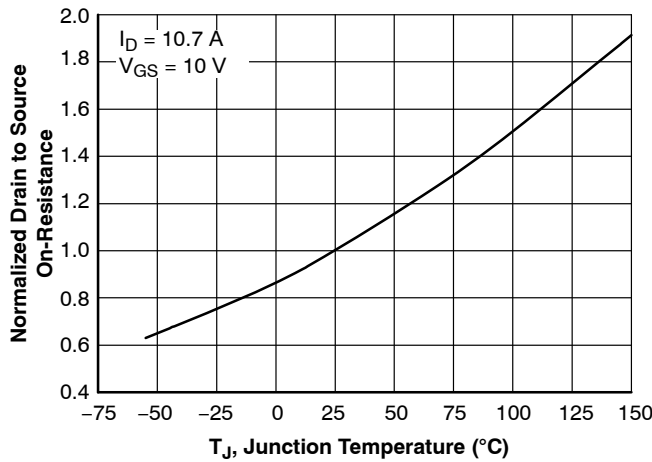


Figure 3. Normalized On-Resistance vs Junction Temperature

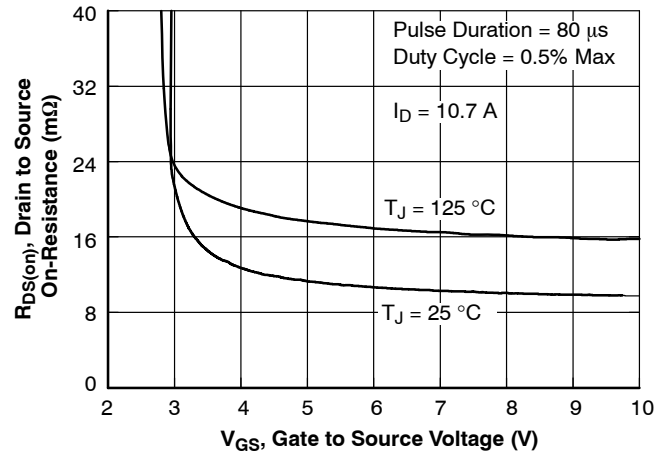


Figure 4. On-Resistance vs Gate to Source Voltage

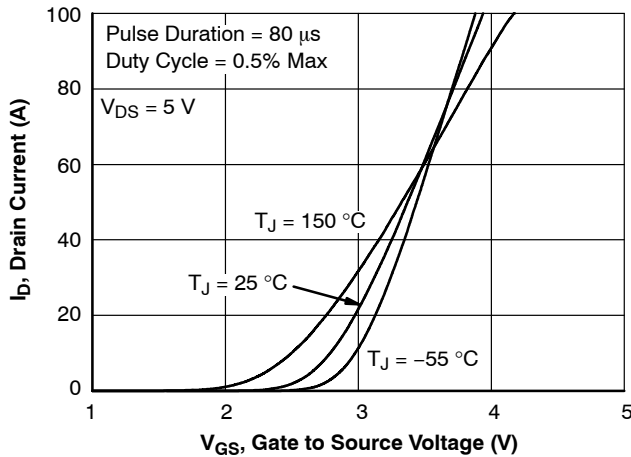


Figure 5. Transfer Characteristics

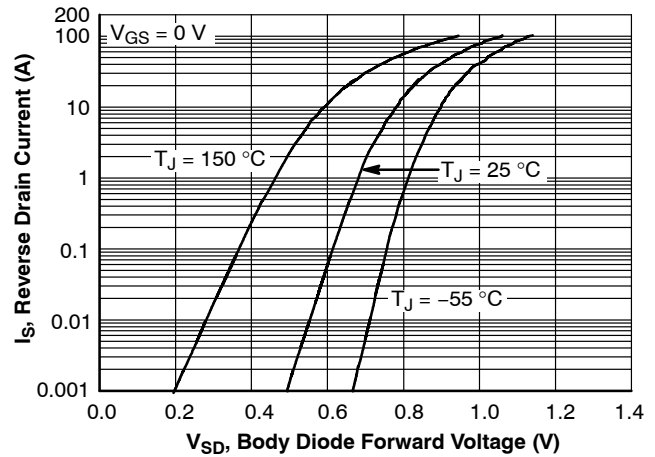


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## TYPICAL CHARACTERISTICS (continued)

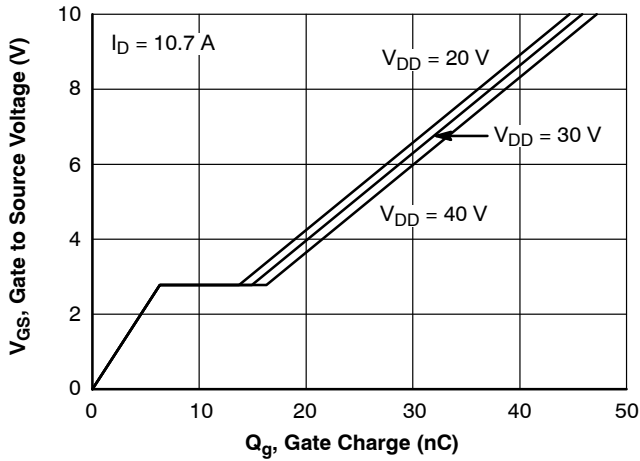
(T<sub>J</sub> = 25°C unless otherwise noted)

Figure 7. Gate Charge Characteristics

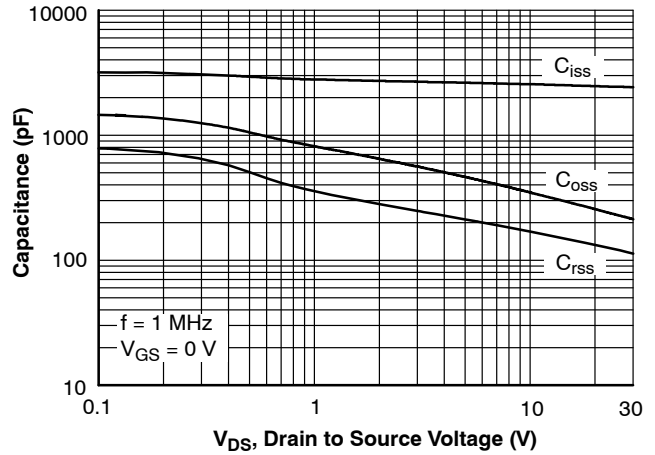


Figure 8. Capacitance vs Drain to Source Voltage

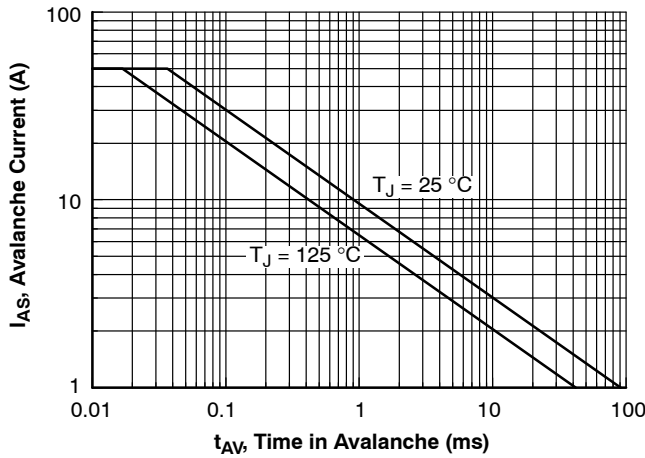


Figure 9. Unclamped Inductive Switching Capability

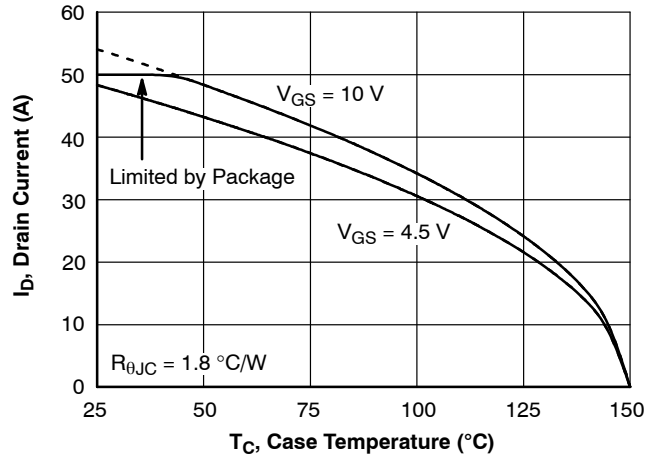


Figure 10. Maximum Continuous Drain Current vs Case Temperature

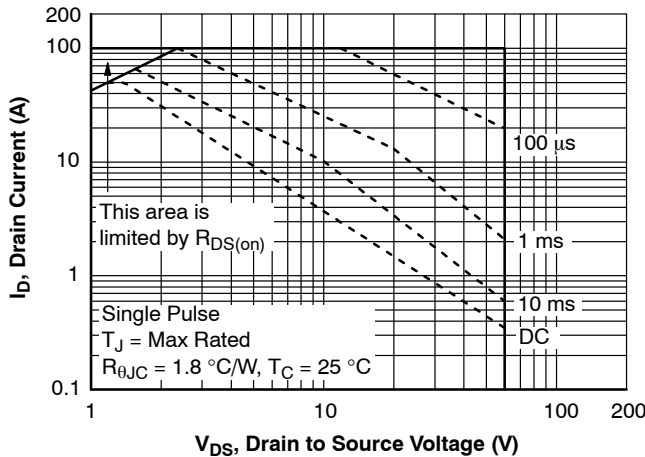


Figure 11. Forward Bias Safe Operating Area

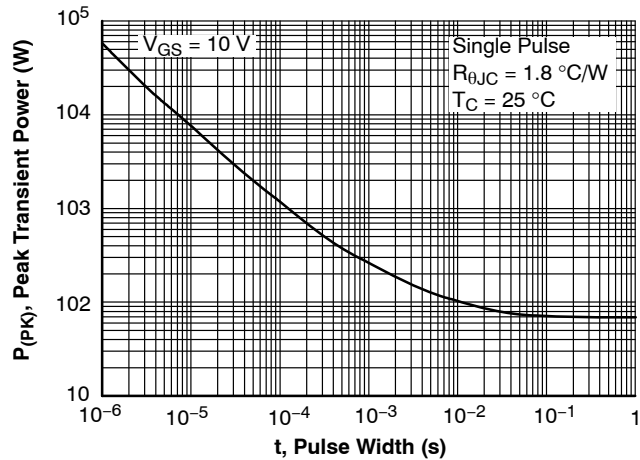


Figure 12. Single Pulse Maximum Power Dissipation

## TYPICAL CHARACTERISTICS

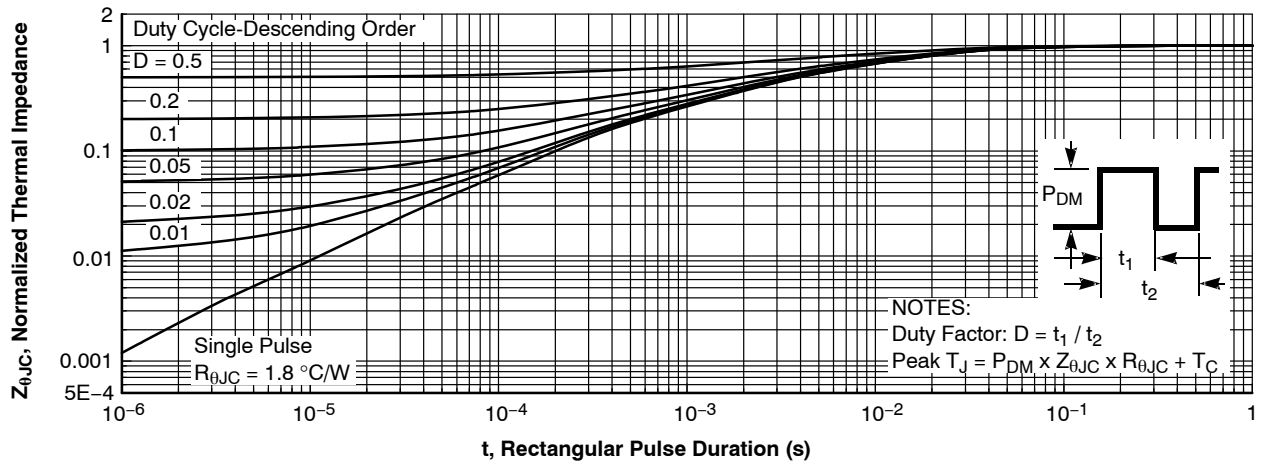
(T<sub>J</sub> = 25°C unless otherwise noted)

Figure 13. Transient Thermal Response Curve

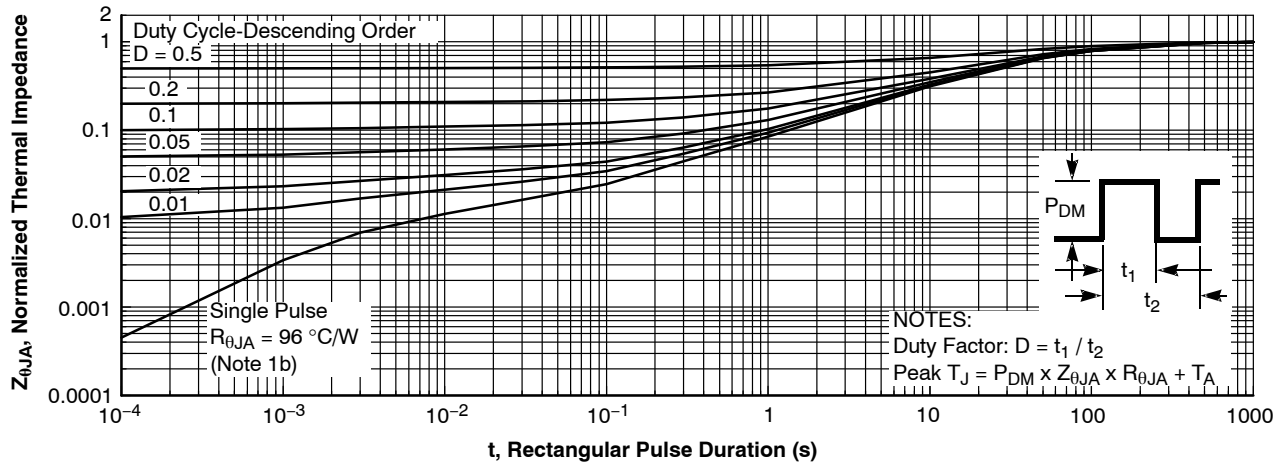
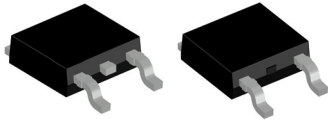
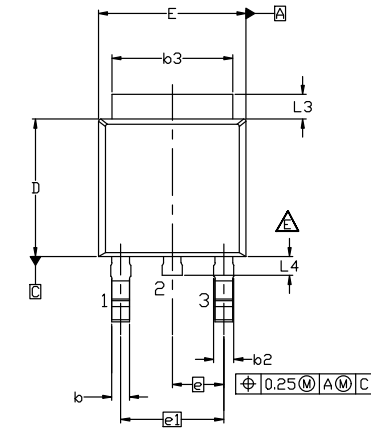


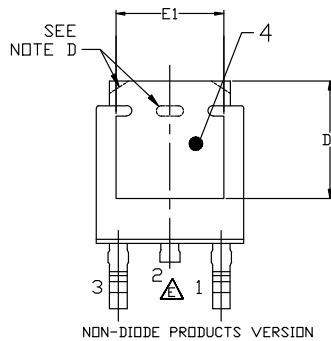
Figure 14. Transient Thermal Response Curve


**DPAK3 6.10x6.54x2.29, 4.57P**  
**CASE 369AS**  
**ISSUE B**

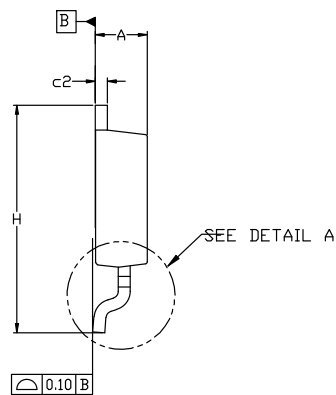
DATE 20 DEC 2023



NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

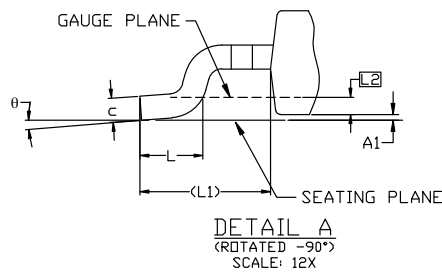
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.

D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

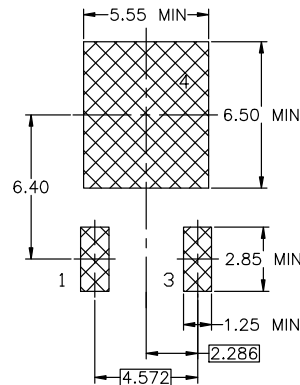
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.

F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

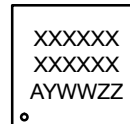
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TD228P991X239-3N.



DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°


**LAND PATTERN RECOMMENDATION**

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***


\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

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