

# N-Channel Enhancement Mode Field Effect Transistor

## FDC653N

### General Description

This N-Channel enhancement mode power field effect transistor is produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 5.0 A, 30 V  
 $R_{DS(ON)} = 0.035 \Omega @ V_{GS} = 10 \text{ V}$   
 $R_{DS(ON)} = 0.055 \Omega @ V_{GS} = 4.5 \text{ V}$
- Proprietary SUPERSOT™-6 Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities.
- High Density Cell Design for Extremely Low  $R_{DS(ON)}$ .
- Exceptional On-Resistance and Maximum DC Current Capability.
- This Device is Pb-Free and Halogen Free

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

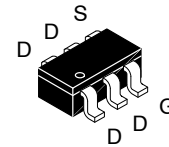
Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage - Continuous	$\pm 20$	V
$I_D$	Drain Current	- Continuous (Note 1a)	5
		- Pulsed	15
$P_D$	Maximum Power Dissipation	(Note 1a)	1.6
		(Note 1b)	0.8
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

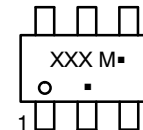
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C/W}$

$V_{DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	0.035 $\Omega @ 10 \text{ V}$	5.0 A
	0.055 $\Omega @ 4.5 \text{ V}$	



TSOT23 6-Lead  
 SUPERSOT™-6  
 CASE 419BL

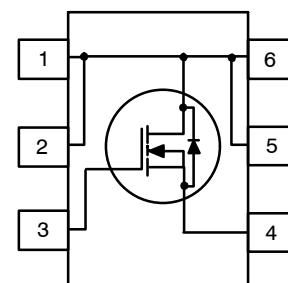
### MARKING DIAGRAM



XXX = Specific Device Code  
 M = Date Code  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

### PINOUT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# FDC653N

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	–	31	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V T <sub>J</sub> = 55°C	–	–	1 10	μA
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	–	–	100	nA
I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	V <sub>GS</sub> = –20 V, V <sub>DS</sub> = 0 V	–	–	–100	nA

### ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	1.7	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	–	–4.2	–	mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.2 A T <sub>J</sub> = 125°C	–	0.027 0.042 0.046	0.035 0.056 0.055	Ω
I <sub>D(on)</sub>	On–State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	8	–	–	A
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 A	–	6.2	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	–	350	–	pF
C <sub>oss</sub>	Output Capacitance		–	220	–	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	80	–	pF

### SWITCHING CHARACTERISTICS (Note 2)

t <sub>d(on)</sub>	Turn–On Delay Time	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 1 A, V <sub>GS</sub> = 4.5 V, R <sub>GEN</sub> = 6 Ω	–	7.5	15	ns
t <sub>r</sub>	Turn–On Rise Time		–	12	25	ns
t <sub>d(off)</sub>	Turn–Off Delay Time		–	13	25	ns
t <sub>f</sub>	Turn–Off Fall Time		–	6	15	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 5 A, V <sub>GS</sub> = 10 V	–	12	17	nC
Q <sub>gs</sub>	Gate–Source Charge		–	2.1	–	nC
Q <sub>gd</sub>	Gate–Drain Charge		–	2.6	–	nC

### DRAIN–SOURCE DIODE CHARACTERISTICS

I <sub>S</sub>	Continuous Source Diode Current	–	–	1.3	A	
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A (Note 2) T <sub>J</sub> = 125°C	–	0.75 0.6	1.2 1.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R<sub>θJA</sub> is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.
  - 78°C/W when mounted on a minimum on 1 in<sup>2</sup> pad of 2oz Cu in FR–4 board.
  - 156°C/W when mounted on a minimum pad of 2oz Cu in FR–4 board.
- Pulse Test: Pulse Width ≤ 300 μs, Duty cycle ≤ 2.0 %.

TYPICAL CHARACTERISTICS

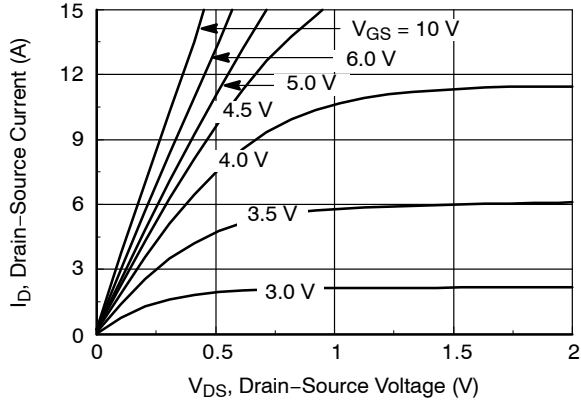


Figure 1. On-Region Characteristics

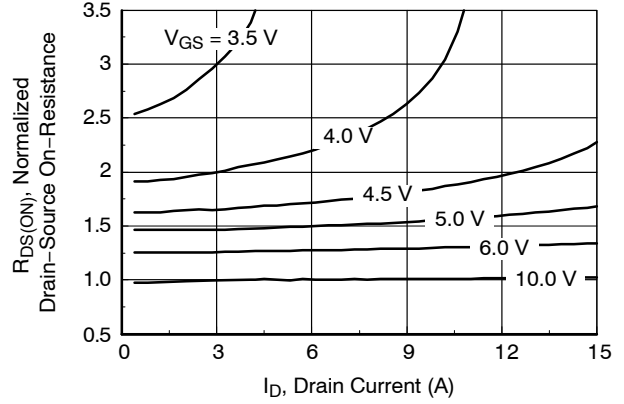


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

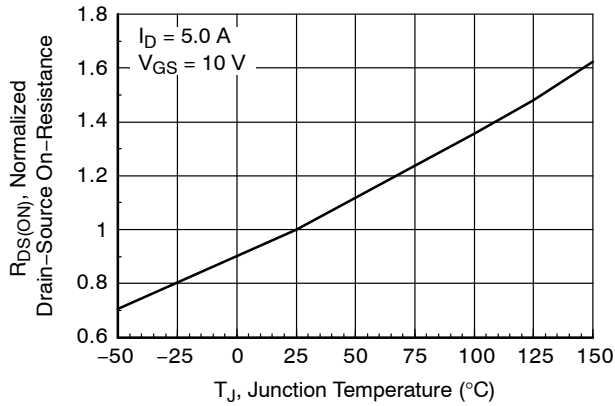


Figure 3. On-Resistance Variation with Temperature

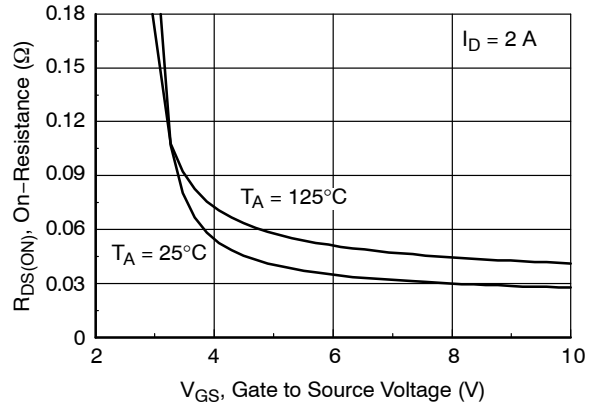


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

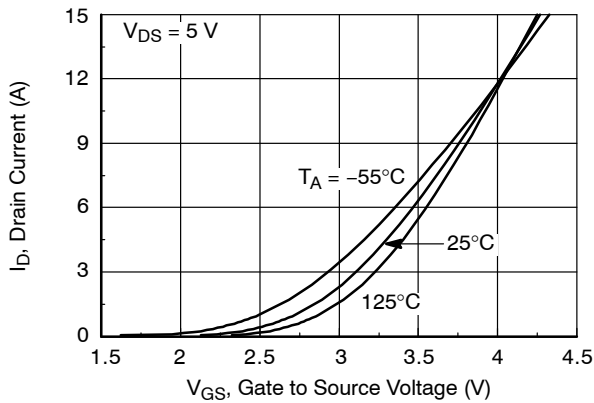


Figure 5. Transfer Characteristics

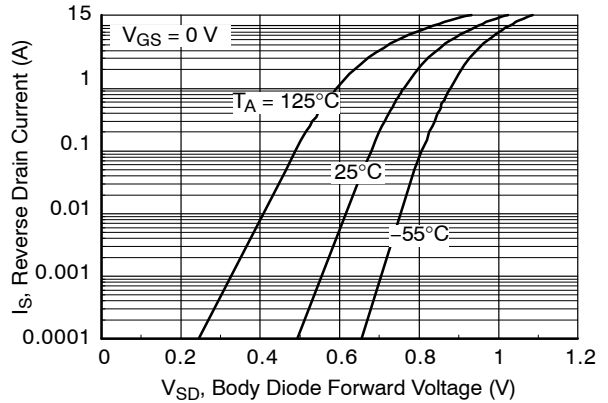


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL ELECTRICAL CHARACTERISTICS (continued)

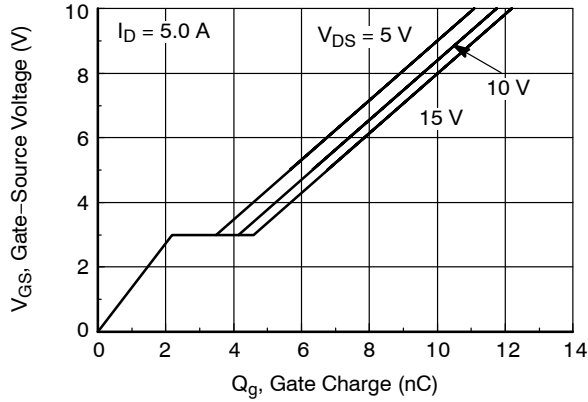


Figure 7. Gate Charge Characteristics

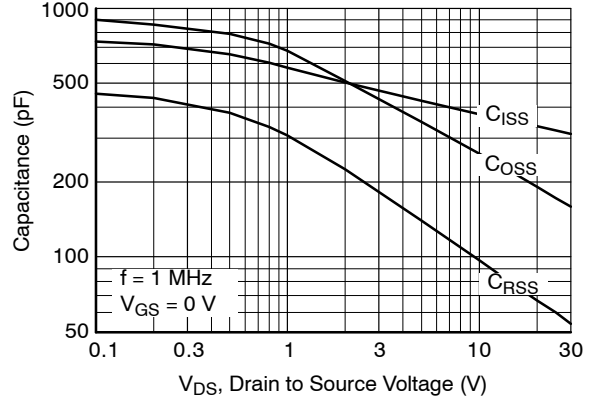


Figure 8. Capacitance Characteristics

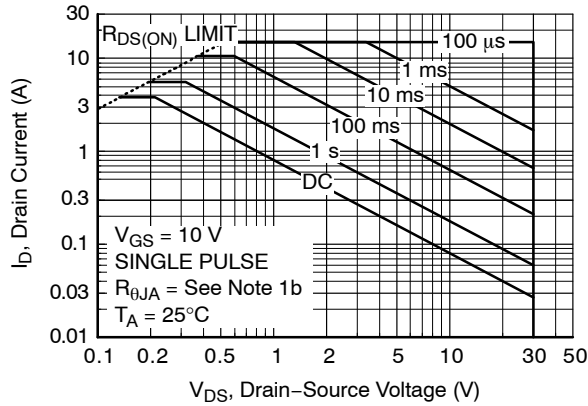


Figure 9. Maximum Safe Operating Area

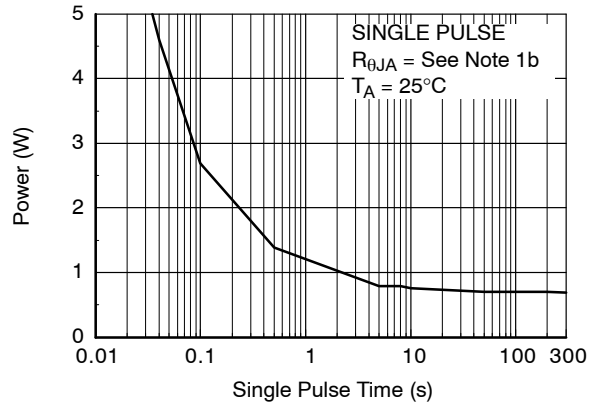


Figure 10. Single Pulse Maximum Power Dissipation

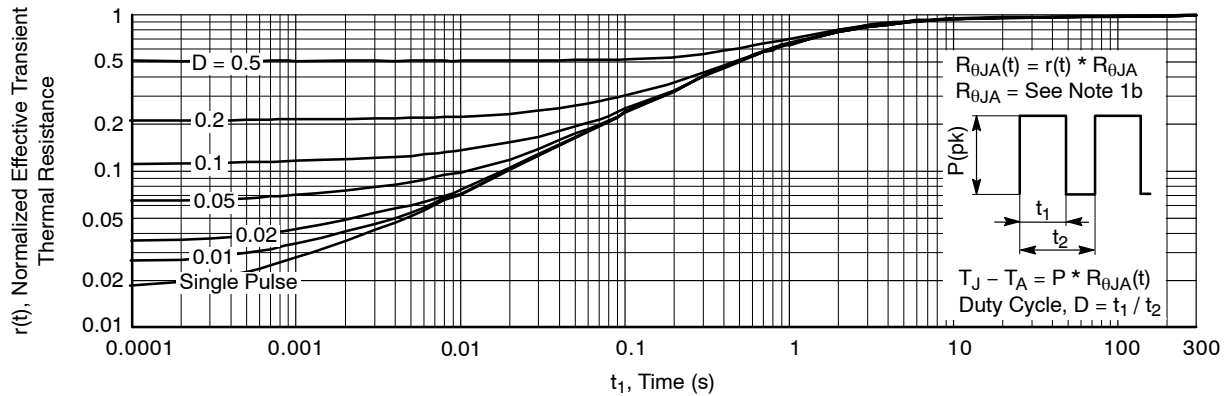


Figure 11. Transient Thermal Response Curve

(Note: Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.)

# FDC653N

## ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping <sup>†</sup>
FDC653N	.653	TSOT23 6-Lead (Pb-free)	7"	8 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

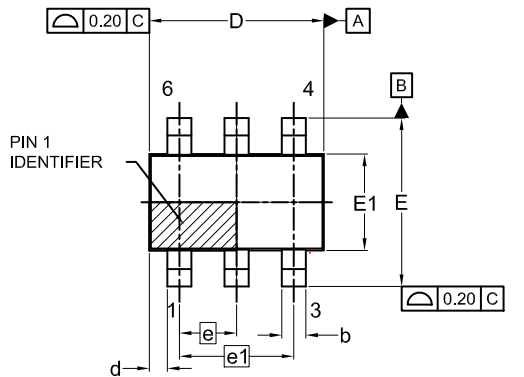
SUPERSOT is a trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.



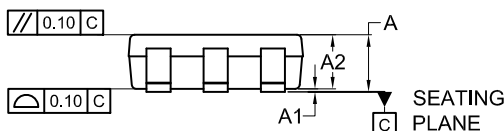
1  
SCALE 2:1

TSOT23 6-Lead  
CASE 419BL  
ISSUE A

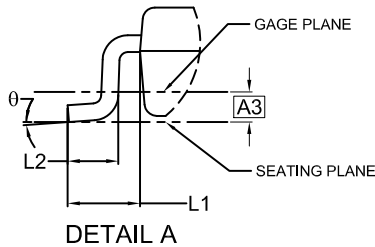
DATE 31 AUG 2020



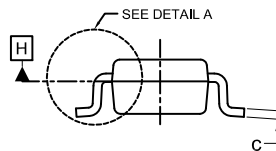
TOP VIEW



FRONT VIEW

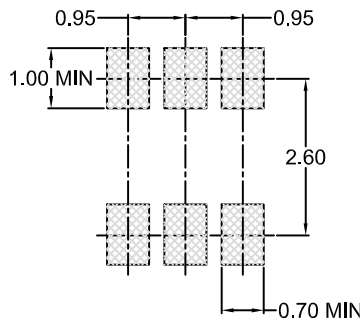


DETAIL A



SIDE VIEW

SYMM  
⌀



LAND PATTERN  
RECOMMENDATION

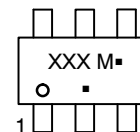
\*FOR ADDITIONAL INFORMATION ON OUR  
Pb-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⌀	0°	--	10°

GENERIC  
MARKING DIAGRAM\*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON83292G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)