

# MOSFET – N-Channel, Logic Level, **POWERTRENCH**<sup>®</sup> 60 V, 4 A, 60 mΩ

## FDC5661N

### Features

- $R_{DS(on)} = 47\text{ m}\Omega$  at  $V_{GS} = 10\text{ V}$ ,  $I_D = 4.3\text{ A}$
- $R_{DS(on)} = 60\text{ m}\Omega$  at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 4\text{ A}$
- Typ  $Q_g(TOT) = 14.5\text{ nC}$  at  $V_{GS} = 10\text{ V}$
- Low Miller Charge
- UIS Capability
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

### Applications

- DC/DC Converter
- Motor Drives

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current Continuous ( $V_{GS} = 10\text{ V}$ )	$I_D$	4.3	A
Pulsed		20	
Single Pulse Avalanche Energy (Note 1)	$E_{AS}$	81	mJ
Power Dissipation	$P_D$	1.6	W
Operating and Storage Temperature	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Thermal Resistance Junction to Case	$R_{\theta JC}$	30	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient TO-263, 1in <sup>2</sup> Copper Pad Area	$R_{\theta JA}$	78	$^\circ\text{C/W}$

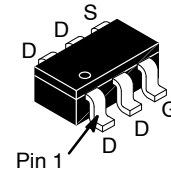
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $E_{AS}$  of 81 mJ is 100% test at  $L = 14\text{ mH}$ ,  $I_{AS} = 3.4\text{ A}$ , Starting  $T_J = 25^\circ\text{C}$ .



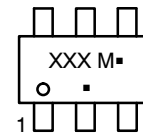
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TSOT23-6  
CASE 419BL

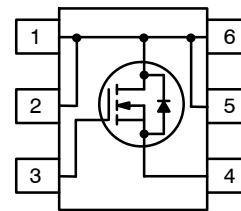
### MARKING DIAGRAM



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDC5661N

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain to Source Breakdown Voltage	$B_{VDSS}$	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	60	–	–	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	$\mu\text{A}$
			$T_A = 150^\circ\text{C}$	–	–	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20 \text{ V}$	–	–	$\pm 100$	nA

### ON CHARACTERISTICS

Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1	2.0	3	V
Drain to Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 4.3 \text{ A}$	–	38	47	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	–	46	60	
		$V_{GS} = 10 \text{ V}, I_D = 4.3 \text{ A}$	$T_J = 150^\circ\text{C}$	–	69	

### DYNAMIC CHARACTERISTICS

Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V},$ $f = 1 \text{ MHz}$	–	763	–	$\text{pF}$
Output Capacitance	$C_{oss}$		–	68	–	
Reverse Transfer Capacitance	$C_{rss}$		–	36	–	
Gate Resistance	$R_G$	$f = 1 \text{ MHz}$	–	2.6	–	$\Omega$
Total Gate Charge at 10 V	$Q_{g(TOT)}$	$V_{GS} = 0 \text{ to } 10 \text{ V}, V_{DD} = 30 \text{ V}, I_D = 4.3 \text{ A}$	–	14.5	19	nC
Gate to Source Gate Charge	$Q_{gs}$	$V_{DD} = 30 \text{ V}, I_D = 4.3 \text{ A}$	–	2.4	–	nC
Gate to Drain “Miller” Charge	$Q_{gd}$		–	2.9	–	nC

### SWITCHING CHARACTERISTICS

Turn-On Time	$t_{on}$	$V_{GS} = 10 \text{ V}, V_{DD} = 30 \text{ V},$ $I_D = 4.3 \text{ A}, R_{GS} = 6 \Omega,$	–	–	17.6	ns
Turn-On Delay Time	$t_{d(on)}$		–	7.2	–	ns
Rise Time	$t_r$		–	1.6	–	ns
Turn-Off Delay Time	$t_{d(off)}$		–	19.3	–	ns
Fall Time	$t_f$		–	3.1	–	ns
Turn-Off Time	$t_{off}$		–	–	36	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 4.3 \text{ A}$	–	0.8	1.25	V
		$I_{SD} = 2.1 \text{ A}$	–	0.8	1.0	
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 4.3 \text{ A}, dI_{SD}/dt = 100 \text{ A}/\mu\text{s}$	–	18.4	24	ns
Reverse Recovery Charge	$Q_{rr}$		–	10.0	13	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# FDC5661N

## TYPICAL CHARACTERISTICS

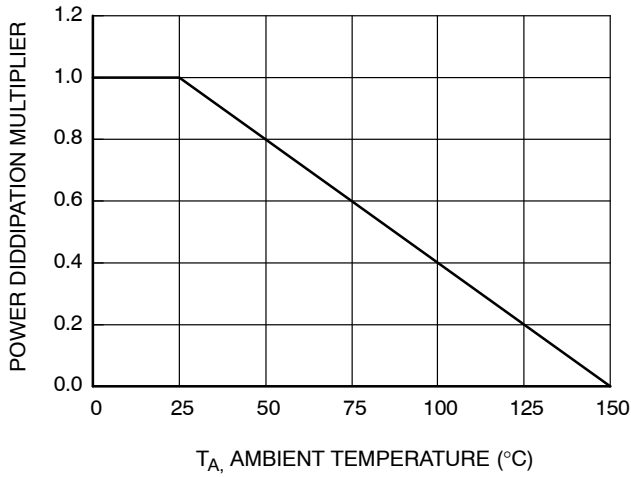


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

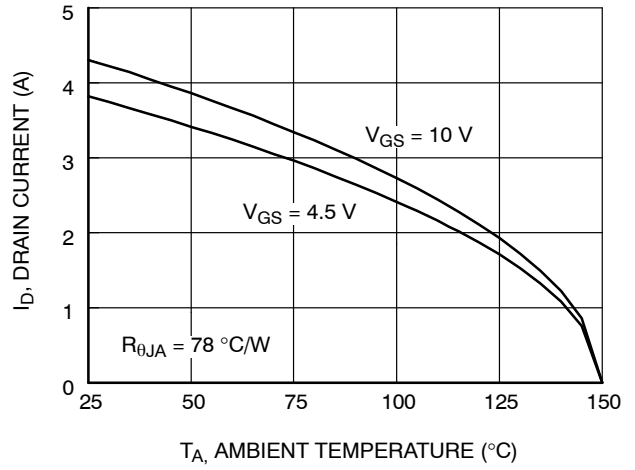


Figure 2. Maximum Continuous Drain Current vs. Ambient Temperature

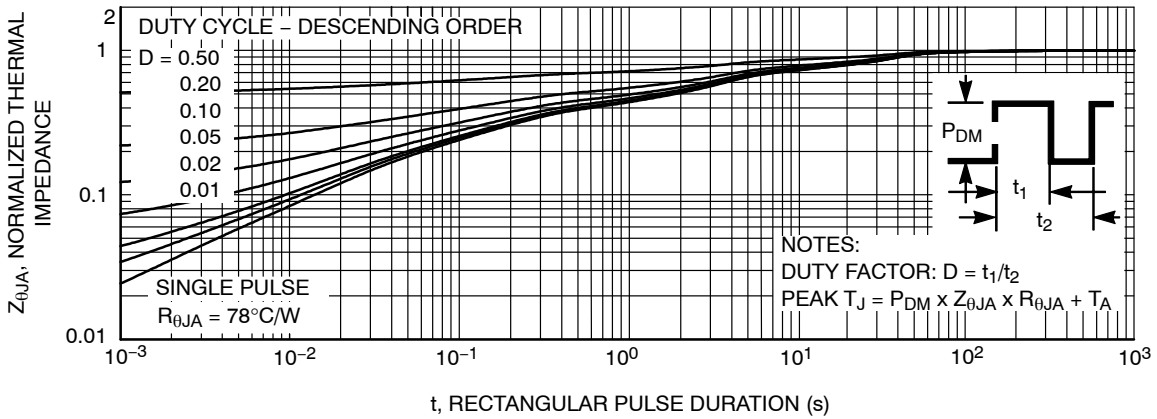


Figure 3. Normalized Maximum Transient Thermal Impedance

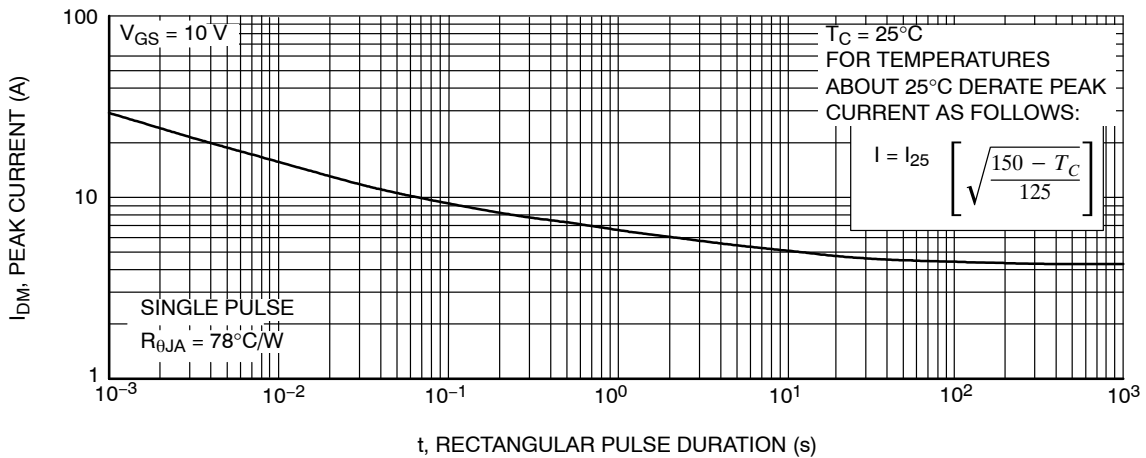


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

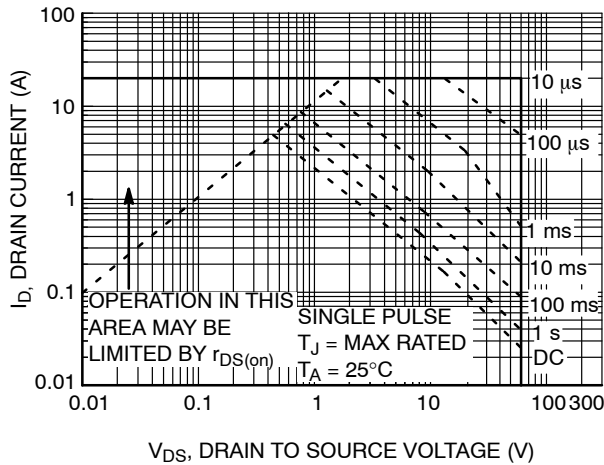


Figure 5. Forward Bias Safe Operating Area

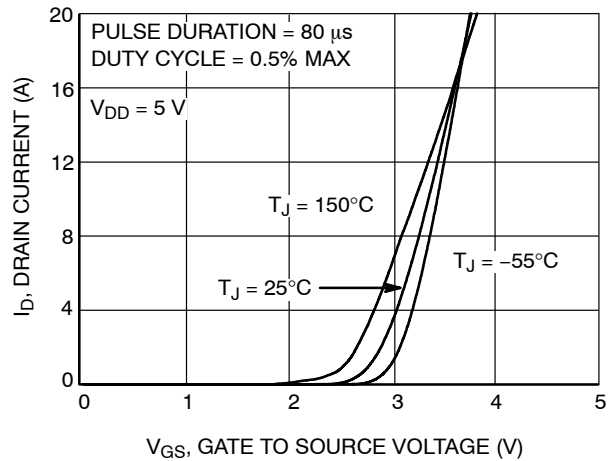


Figure 6. Transfer Characteristics

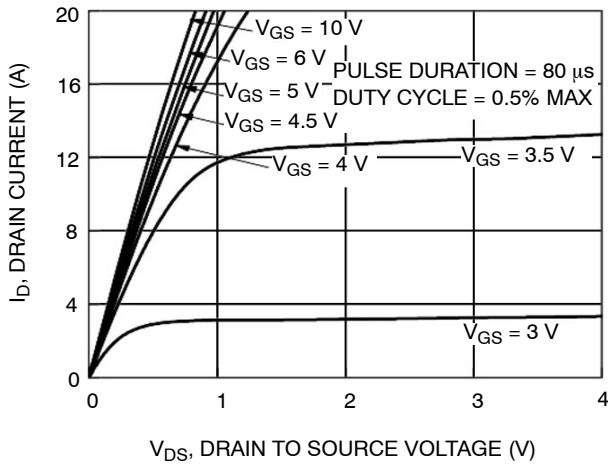


Figure 7. Saturation Characteristics

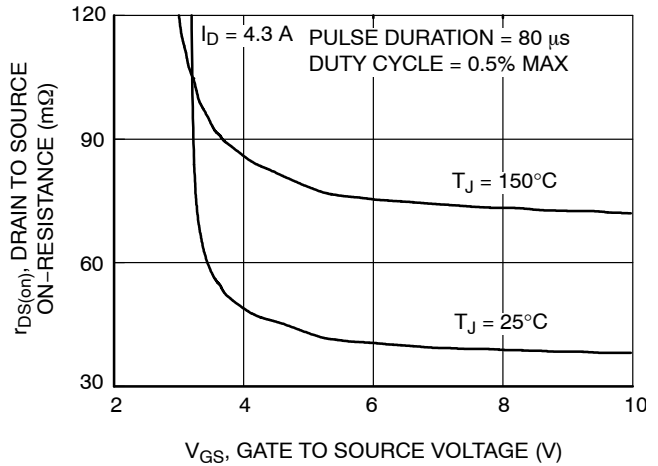


Figure 8. Drain to Source On-Resistance Variation vs. Gate to Source Voltage

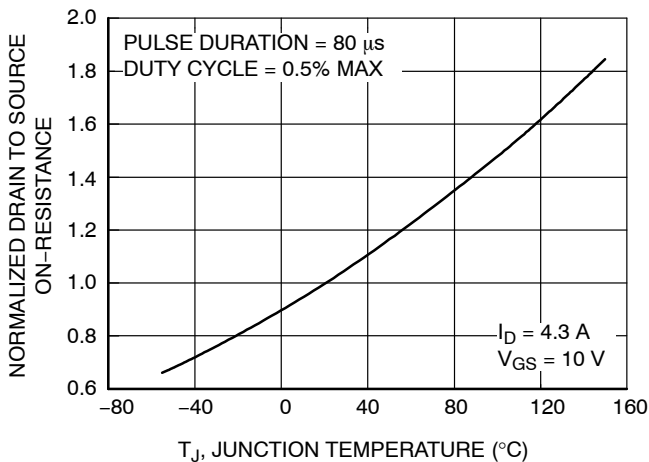


Figure 9. Normalized Drain to Source On Resistance vs. Junction Temperature

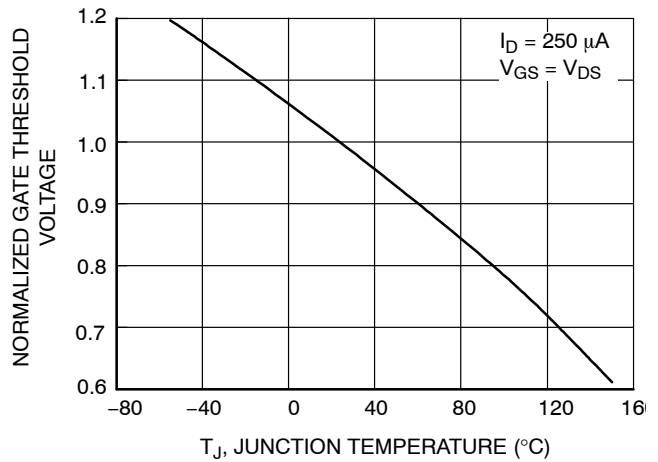
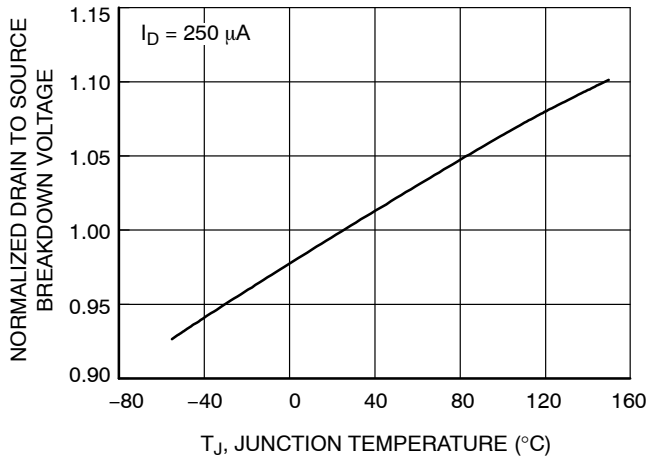


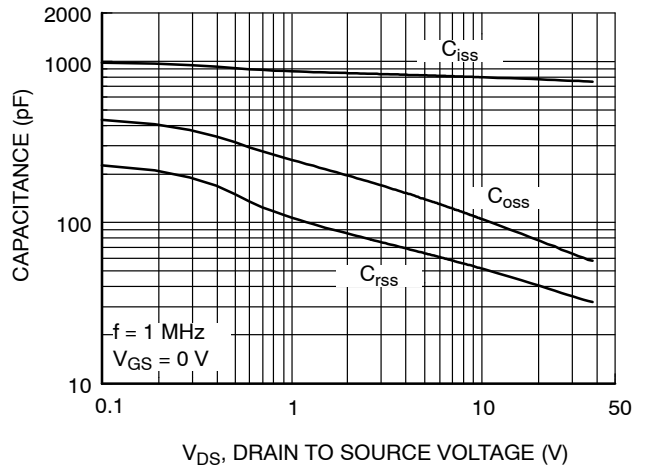
Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature

# FDC5661N

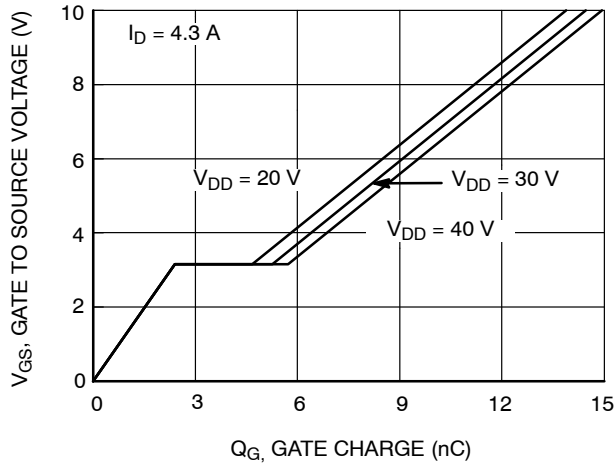
## TYPICAL CHARACTERISTICS (continued)



**Figure 11. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature**



**Figure 12. Capacitance vs. Drain to Source Voltage**



**Figure 13. Gate Charge vs. Gate to Source Voltage**

# FDC5661N

## ORDERING INFORMATION

Device Marking	Device	Package	Shipping†
.661N	FDC5661N	TSOT23-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

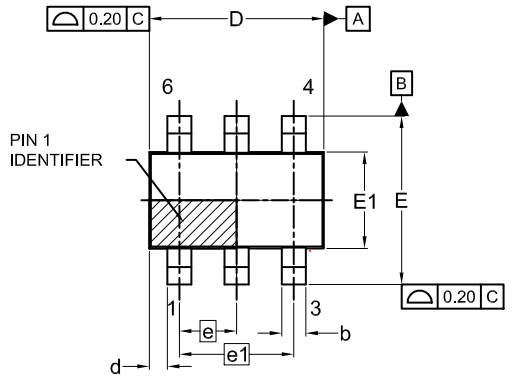
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1  
SCALE 2:1

### TSOT23 6-Lead CASE 419BL ISSUE A

DATE 31 AUG 2020



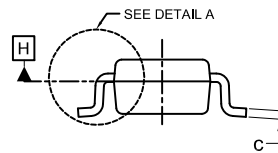
TOP VIEW



FRONT VIEW

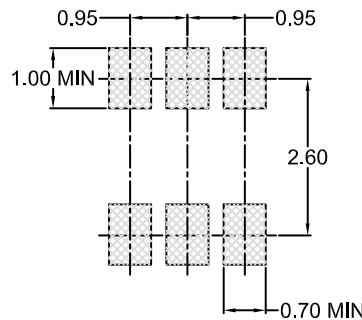


DETAIL A



SIDE VIEW

SYMM  
⌀



LAND PATTERN  
RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR  
Pb-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⌀	0°	--	10°

#### GENERIC MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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