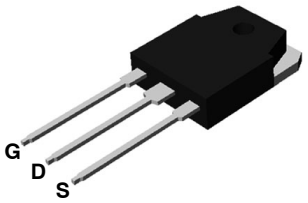
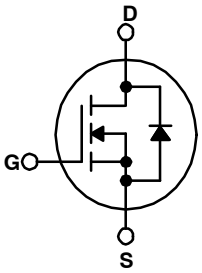
MOSFET – N-Channel, UniFET™

500 V, 28 A, 155 mΩ

FDA28N50



TO−3P−3L
CASE 340BZ



Description

UniFET MOSFET is **onsemi**'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)}$ = 122 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 14 A
- Low Gate Charge (Typ. 80 nC)
- Low Crss (Typ. 42 pF)
- 100% Avalanche Tested
- This Device is Pb−Free Halide, Free and RoHS Compliant

Applications

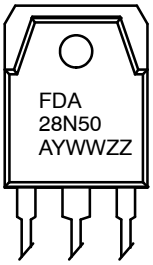
- PDP TV
- Uninterruptible Power Supply
- AC−DC Power Supply

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	±30	V
I_D	Drain Current – Continuous (T_C = 25°C) – Continuous (T_C = 100°C)	 28 17	A
I_{DM}	Drain Current – Pulsed (Note 1)	112	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	2391	mJ
I_{AR}	Avalanche Current (Note 1)	28	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	31	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5	V/ns
P_D	Power Dissipation – (T_C = 25°C) – Derate Above 25°C	 310 2.5	 W W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	−55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



FDA28N50	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year and Week)
ZZ	= Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping†
FDA28N50	TO−3P−3L (Pb−Free)	450 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_J = 25°C	500	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.59	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 400 V, T_C = 125°C	–	–	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 14 A	–	0.122	0.155	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 14 A	–	34	–	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	3866	5140	pF
C_{oss}	Output Capacitance		–	576	766	pF
C_{rss}	Reverse Transfer Capacitance		–	42	63	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 28 A, V_{GS} = 10 V (Note 4)	–	80	105	nC
Q_{gs}	Gate to Source Gate Charge		–	21	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	32	–	nC
Switching Characteristics						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 250 V, I_D = 28 A, V_{GS} = 10 V R_G = 25 Ω (Note 4)	–	56	122	ns
t_r	Turn−On Rise Time		–	126	262	ns
$t_{d(off)}$	Turn−Off Delay Time		–	210	430	ns
t_f	Turn−Off Fall Time		–	110	230	ns
Drain−Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	28	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	112	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 20 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 20 A, dI_F/dt = 100 A/μs	–	530	–	ns
Q_{rr}	Reverse Recovery Charge		–	8	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:
1. Repetitive Rating: Pulse−width limited by maximum junction temperature.
2. L = 6.1 mH, I_{AS} = 28 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 28 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature typical Characteristics.

TYPICAL CHARACTERISTICS

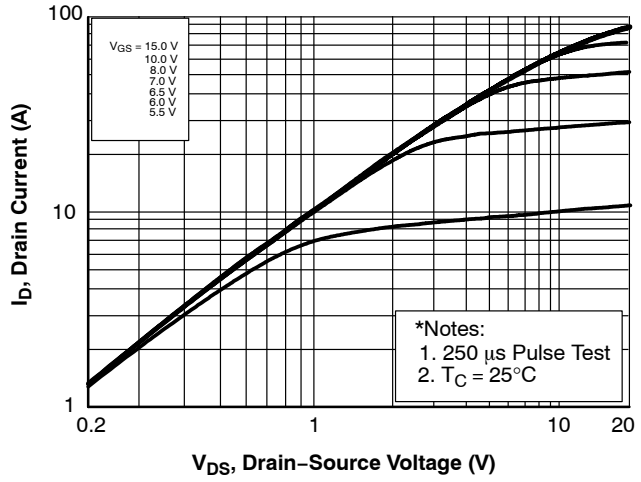


Figure 1. On−Region Characteristics

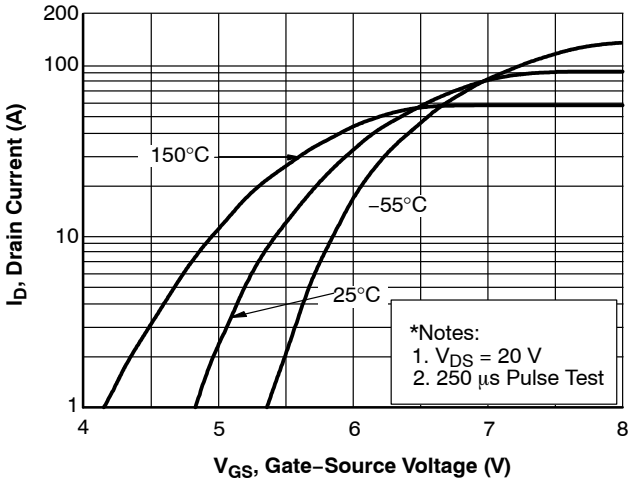


Figure 2. Transfer Characteristics

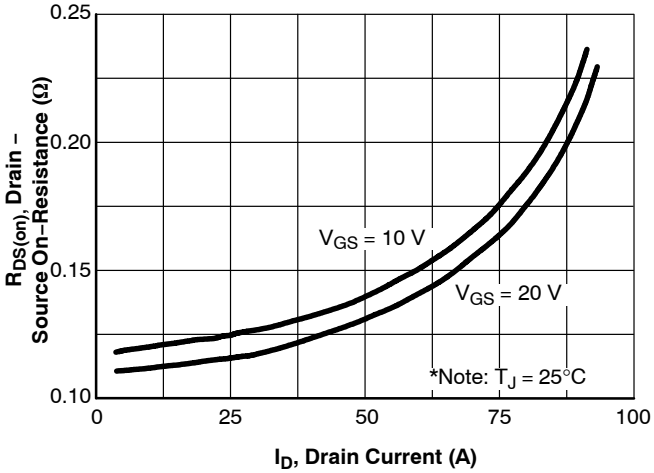


Figure 3. On−Resistance Variation vs Drain Current and Gate Voltage

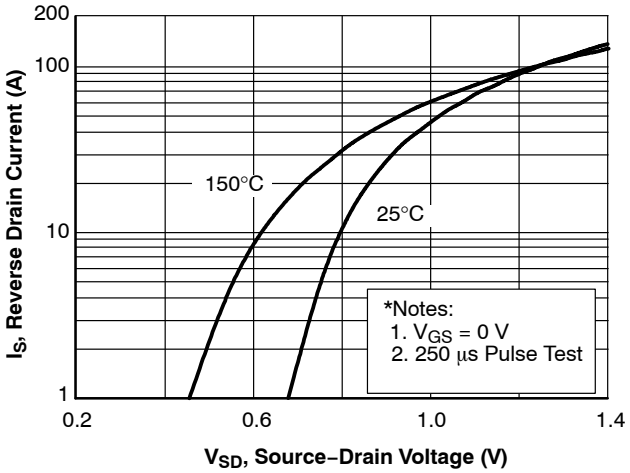


Figure 4. Body Diode Forward Voltage Variation vs Source Current and Temperature

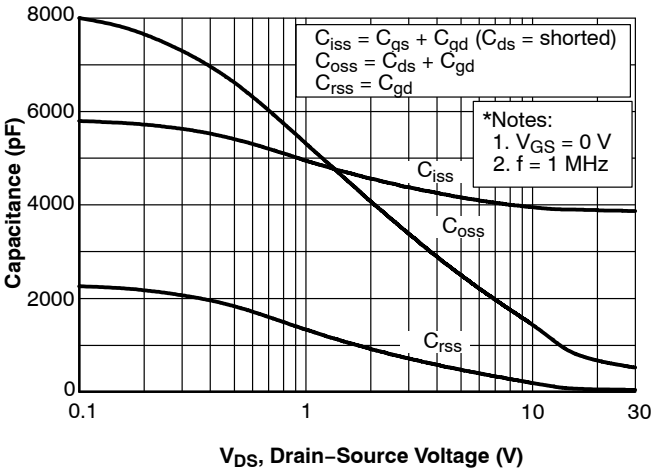


Figure 5. Capacitance Characteristics

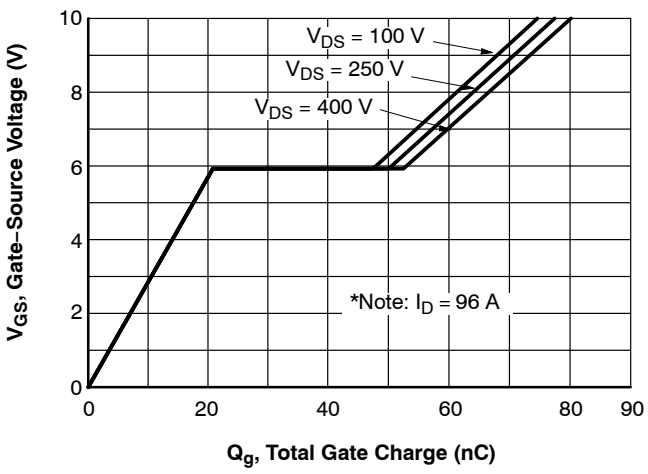


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

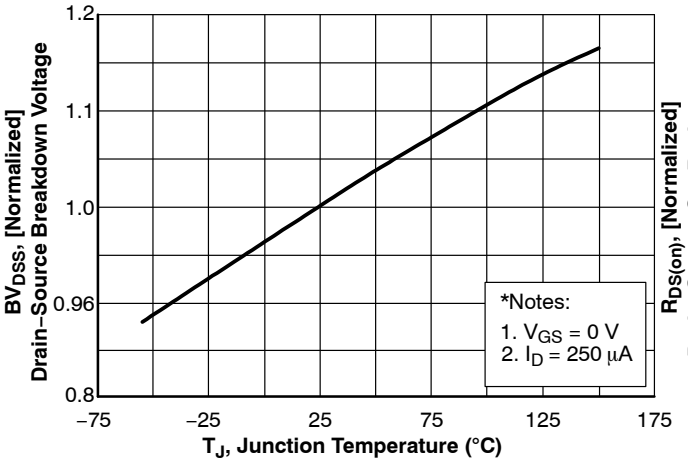


Figure 7. Breakdown Voltage Variation vs Temperature

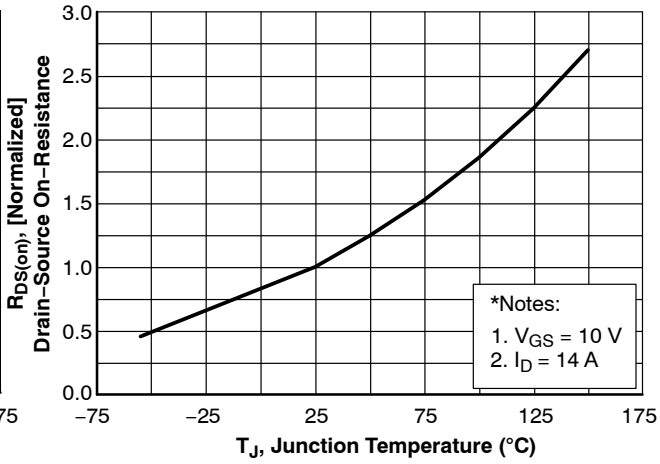


Figure 8. On−Resistance Variation vs Temperature

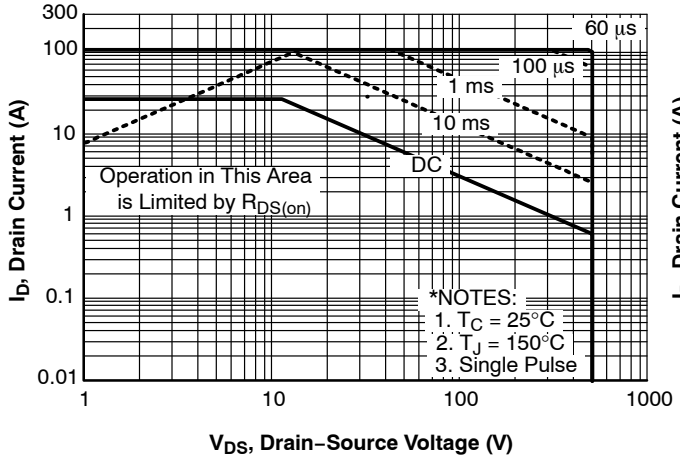


Figure 9. Maximum Safe Operating Area

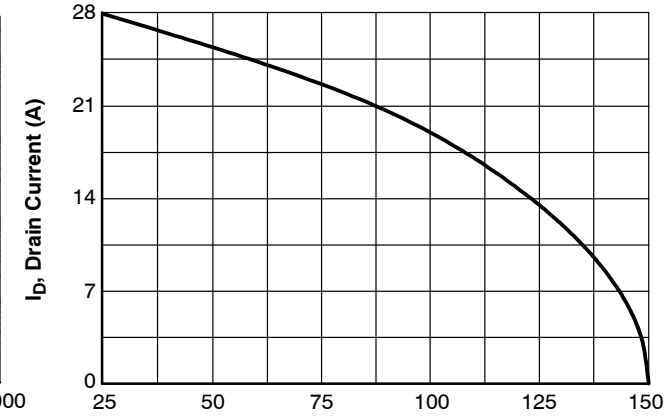


Figure 10. Maximum Drain Current vs. Case Temperature

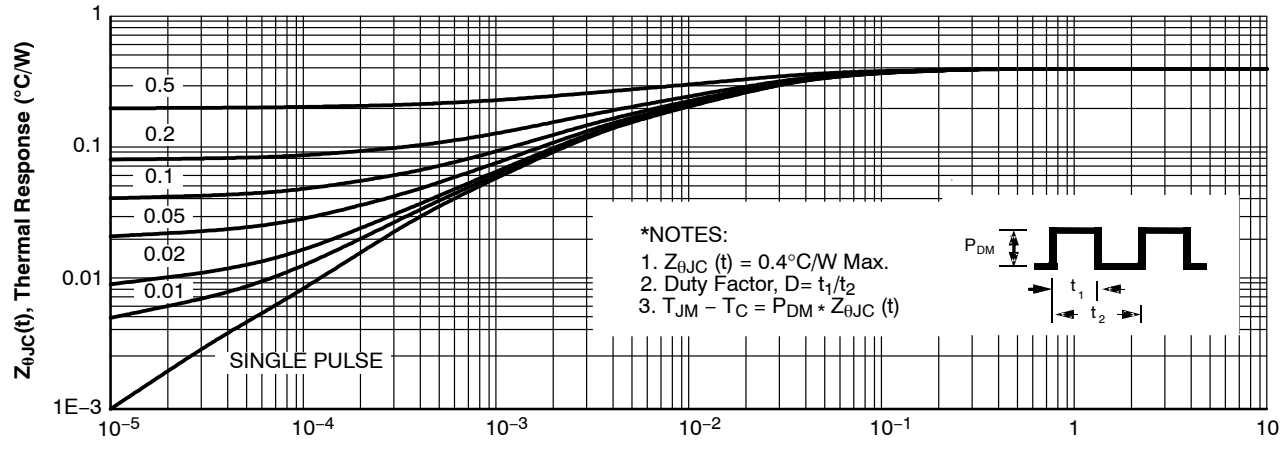


Figure 11. Transient Thermal Response Curve

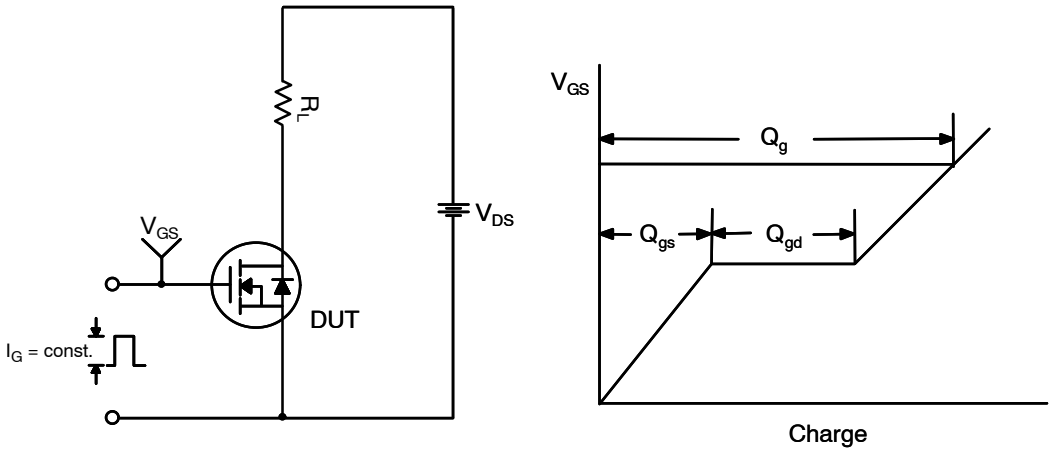


Figure 12. Gate Charge Test Circuit & Waveform

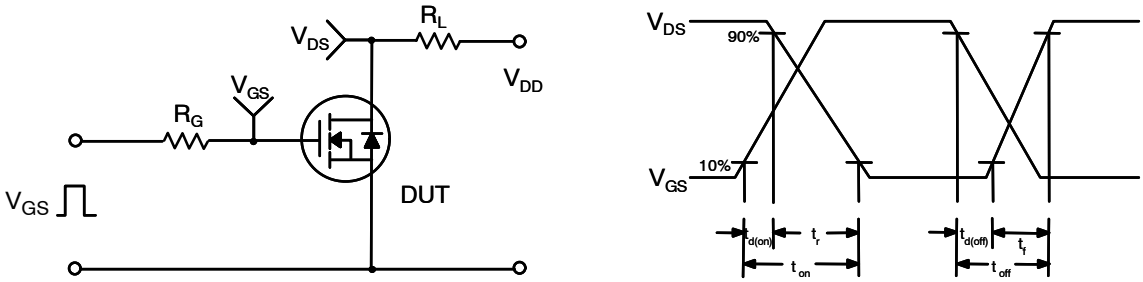


Figure 13. Resistive Switching Test Circuit & Waveforms

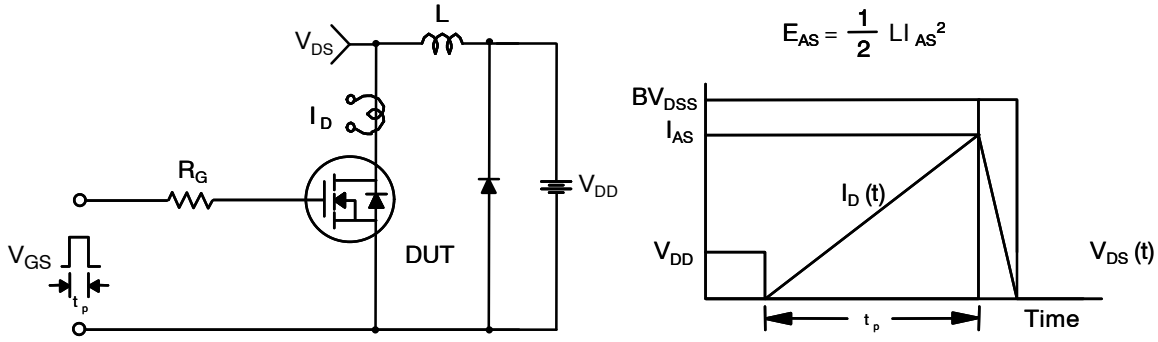


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

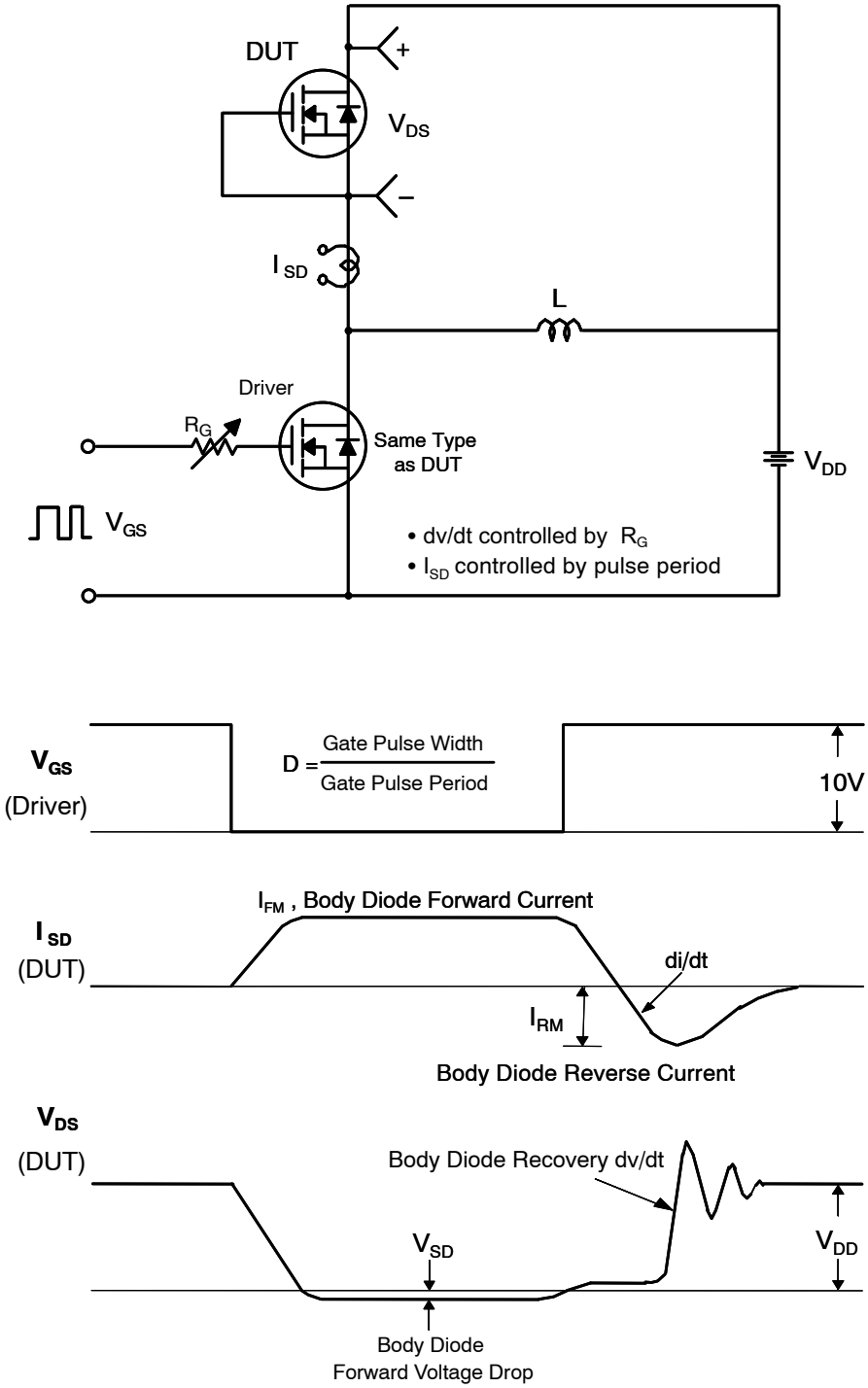
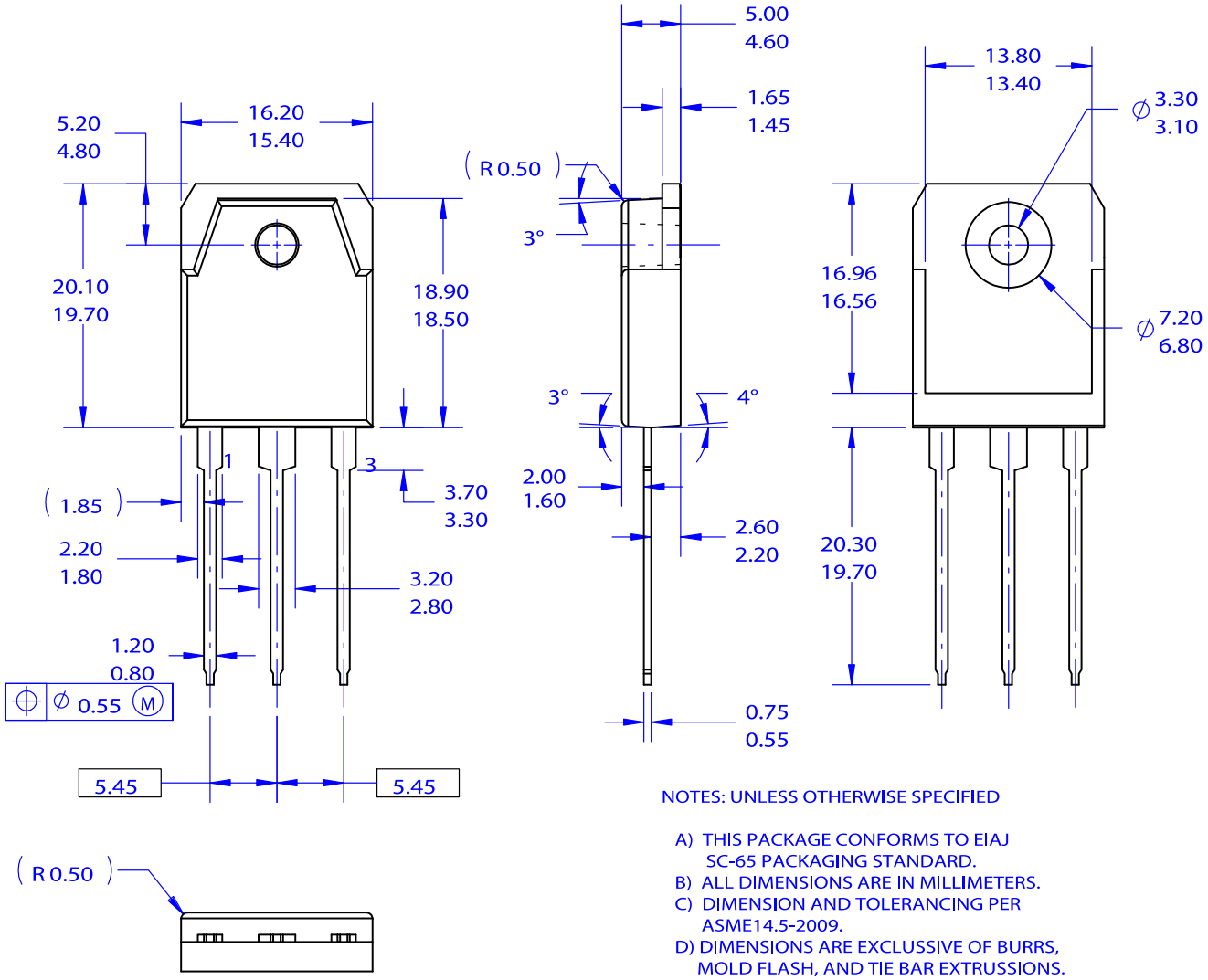


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO−3P−3LD / EIAJ SC−65, ISOLATED
CASE 340BZ
ISSUE O

DATE 31 OCT 2016



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C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.

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