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MOSFET – Power, N-Channel, SUPERFET III, Easy Drive

650 V, 30 A, 99 mΩ FCP099N65S3

Description

SUPERFET III MOSFET is **onsemi**'s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

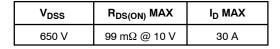
Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

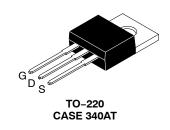
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)} = 79 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 61 \text{ nC}$)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 544 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

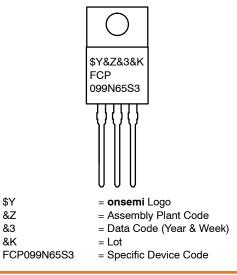
Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar





MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage		650	V
V _{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I _D	Drain Current	– Continuous (T _C = 25°C)	30	А
		– Continuous (T _C = 100°C)	19	
I _{DM}	Drain Current	– Pulsed (Note 1)	75	А
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		145	mJ
I _{AS}	Avalanche Current (Note 2)		4.4	А
E _{AR}	Repetitive Avalanche Energy (Note 1)		2.27	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	1
PD	Power Dissipation	(T _C = 25°C)	227	W
		– Derate Above 25°C	1.82	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		–55 to +150	°C
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality shows be assumed, damage may occur and reliability may be affected. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 4.4 \text{ A}, R_G = 25 \Omega$, starting $T_J = 25^{\circ}C$. 3. $I_{SD} \le 15 \text{ A}, \text{ di/dt} \le 200 \text{ A/}\mu\text{s}, \text{ V}_{DD} \le 400 \text{ V}, \text{ starting } T_J = 25^{\circ}C$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.55	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP099N65S3	FCP099N65S3	TO-220	Tube	N/A	N/A	50 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
OFF CHARACT	ERISTICS	·	•	-	-	-
BV _{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_{D} = 1 mA, T_{J} = 150°C	700			V
$\Delta \text{BV}_{\text{DSS}} / \Delta \text{T}_{\text{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 1$ mA, Referenced to $25^{\circ}C$		0.68		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			1	μA
		V_{DS} = 520 V, T_{C} = 125 °C		1.4		
I _{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTE	RISTICS	•				
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 0.74 \text{ mA}$	2.5		4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 15 A		79	99	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 15 A		19		S
OYNAMIC CHAI	RACTERISTICS	•		•		
C _{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		2480		pF
Coss	Output Capacitance			55		pF
C _{oss(eff.)}	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		544		pF
Coss(er.)	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		78		pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 15 A, V _{GS} = 10 V (Note 4)		61		nC
Q _{gs}	Gate to Source Gate Charge			15		nC
Q _{gd}	Gate to Drain "Miller" Charge			25		nC
ESR	Equivalent Series Resistance	f = 1 MHz		0.4		Ω
WITCHING CH	IARACTERISTICS	•				
t _{d(on)}	Turn-On Delay Time	V_{DD} = 400 V, I_{D} = 15 A, V_{GS} = 10 V, R_{g} = 4.7 Ω (Note 4)		23		ns
t _r	Turn-On Rise Time			24		ns
t _{d(off)}	Turn-Off Delay Time			60		ns
t _f	Turn-Off Fall Time			5		ns
SOURCE-DRAI	N DIODE CHARACTERISTICS	•		•	•	•
۱ _S	Maximum Continuous Source to Drain Diode Forward Current				30	Α
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current				75	Α
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 15 A			1.2	V
t _{rr}	Reverse Recovery Time	$V_{DD} = 400 \text{ V}, \text{ I}_{SD} = 15 \text{ A}, \text{ dI}_{\text{F}}/$		408		ns
Q _{rr}	Reverse Recovery Charge	dt = 100 A/µs		8.4	1	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

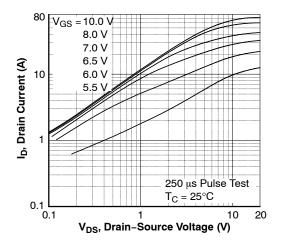
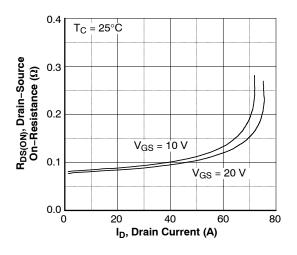
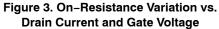
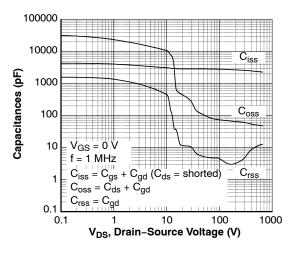


Figure 1. On-Region Characteristics









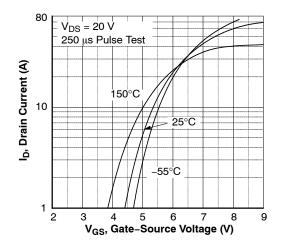


Figure 2. Transfer Characteristics

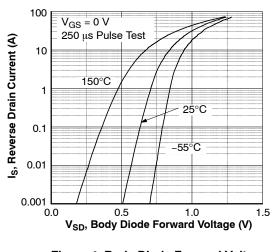


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

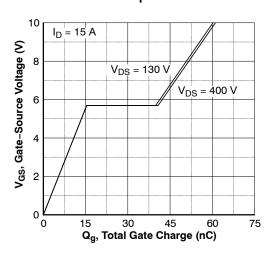


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

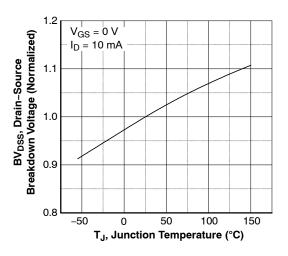


Figure 7. Breakdown Voltage Variation vs. Temperature

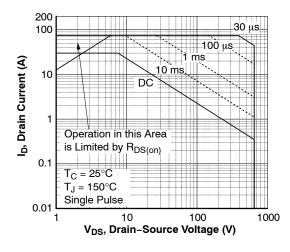


Figure 9. Maximum Safe Operating Area

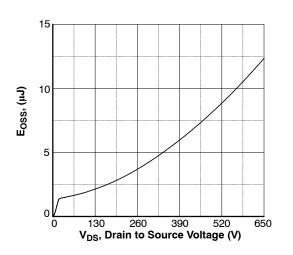


Figure 11. E_{OSS} vs. Drain to Source Voltage

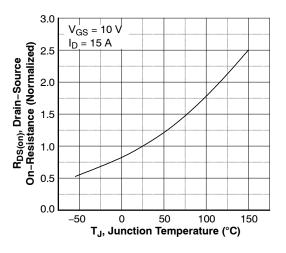


Figure 8. On–Resistance Variation vs. Temperature

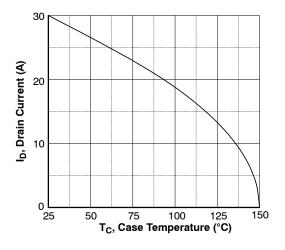


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

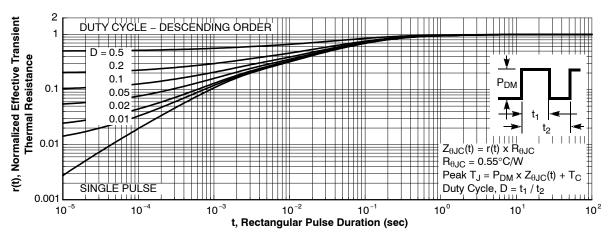
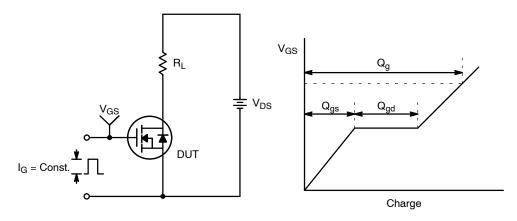


Figure 12. Transient Thermal Response Curve





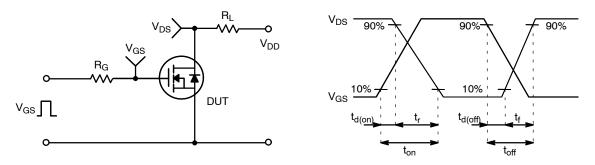
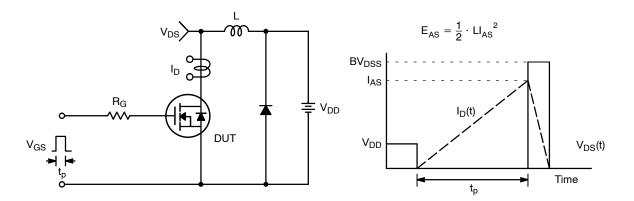


Figure 14. Resistive Switching Test Circuit & Waveforms





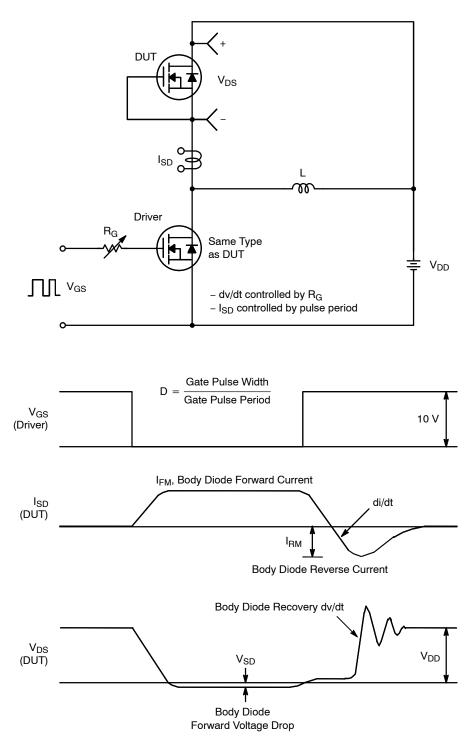
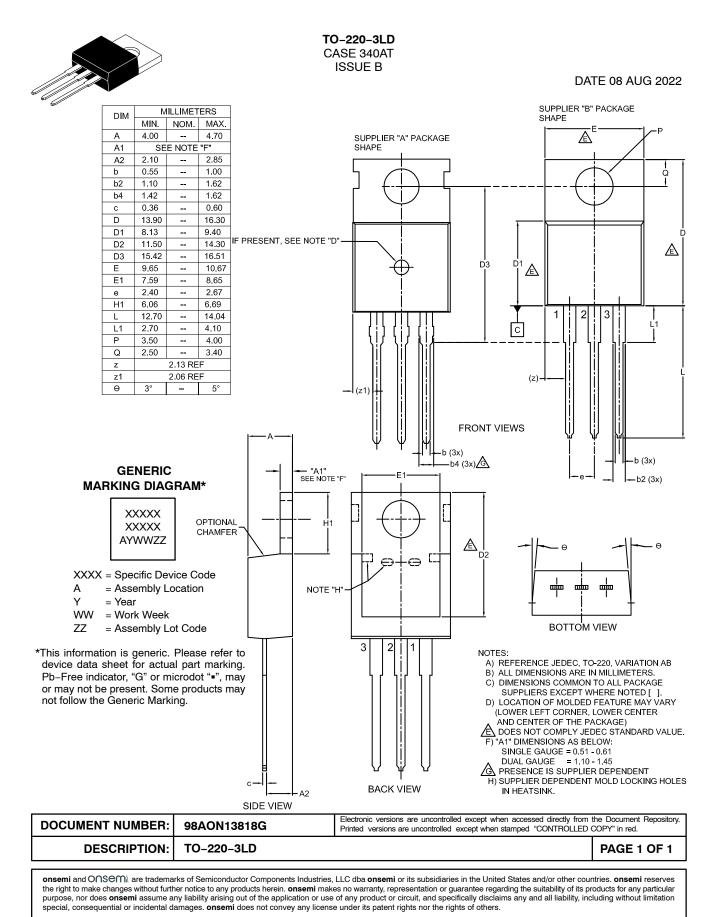


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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