

# MOSFET – N-Channel,

## 600 V, 47 A, 75 mΩ

### FCH47N60F-F085

#### Description

SUPERFET<sup>®</sup> is ON Semiconductor's proprietary new generation of high voltage MOSFETs utilizing an advanced charge balance mechanism for outstanding low on-resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.

Consequently, SUPERFET is suitable for various automotive DC/DC power conversion.

#### Features

- Typical  $r_{DS(on)}$  = 66 mΩ at  $V_{GS} = 10$  V,  $I_D = 47$  A
- Typical  $Q_{g(tot)}$  = 190 nC at  $V_{GS} = 10$  V,  $I_D = 47$  A
- UIS Capability
- Qualified to AEC Q101 and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

#### Applications

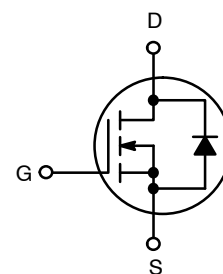
- Automotive On Board Charger
- Automotive DC/DC Converter for HEV



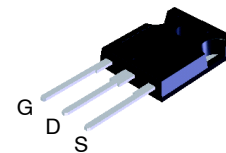
ON Semiconductor<sup>®</sup>

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$V_{DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
600 V	75 mΩ	47 A

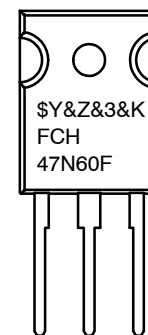


N-Channel MOSFET



TO-247  
CASE 340CK

#### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
&Z = Assembly Plant Code  
&3 = Data Code (Year & Week)  
&K = Lot Code  
FCH47N60F = Specific Device Code

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FCH47N60F–F085

## MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current – Continuous ( $V_{GS} = 10$ ) (Note 1)	$T_C = 25^\circ\text{C}$ 47	A
	Pulsed Drain Current	$T_C = 25^\circ\text{C}$ See Fig. 4	
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	810	mJ
$P_D$	Power Dissipation	417	W
	Derate above $25^\circ\text{C}$	3.3	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	$-55$ to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Current is limited by bondwire configuration.
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 5$  mH,  $I_{AS} = 18$  A,  $V_{DD} = 100$  V during inductor charging and  $V_{DD} = 0$  V during time in avalanche.
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2oz copper.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	50	

## PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FCH47N60F–F085	FCH47N60F	TO–247–3LD	–	–	30 Units

# FCH47N60F–F085

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	600	–	–	V
$I_{DSS}$	Drain to Source Leakage Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	–	–	10	$\mu\text{A}$
		$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$ (Note 4)	–	–	1	mA
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 30\text{ V}$	–	–	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3	4	5	V
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 47\text{ A}, T_J = 25^\circ\text{C}$	–	66	75	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 47\text{ A}, T_J = 150^\circ\text{C}$ (Note 4)	–	180	223	$\text{m}\Omega$

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	–	5900	8000	pF
$C_{oss}$	Output Capacitance		–	3200	4200	pF
$C_{rss}$	Reverse Transfer Capacitance		–	250	–	pF
$R_g$	Gate Resistance	$f = 1\text{ MHz}$	–	1	–	$\Omega$
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{GS} = 0\text{ to }10\text{ V}, V_{DD} = 300\text{ V}, I_D = 47\text{ A}$	–	190	250	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0\text{ to }2\text{ V}, V_{DD} = 300\text{ V}, I_D = 47\text{ A}$	–	12	18	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 300\text{ V}, I_D = 47\text{ A}$	–	40	–	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		–	96	–	nC

### SWITCHING CHARACTERISTICS

$t_{on}$	Turn-On Time	$V_{DD} = 300\text{ V}, I_D = 47\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	–	–	410	ns
$t_{d(on)}$	Turn-On Delay Time		–	110	–	ns
$t_r$	Rise Time		–	160	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	540	–	ns
$t_f$	Fall Time		–	125	–	ns
$t_{off}$	Turn-Off Time		–	–	1000	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

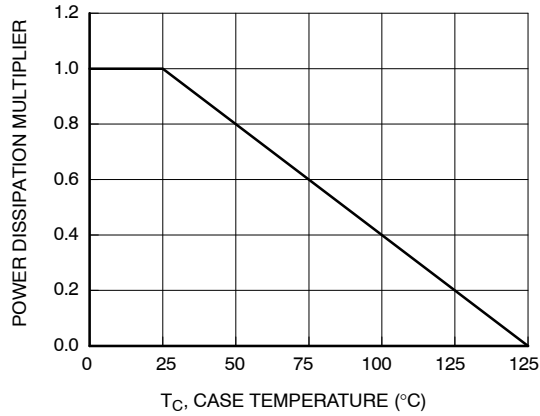
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 47\text{ A}, V_{GS} = 0\text{ V}$	–	–	1.4	V
		$I_{SD} = 23.5\text{ A}, V_{GS} = 0\text{ V}$	–	–	1.25	V
$T_{rr}$	Reverse Recovery Time	$I_F = 47\text{ A}, dI_{SD}/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 480\text{ V}$	–	207	350	ns
$Q_{rr}$	Reverse Recovery Charge		–	2	3.6	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

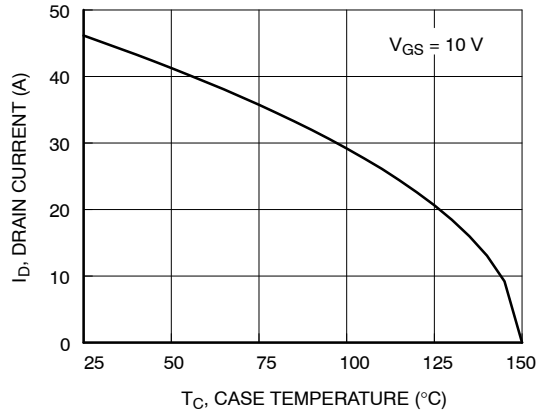
4. The maximum value is specified by design at  $T_J = 150^\circ\text{C}$ . Product is not tested to this condition in production.

# FCH47N60F-F085

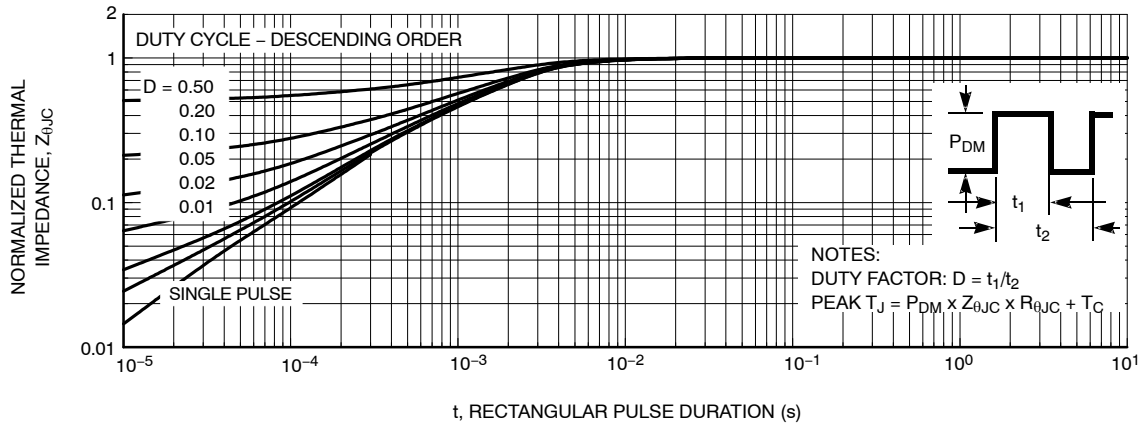
## TYPICAL CHARACTERISTICS



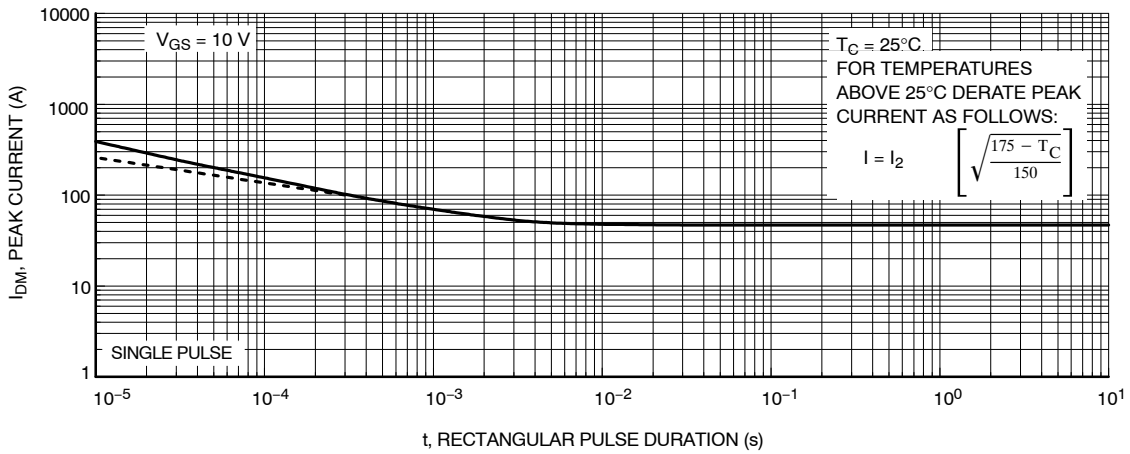
**Figure 1. Normalized Power Dissipation vs. Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 3. Normalized Maximum Transient Thermal Impedance**



**Figure 4. Peak Current Capability**

TYPICAL CHARACTERISTICS (continued)

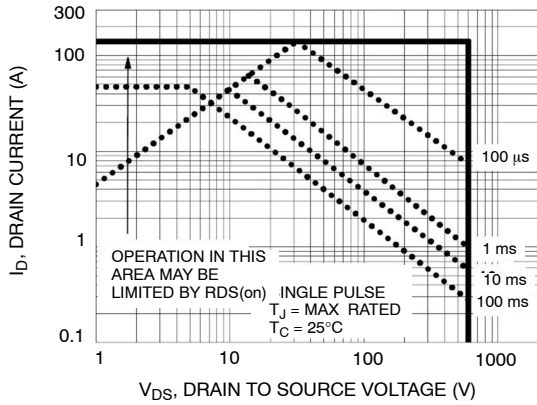


Figure 5. Forward Bias Safe Operating Area

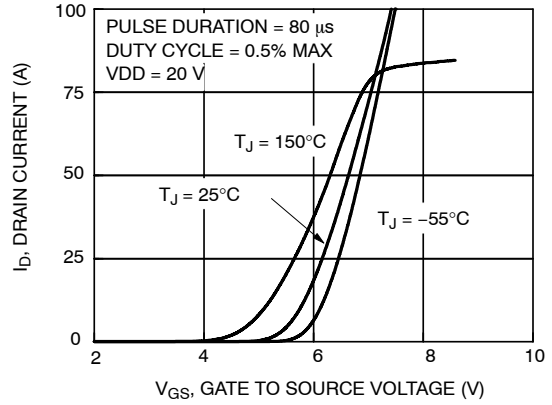


Figure 6. Transfer Characteristics

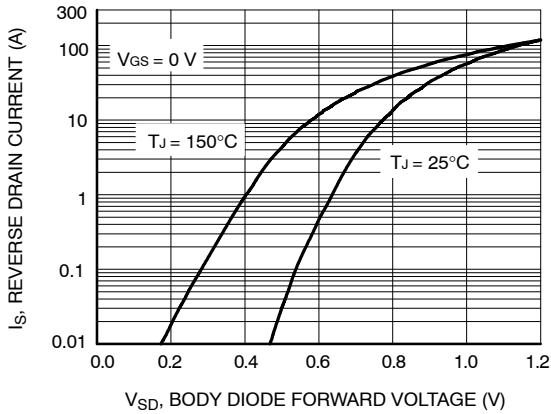


Figure 7. Forward Diode Characteristics

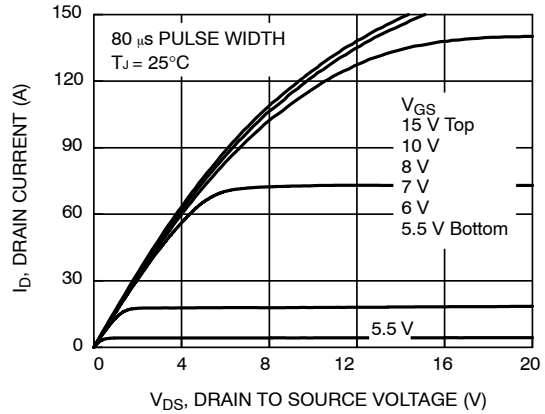


Figure 8. Saturation Characteristics

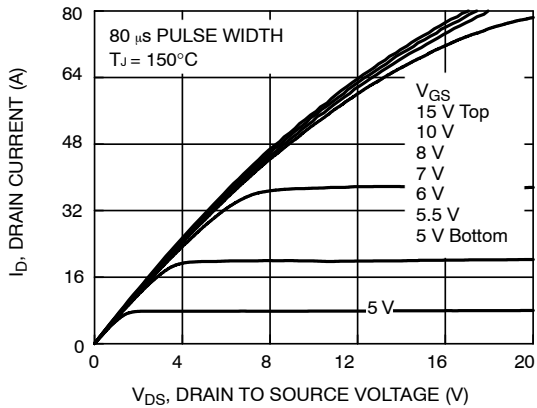


Figure 9. Saturation Characteristics

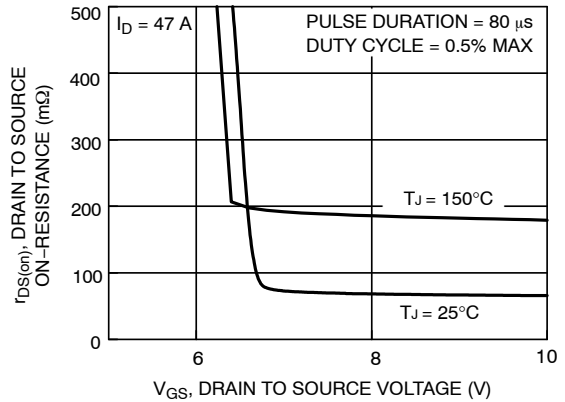


Figure 10.  $R_{DS(on)}$  vs. Gate Voltage

TYPICAL CHARACTERISTICS (continued)

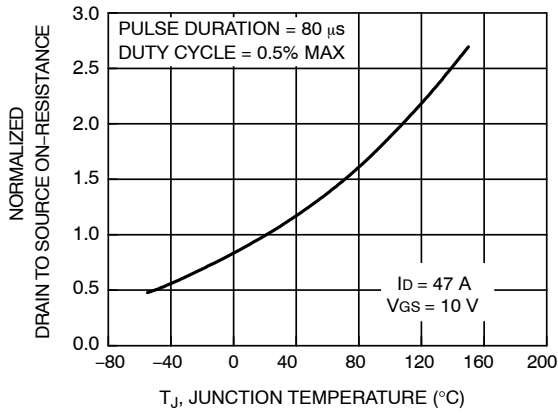


Figure 11. Normalized  $R_{DS(on)}$  vs. Junction Temperature

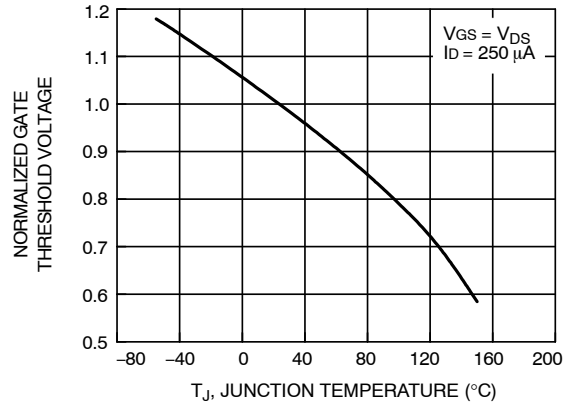


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

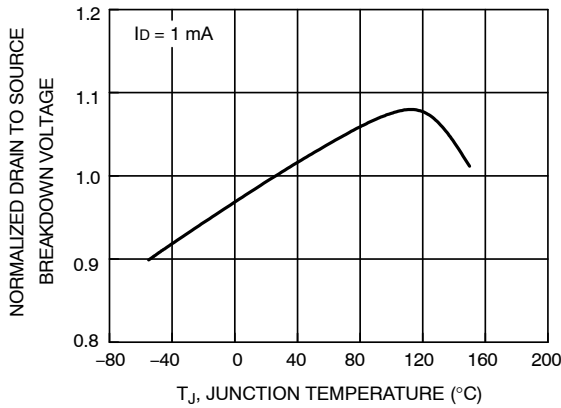


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

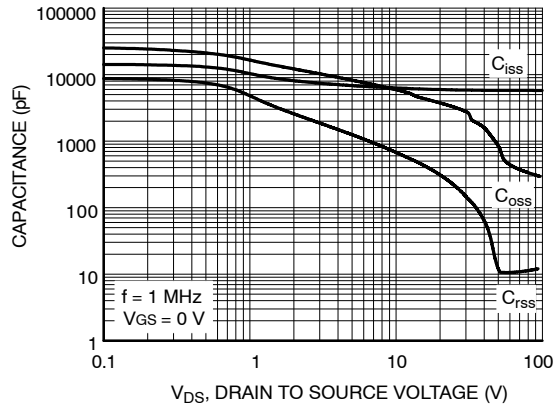


Figure 14. Capacitance vs. Drain to Source Voltage

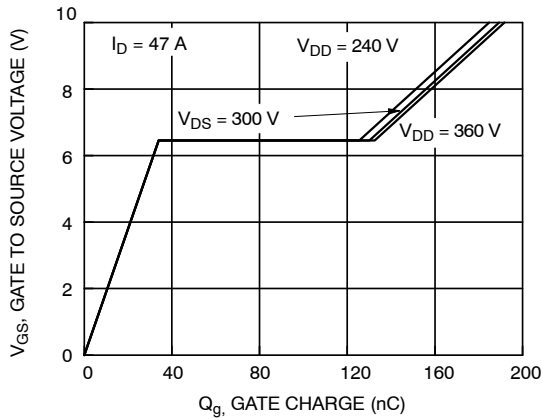
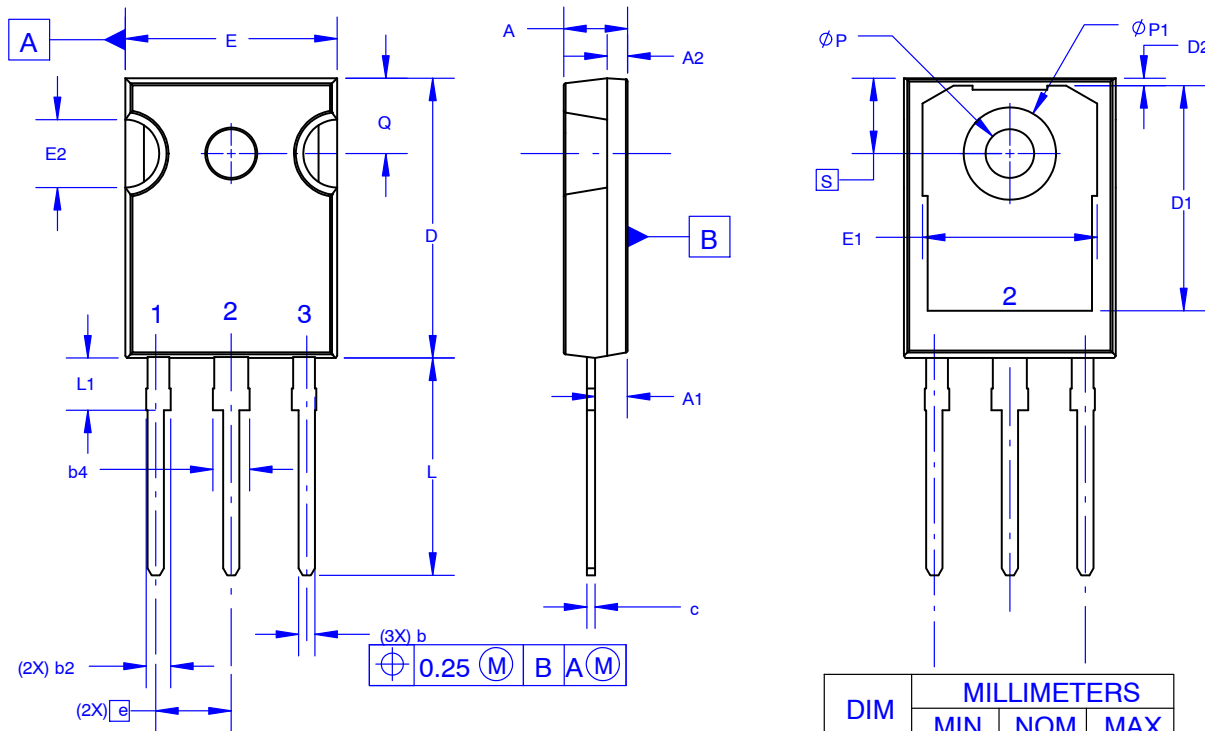


Figure 15. Gate Charge vs. Gate to Source Voltage

**TO-247-3LD SHORT LEAD  
CASE 340CK  
ISSUE A**

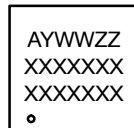
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NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

**GENERIC  
MARKING DIAGRAM\***



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
∅P	3.51	3.58	3.65
∅P1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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