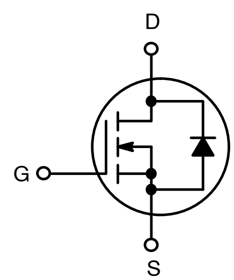
MOSFET – N-Channel, 600 V, 47 A, 75 mΩ

FCH47N60F-F085

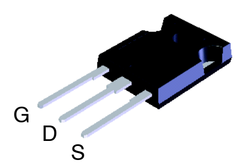
ON Semiconductor®

www.onsemi.com

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
600 V	75 mΩ	47 A

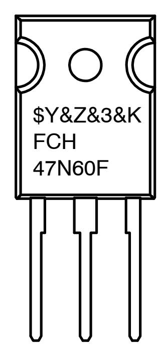


N-Channel MOSFET



TO−247
CASE 340CK

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot Code
FCH47N60F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

SUPERFET® is ON Semiconductor's proprietary new generation of high voltage MOSFETs utilizing an advanced charge balance mechanism for outstanding low on−resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.

Consequently, SUPERFET is suitable for various automotive DC/DC power conversion.

Features

- Typical $r_{DS(on)}$ = 66 mΩ at V_{GS} = 10 V, I_D = 47 A
- Typical $Q_{g(tot)}$ = 190 nC at V_{GS} = 10 V, I_D = 47 A
- UIS Capability
- Qualified to AEC Q101 and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for HEV

MOSFET MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GS}	Gate to Source Voltage		±30	V
I_D	Drain Current − Continuous (V_{GS} = 10) (Note 1)	T_C = 25°C	47	A
	Pulsed Drain Current	T_C = 25°C	See Fig. 4	
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		810	mJ
P_D	Power Dissipation		417	W
	Derate above 25°C		3.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 5 mH, I_{AS} = 18 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	50	

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FCH47N60F−F085	FCH47N60F	TO−247−3LD	–	–	30 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
B_{VDSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	600	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 25°C	–	–	10	μA
		V_{DS} = 600 V, V_{GS} = 0 V, T_J = 150°C (Note 4)	–	–	1	mA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±30 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3	4	5	V
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 47 A, T_J = 25°C	–	66	75	mΩ
		V_{GS} = 10 V, I_D = 47 A, T_J = 150°C (Note 4)	–	180	223	mΩ
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	5900	8000	pF
C_{oss}	Output Capacitance		–	3200	4200	pF
C_{rss}	Reverse Transfer Capacitance		–	250	–	pF
R_g	Gate Resistance	f = 1 MHz	–	1	–	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V_{GS} = 0 to 10 V, V_{DD} = 300 V, I_D = 47 A	–	190	250	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V, V_{DD} = 300 V, I_D = 47 A	–	12	18	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 300 V, I_D = 47 A	–	40	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	96	–	nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn-On Time	V_{DD} = 300 V, I_D = 47 A, V_{GS} = 10 V, R_G = 25 Ω	–	–	410	ns
$t_{d(on)}$	Turn-On Delay Time		–	110	–	ns
t_r	Rise Time		–	160	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	540	–	ns
t_f	Fall Time		–	125	–	ns
t_{off}	Turn-Off Time		–	–	1000	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 47 A, V_{GS} = 0 V	–	–	1.4	V
		I_{SD} = 23.5 A, V_{GS} = 0 V	–	–	1.25	V
T_{rr}	Reverse Recovery Time	I_F = 47 A, dI_{SD}/dt = 100 A/μs, V_{DD} = 480 V	–	207	350	ns
Q_{rr}	Reverse Recovery Charge		–	2	3.6	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

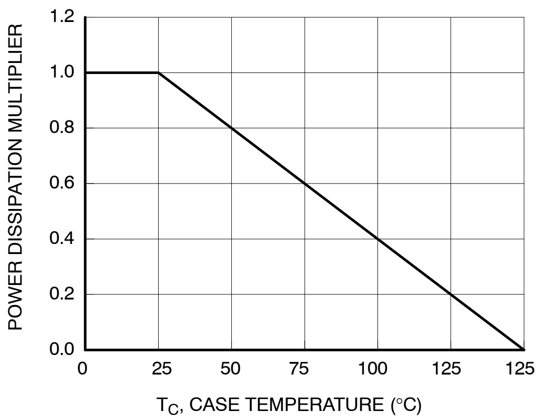


Figure 1. Normalized Power Dissipation vs. Case Temperature

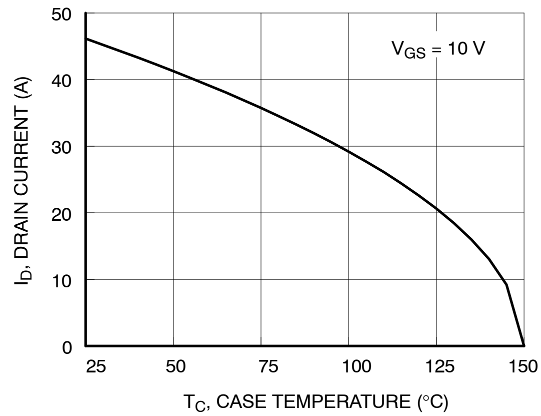


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

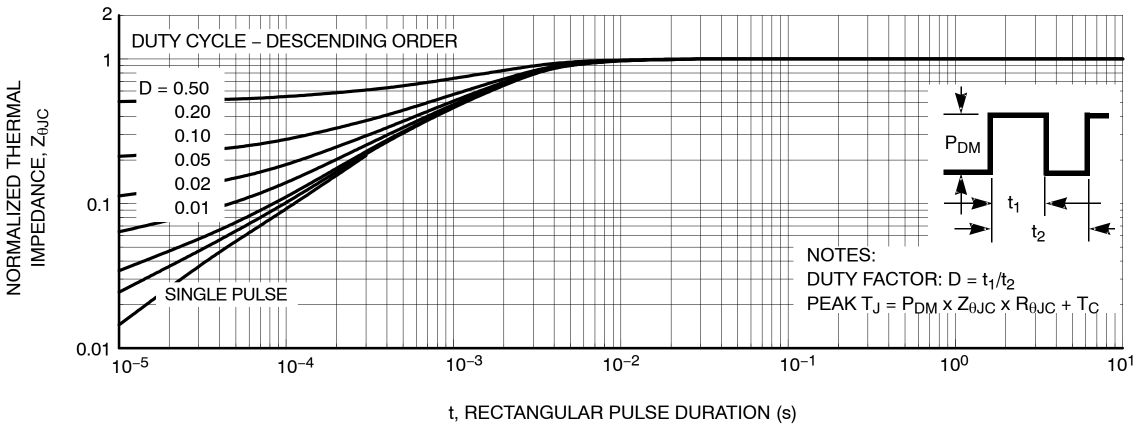


Figure 3. Normalized Maximum Transient Thermal Impedance

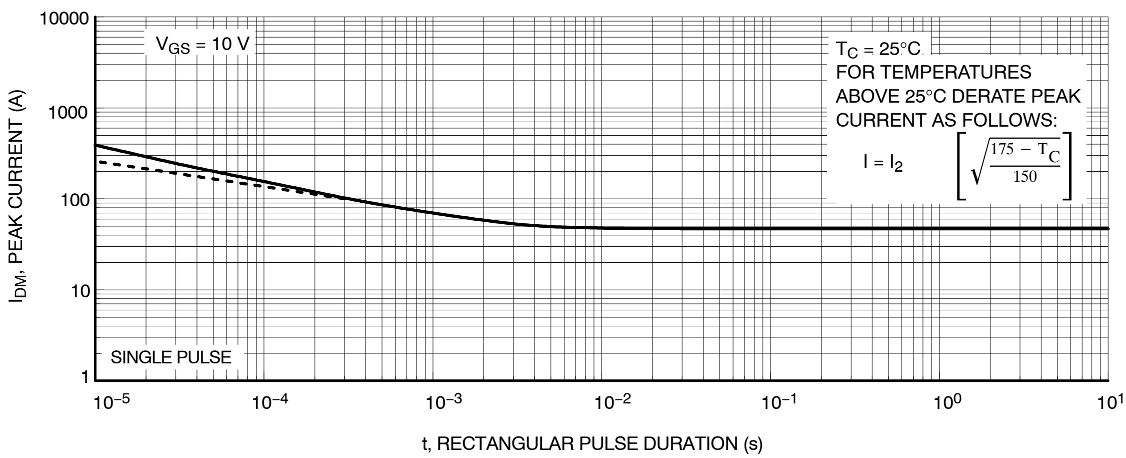


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

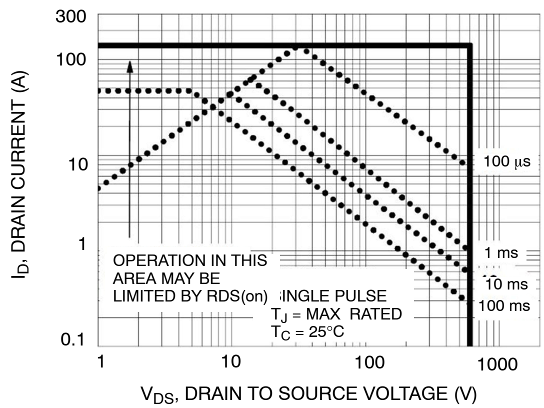


Figure 5. Forward Bias Safe Operating Area

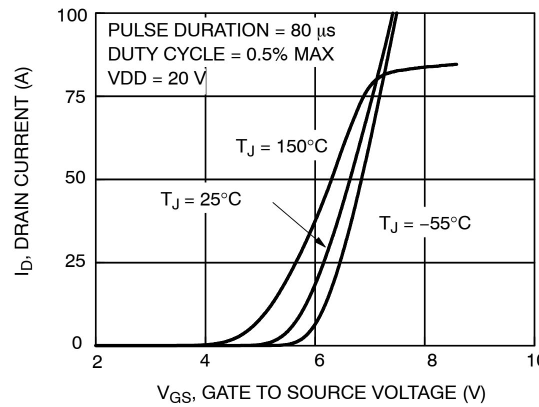


Figure 6. Transfer Characteristics

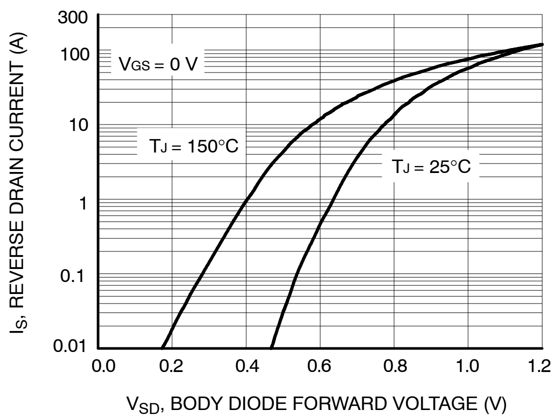


Figure 7. Forward Diode Characteristics

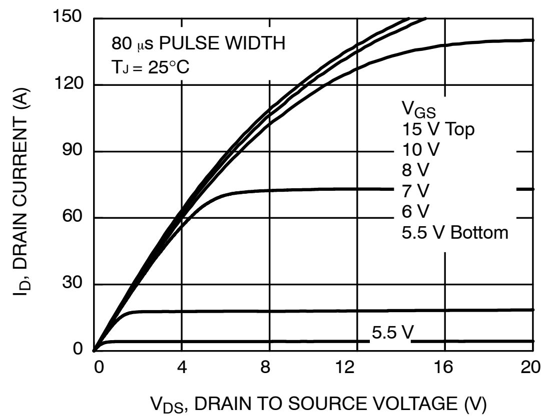


Figure 8. Saturation Characteristics

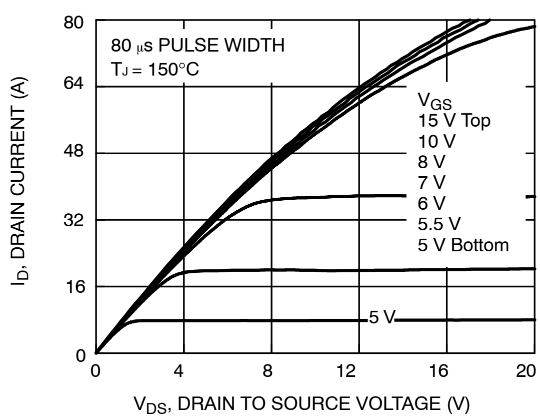


Figure 9. Saturation Characteristics

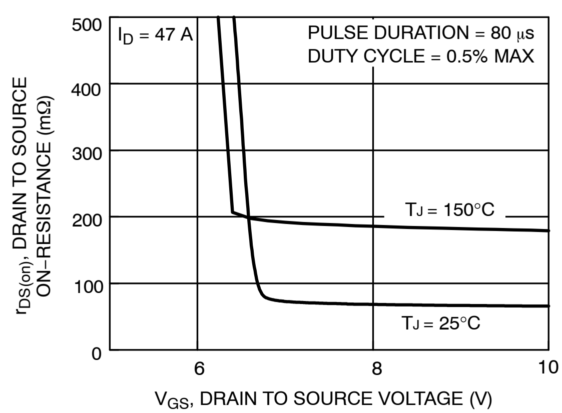


Figure 10. R_{DSON} vs. Gate Voltage

TYPICAL CHARACTERISTICS (continued)

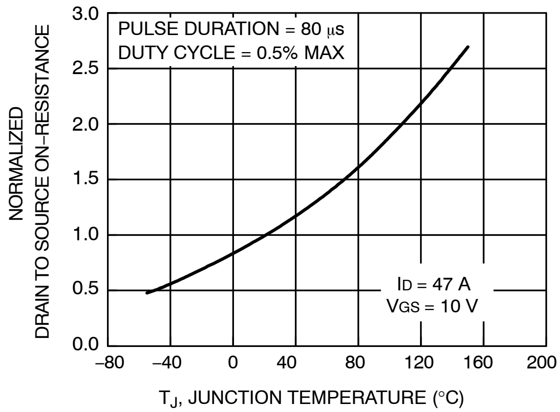


Figure 11. Normalized R_{DSON} vs. Junction Temperature

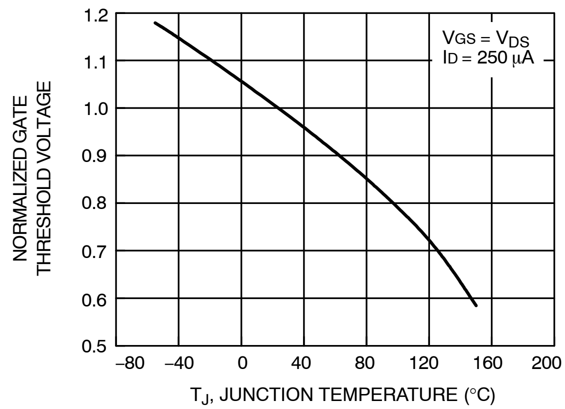


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

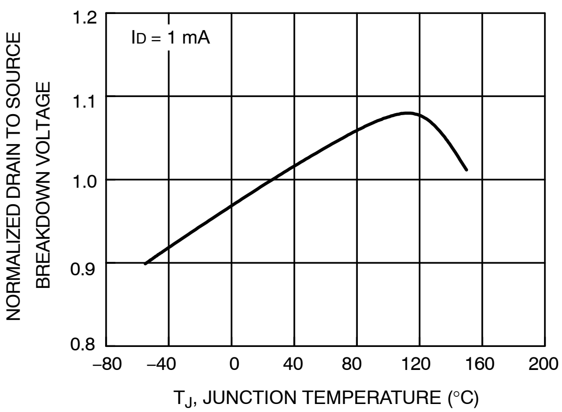


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

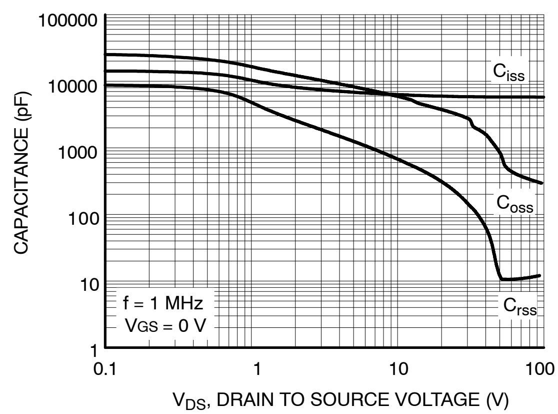


Figure 14. Capacitance vs. Drain to Source Voltage

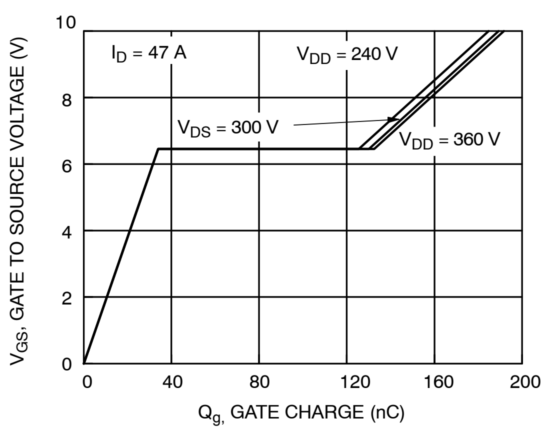
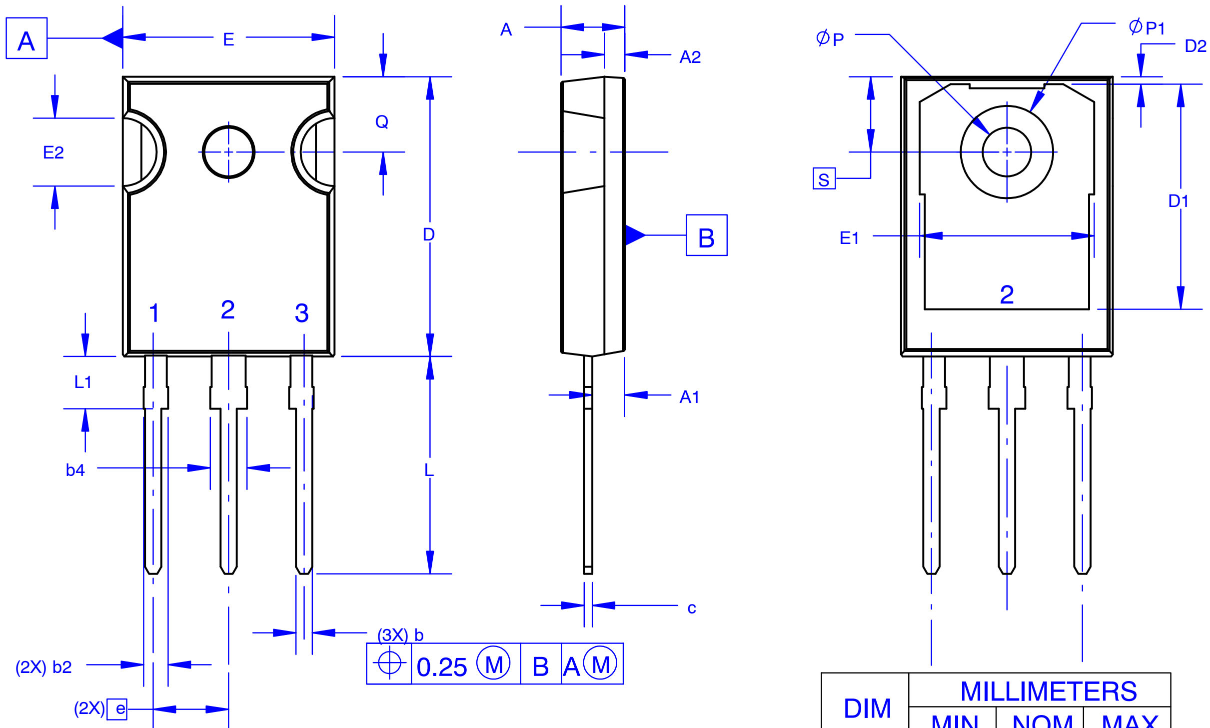


Figure 15. Gate Charge vs. Gate to Source Voltage

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019

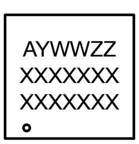


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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