



















## Typical Characteristics

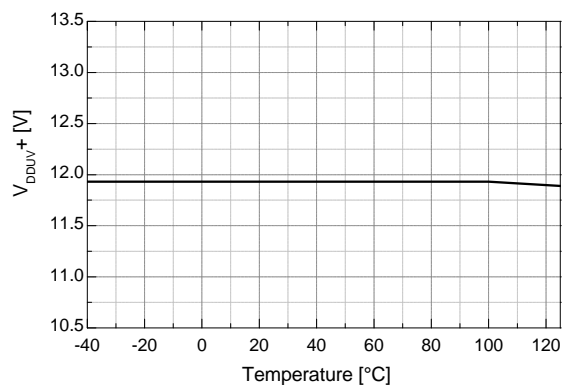


Figure 5.  $V_{DD}$  UVLO (+) vs. Temperature

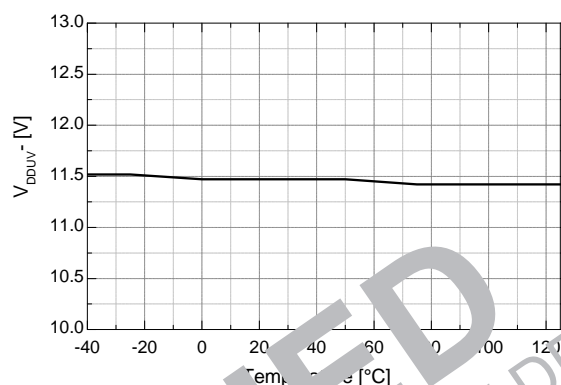


Figure 6.  $V_{DD}$  UVLO (-) vs. Temperature

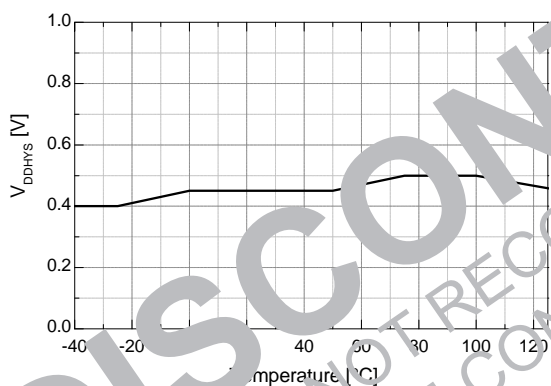


Figure 7.  $V_{DD}$  UVLO Hysteresis vs. Temperature

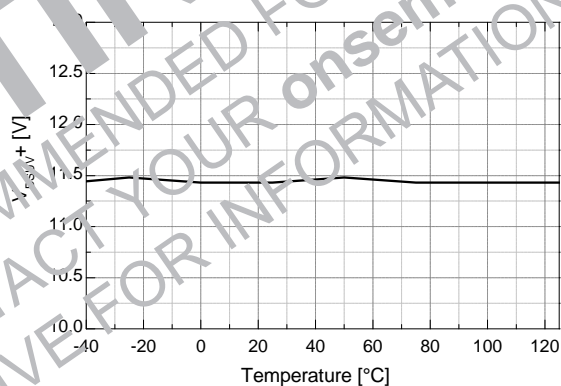


Figure 8.  $V_{BS}$  UVLO (+) vs. Temperature

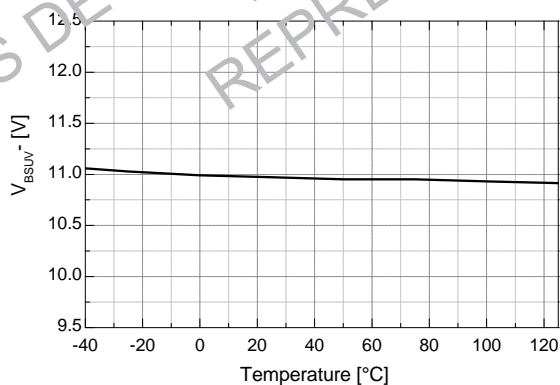


Figure 9.  $V_{BS}$  UVLO (-) vs. Temperature

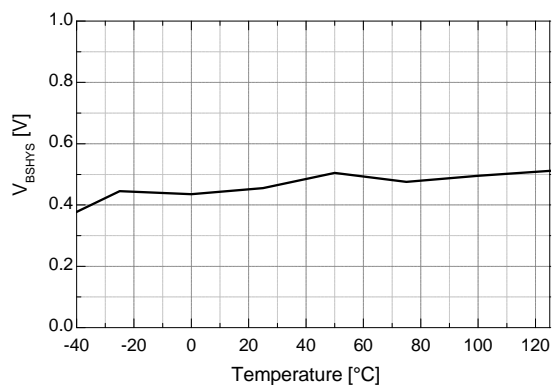


Figure 10.  $V_{BS}$  UVLO Hysteresis vs. Temperature

## Typical Characteristics (Continued)

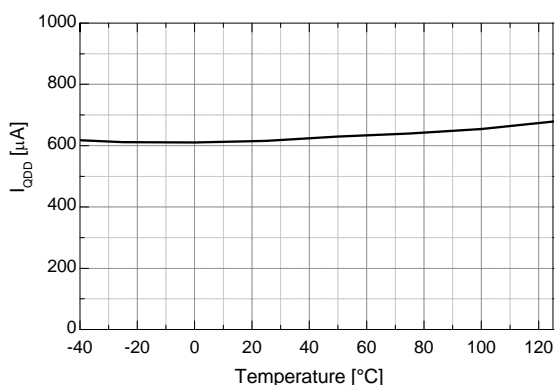
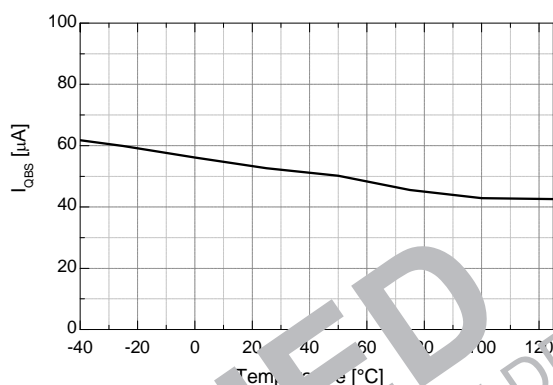
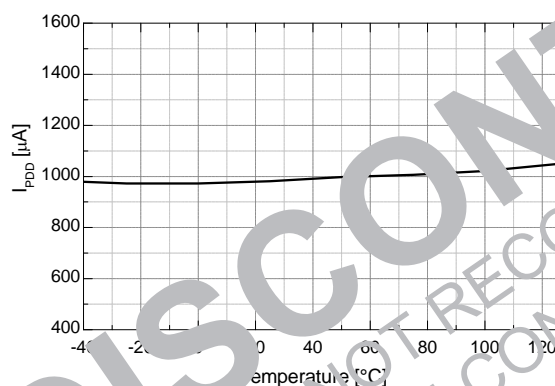
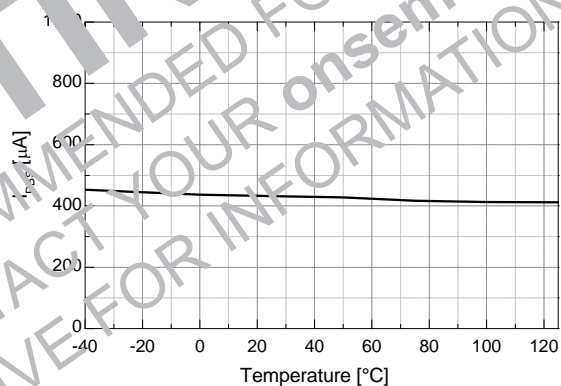
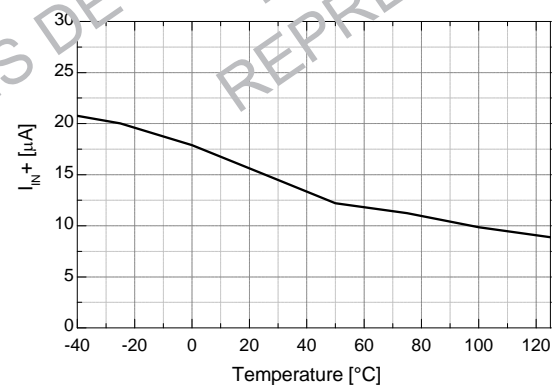
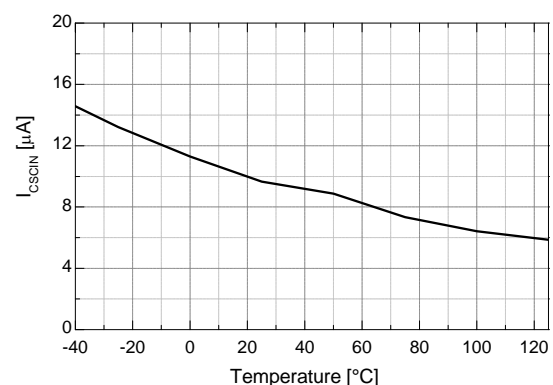
Figure 11.  $V_{DD}$  Quiescent Current vs. TemperatureFigure 12.  $V_E$  Quiescent Current vs. TemperatureFigure 13.  $V_{DD}$  Operating Current vs. TemperatureFigure 14.  $V_{BS}$  Operating Current vs. Temperature

Figure 15. Logic Input Current vs. Temperature

Figure 16.  $I_{CSCIN}$  vs. Temperature

## Typical Characteristics (Continued)

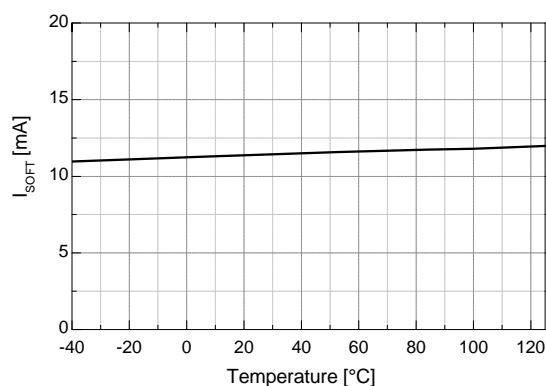
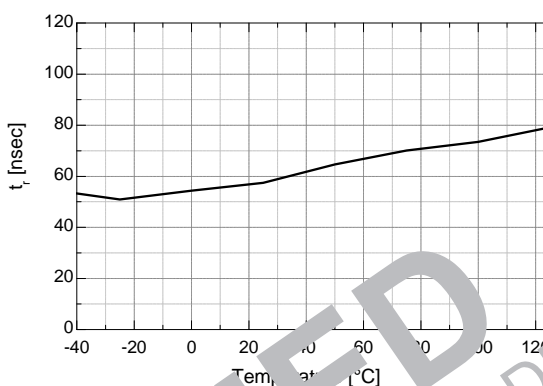
Figure 17.  $I_{SOFT}$  vs. Temperature

Figure 18. Turn-on Rising Time vs. Temperature

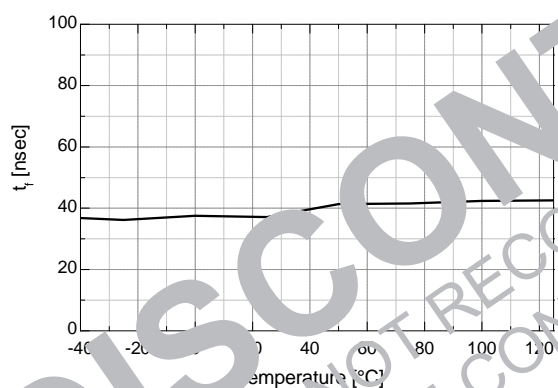


Figure 19. Turn-off Falling Time vs. Temperature

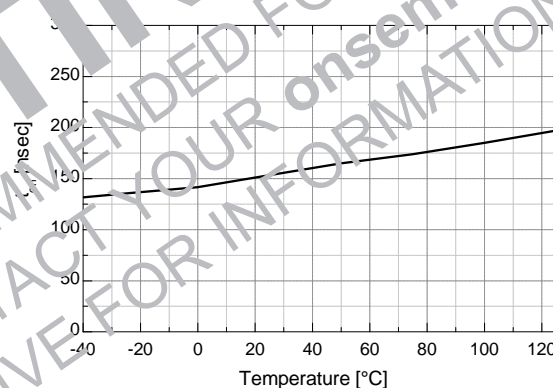


Figure 20. Turn-on Delay Time vs. Temperature

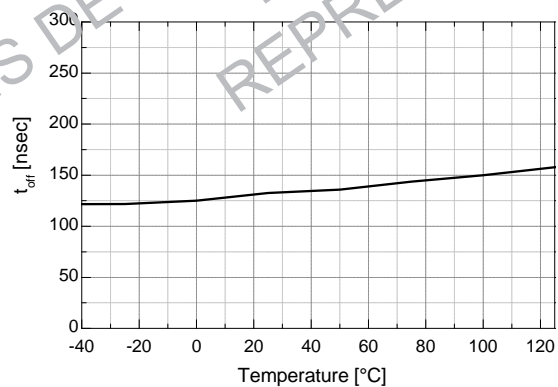


Figure 21. Turn-off Delay Time vs. Temperature

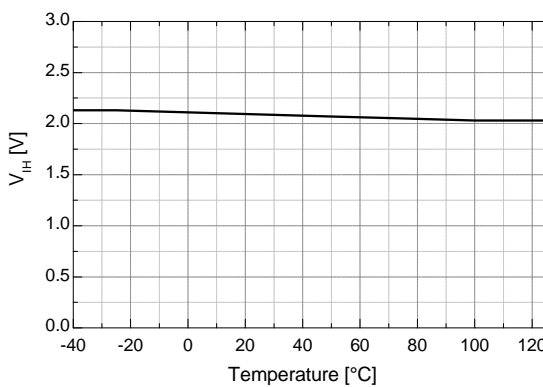


Figure 22. Logic Input High Voltage vs. Temperature

## Typical Characteristics (Continued)

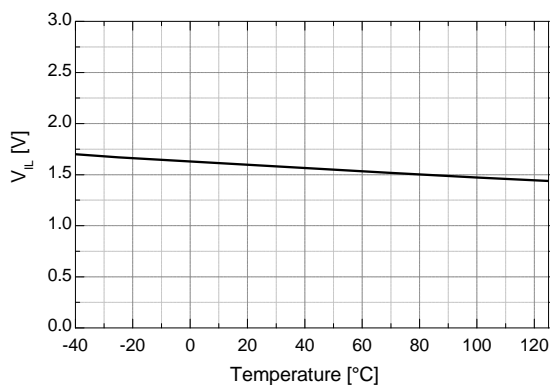


Figure 23. Logic Input Low Voltage vs. Temperature

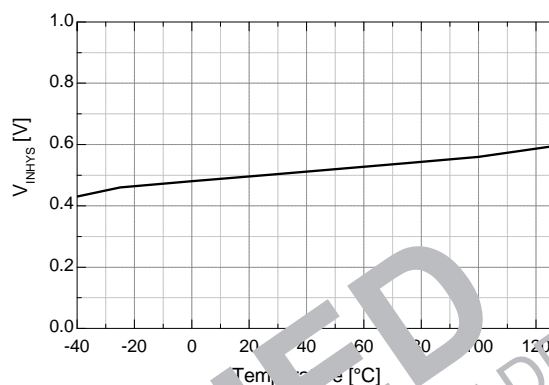


Figure 24. Logic Input Hysteresis vs. Temperature

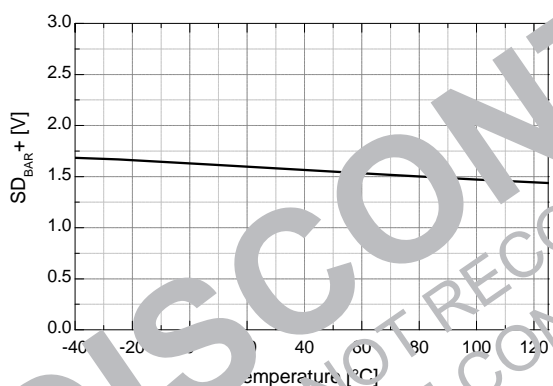
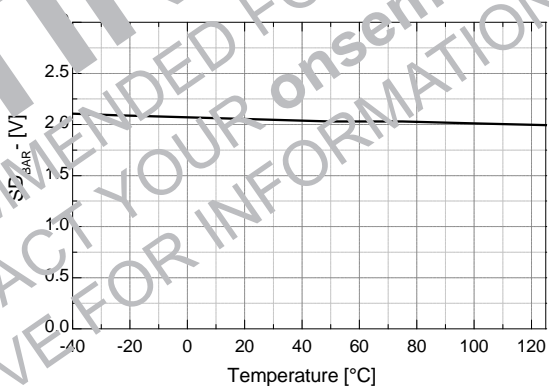
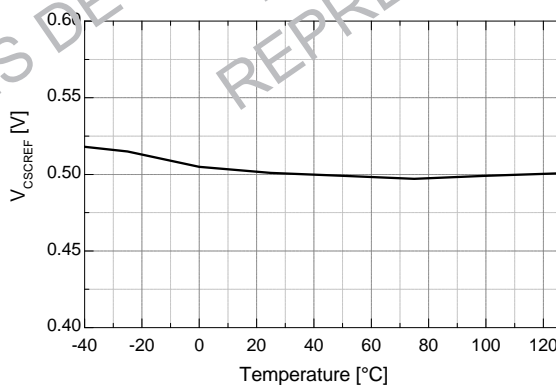
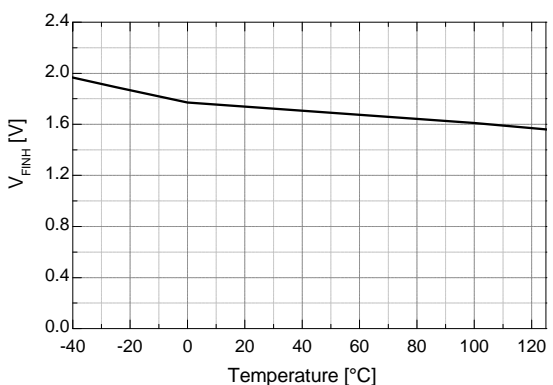
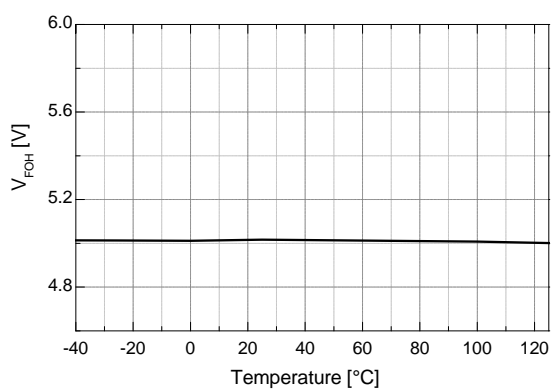
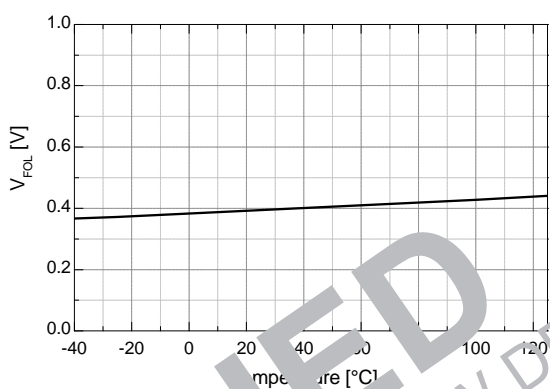
Figure 25.  $\overline{SD}$  Positive Threshold vs. TemperatureFigure 26.  $\overline{SD}$  Negative Threshold vs. TemperatureFigure 27.  $V_{CSCREF}$  vs. Temperature

Figure 28. Fault Input High Voltage vs. Temperature

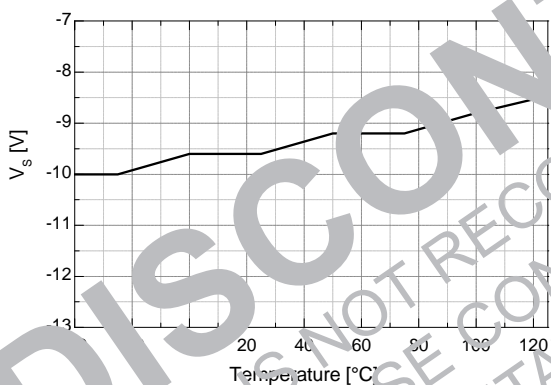
# Typical Characteristics (Continued)



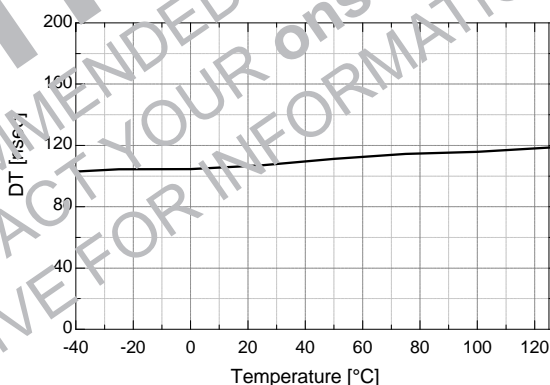
**Figure 29. Fault Output High Voltage vs. Temperature**



**Figure 30. Fault Output Low Voltage vs. Temperature**



**Figure 31. Allowable Negative  $V_S$  Voltage for Signal Propagation to High Side vs. Temperature**



**Figure 32. Dead Time vs. Temperature**

## Switching Time Definitions

The overall switching timing waveforms definition of FAN7384 as shown Figure 33.

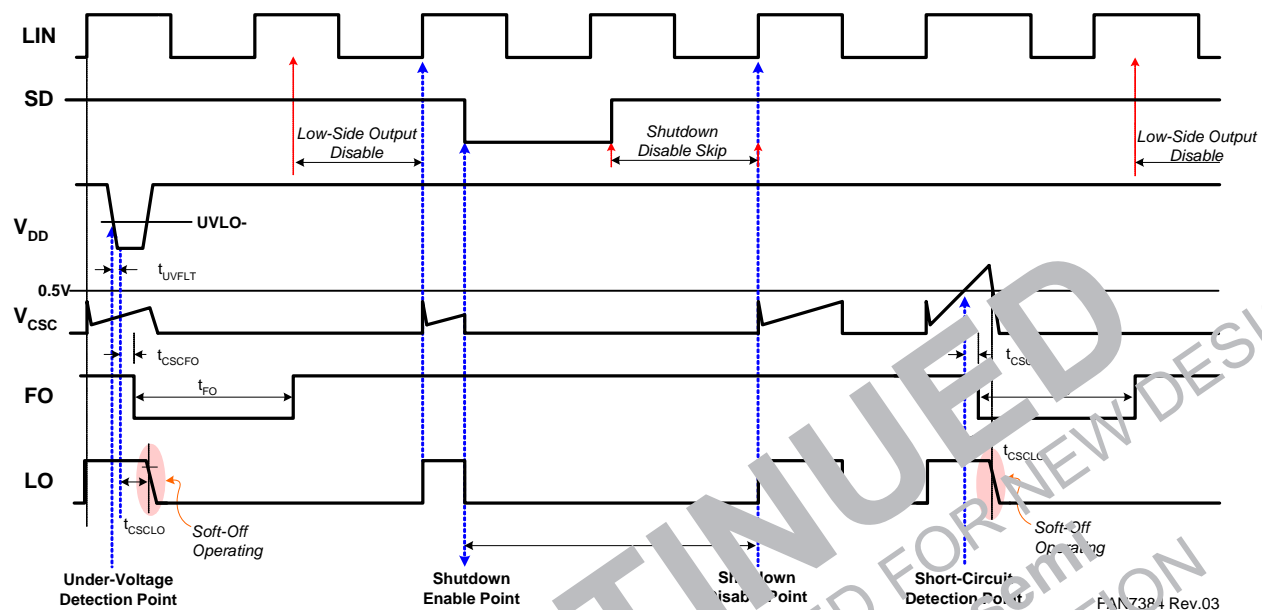


Figure 33. Switching Timing Waveforms Definition

## Typical Application Information

### 1. Protection Function

#### 1.1 Under-Voltage Lockout (UVLO)

The high- and low-side drivers include under-voltage lockout (UVLO) protection circuitry that monitors the supply voltage ( $V_{DD}$ ) and bootstrap capacitor voltage ( $V_{BS}$ ) independently. It can be designed to prevent malfunction when  $V_{DD}$  and  $V_{BS}$  are lower than the specified threshold voltage. Moreover, the UVLO hysteresis prevents chattering during power supply transitions. If the supply voltage ( $V_{DD}$ ) maintains an under-voltage condition over under-voltage filtering times (typically  $16\mu s$ ), the fault and soft-off circuits are activated, as shown Figure 34.

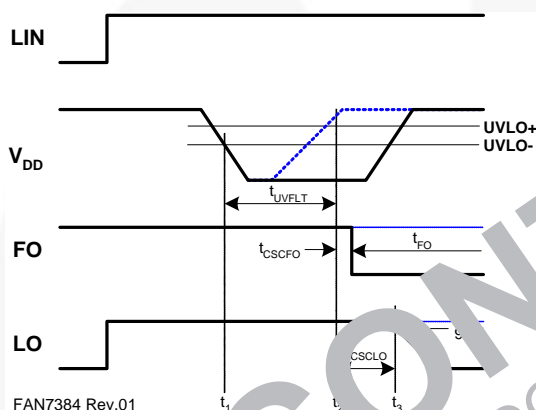


Figure 34. Waveform for Under-Voltage Lockout

#### 1.2 Shoot-Through Prevention Function

The FAN7384 has a shoot-through prevention circuitry that monitors the high- and low-side inputs. It can be designed to prevent outputs of high- and low-side turning on at the same time, as shown Figure 35 and 36.

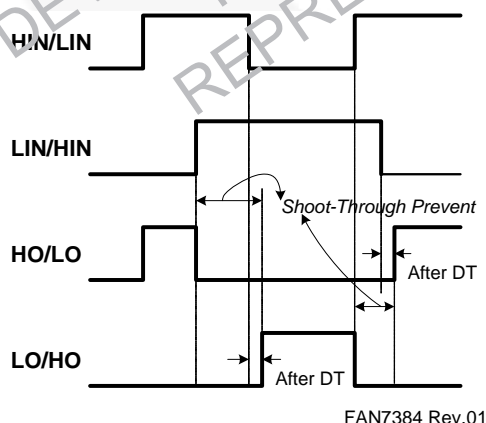


Figure 35. Waveforms for Shoot-Through Prevention

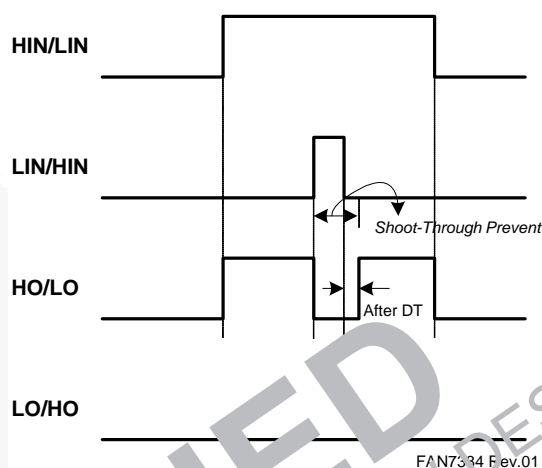


Figure 36. Waveform for Shoot-Through Prevention

#### 3. Current Limit Protection Function

The FAN7384 has over-current detection circuitry that monitors the current-by-current sensing resistor connected from the low-side switch source ( $V_{SL}$ ) to ground.

It is a built-in time-filler from the over-current event to prevent malfunction from a noise source, such as leading edge pulse in inductive load application, as shown Figure 37.

The sensing current is calculated as follows:

$$I_{CS} = \frac{V_{CSCREF}}{R_{CS}} [A] \quad (1)$$

where,

$V_{CSCREF}$ : Reference voltage of current sense comparator

$R_{CS}$ : Current sensing resistor

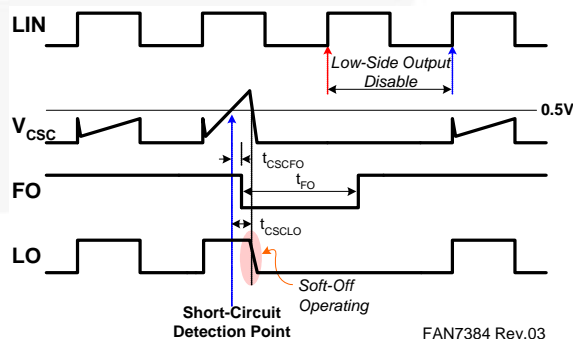


Figure 37. Waveforms for Short-Circuit Protection

## 2. Layout Considerations

For optimum performance, considerations must be taken during printed circuit board (PCB) layout.

### 2.1 Supply Capacitors

If the output stages are able to quickly turn on a switching device with a high value of current, the supply capacitors must be placed as close as possible to the device pins ( $V_{DD}$  and GND for the ground-tied supply,  $V_B$  and  $V_S$  for the floating supply) to minimize parasitic inductance and resistance.

### 2.2 Gate-Drive Loop

Current loops behave like antennae, able to receive and transmit noise. To reduce the noise coupling/emission and improve the power switch turn-on and off performance, gate-drive loops must be reduced as much as possible.

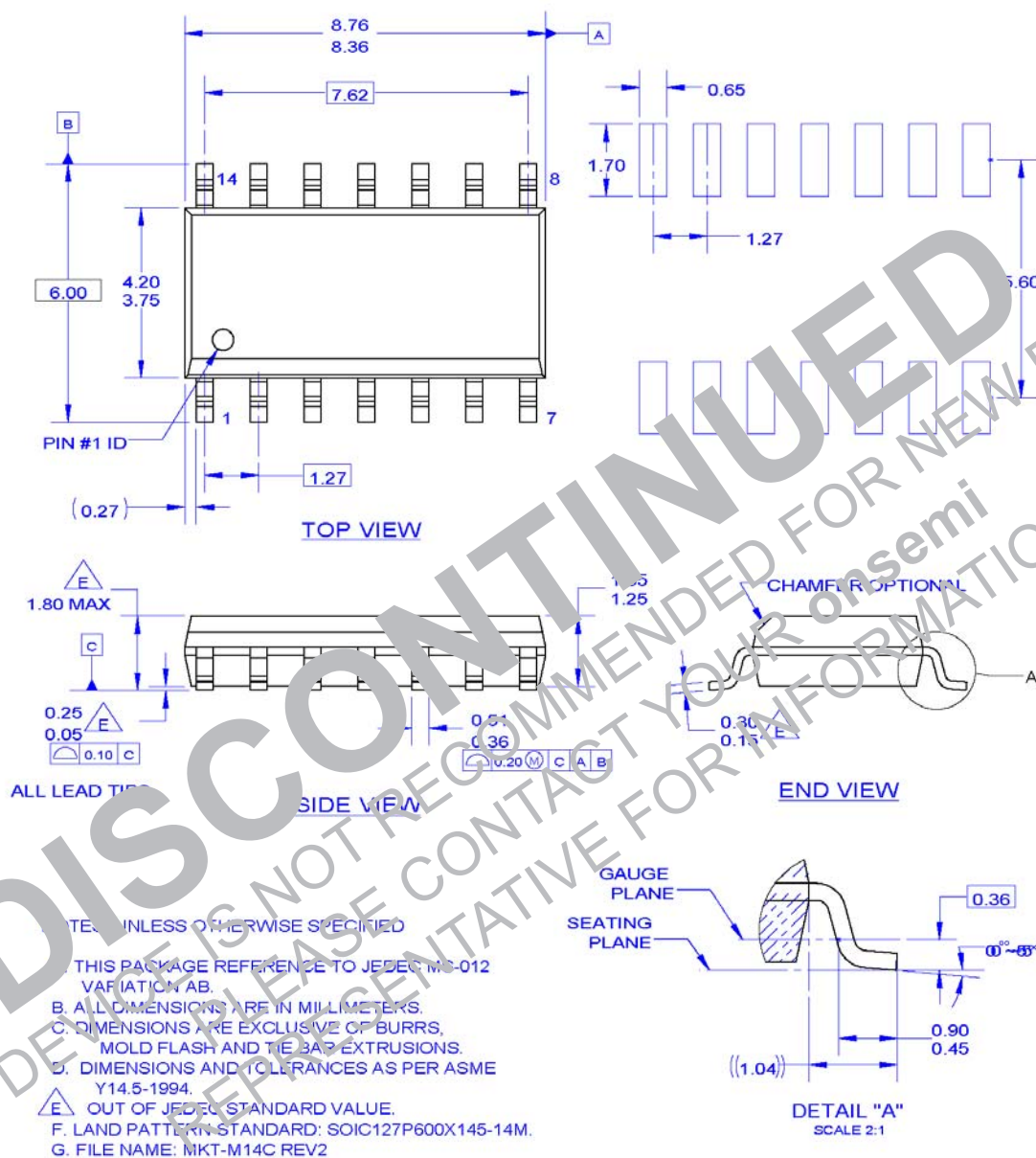
### 2.3 Ground Plane

To minimize noise coupling, the ground plane should not be placed under or near the high-voltage floating side.

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## Package Dimensions



**Figure 38. 14-Lead, Small Outline Integrated Circuit (SOIC), Non-JEDEC, .150 Inch Narrow Body, 225SOP**

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