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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor’s system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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FAN602
Offline Quasi-Resonant PWM Controller

Features

- High Efficiency Across Wide Input and Output Conditions in a Small Form Factor
- Quasi-Resonant Switching Operation with Programmable Maximum Blanking Frequency Range (60 kHz – 140 kHz)
- User Configurable Burst Mode Entry and Exit to Maximize Light Load Efficiency and Minimize Audible Noise
- Adaptive Burst Mode Entry Level for Adaptive Charger Application
- mWSaver® Technology for Ultra Low Standby Power Consumption (< 20 mW)
- Forced and Inherent Frequency Modulation of Valley Switching for Low EMI Emissions and Common Mode Noise
- Built-In and User Configurable Over-Voltage Protection (OVP), Under-Voltage Protection (UVP) and Over-Temperature Protection (OTP)
- Fully Programmable Brown-In and Brownout Protection
- Precise Constant Output Current Regulation with Programmable Line Compensation
- Built-In High-Voltage Startup to Reduce External Components
- 10 Lead SOIC JEDEC

Applications

- Battery Charges for Smart Phones, Feature Phones, and Tablet PCs
- AC-DC Adapters for Portable Devices or Battery Chargers that Require CV/CC Control

Description

The FAN602 is an advanced PWM controller aimed at achieving power density of ≥10W/in³ in universal input range AC/DC flyback isolated power supplies. It incorporates Quasi-Resonant (QR) control with proprietary Valley Switching with a limited frequency variation. QR switching provides high efficiency by reducing switching losses while Valley Switching with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

FAN602 features mWSaver® burst mode operation with extremely low operating current (300 μA) and significantly reduces standby power consumption to meet the most stringent efficiency regulations such as Energy Star’s 5-Star Level and CoC Tier II specifications.

FAN602 includes several user configurable features aimed at optimizing efficiency, EMI and protections. FAN602 has a programmable blanking frequency range that provides flexibility in choosing noise rejection in targeted frequency zones. It incorporates user-configurable minimum peak current, which allows controlling the burst mode entry/exit power level, thereby enhancing light-load efficiency and eliminating audible noise. It also includes several rich programmable protection features such as over-voltage protection (OVP), precise constant output current regulation (CC).

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN602MX</td>
<td>-40°C to +125°C</td>
<td>10-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch Narrow Body</td>
<td>Tape &amp; Reel</td>
</tr>
</tbody>
</table>
Typical Application

Figure 1. FAN602 Typical Application

Block Diagram

Figure 2. FAN602 Block Diagram
Marking Information

FAN602 MX
ZXYTT TM

F- Fairchild Logo
Z: Assembly Plant Code
X: Year Code
Y: Week Code
T: Die Run Code
TM: Package Type (M=SOIC)
M: Manufacture Flow Code

Pin Configuration

![Pin Configuration Diagram]

Figure 3. Top Mark

Pin Definitions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>HV</td>
<td>High Voltage. This pin connects to DC bus for high-voltage startup.</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>3</td>
<td>CS</td>
<td>Current Sense. This pin connects to a current-sense resistor to sense the MOSFET current for Peak-Current-Mode control for output regulation. The current sense information is also used to estimate the output current for CC regulation.</td>
</tr>
<tr>
<td>4</td>
<td>GATE</td>
<td>PWM Signal Output. This pin has an internal totem-pole output driver to drive the power MOSFET. The gate driving voltage is internally clamped at 7.5 V.</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
<td>Power Supply. IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external VDD capacitor.</td>
</tr>
<tr>
<td>6</td>
<td>VS</td>
<td>Voltage Sense. The VS voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage. It also senses input voltage for Brownout protection.</td>
</tr>
<tr>
<td>7</td>
<td>FMAX</td>
<td>Maximum Blanking Frequency. This pin connects to external resistor to program maximum blanking frequency.</td>
</tr>
<tr>
<td>8</td>
<td>IMIN</td>
<td>Minimum Vcs. This pin connects to external resistor to program minimum VCS Threshold level for burst mode operating optimization.</td>
</tr>
<tr>
<td>9</td>
<td>FB</td>
<td>Feedback. Typically Opto-Coupler is connected to this pin to provide feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in CV regulation.</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>Ground.</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{HV}$</td>
<td>HV Pin Input Voltage</td>
<td>500</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{VDD}$</td>
<td>DC Supply Voltage</td>
<td>30</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{VS}$</td>
<td>VS Pin Input Voltage</td>
<td>-0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CS}$</td>
<td>CS Pin Input Voltage</td>
<td>-0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>FB Pin Input Voltage</td>
<td>-0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FMAX}$</td>
<td>FMAX Pin Input Voltage</td>
<td>-0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IMIN}$</td>
<td>IMIN Pin Input Voltage</td>
<td>-0.3</td>
<td>6.0</td>
<td>V</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation ($T_A=25^\circ$C)</td>
<td>850</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>Thermal Resistance (Junction-to-Ambient)</td>
<td>140</td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>$\Psi_{JT}$</td>
<td>Thermal Resistance (Junction-to-Top)</td>
<td>13</td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating Junction Temperature</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature Range</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_L$</td>
<td>Lead Temperature, (Wave soldering or IR, 10 Seconds)</td>
<td>+260</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>ESD(3)</td>
<td>Electrostatic Discharge Capability</td>
<td>Human Body Model, JEDEC:JESD22_A114 (Except HV Pin)</td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Charged Device Model, JEDEC:JESD22_C101 (Except HV Pin)</td>
<td>2.0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD ratings including HV pin: HBM=2.0 kV, CDM=2.0 kV.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{HV}$</td>
<td>HV Pin Supply Voltage</td>
<td>50</td>
<td></td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td>$V_{VDD}$</td>
<td>VDD Pin Supply Voltage</td>
<td>6</td>
<td>15</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{VS}$</td>
<td>VS Pin Supply Voltage</td>
<td>0.65</td>
<td>2.90</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{CS}$</td>
<td>CS Pin Supply Voltage</td>
<td>0</td>
<td>0.9</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>FB Pin Supply Voltage</td>
<td>0</td>
<td>5.25</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{FMAX}$</td>
<td>FMAX Pin Supply Voltage</td>
<td>0</td>
<td>1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IMIN}$</td>
<td>IMIN Pin Supply Voltage</td>
<td>0</td>
<td>2.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating Temperature</td>
<td>-40</td>
<td></td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>
### Electrical Characteristics

$V_{DD}=15 \text{ V and } T_J=40\text{~to~}125 \, ^\circ\text{C unless noted.}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HV Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{HV}$</td>
<td>Supply Current Drawn from HV Pin</td>
<td>$V_{HV}=120 \text{ V, } V_{DD}=0 \text{ V}$</td>
<td>1.2</td>
<td>2.0</td>
<td>10.0</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{HV-LC}$</td>
<td>Leakage Current Drawn from HV Pin</td>
<td>$V_{HV}=500 \text{ V, } V_{DD}=V_{DD-OFF}+1 \text{ V}$</td>
<td>0</td>
<td>0.8</td>
<td>10.0</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{Brown-IN}$</td>
<td>Brown-In Threshold Voltage.</td>
<td>$R_{HV}=150 , \text{k}\Omega, , V_{IN}=80 , \text{V}_{\text{rms}}$</td>
<td>100</td>
<td>110</td>
<td>120</td>
<td>V</td>
</tr>
<tr>
<td><strong>V_{DD} Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD-ON}$</td>
<td>Turn-On Threshold Voltage</td>
<td>$V_{DD}$ Rising</td>
<td>15.3</td>
<td>17.2</td>
<td>18.7</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DD-OFF}$</td>
<td>Turn-Off Threshold Voltage</td>
<td>$V_{DD}$ Falling</td>
<td>5.0</td>
<td>5.5</td>
<td>5.7</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DD-HV-ON}$</td>
<td>Threshold Voltage for HV Startup</td>
<td>$T_J=25, ^\circ\text{C}$</td>
<td>4.1</td>
<td>4.7</td>
<td>5.4</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD-ST}$</td>
<td>Startup Current</td>
<td>$V_{DD}=V_{DD-ON}=0.16 , \text{V, } T_J=25, ^\circ\text{C}$</td>
<td>300</td>
<td>400</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{DD-OP}$</td>
<td>Operating Supply Current</td>
<td>$V_{CS}=5.0 , \text{V, } V_S=3 , \text{V, } V_{FB}=3 , \text{V, } V_{DD}=15 , \text{V, } C_{\text{GATE}}=1 , \text{nF}$</td>
<td>2</td>
<td>3</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DD-Burst}$</td>
<td>Burst-Mode Operating Supply Current</td>
<td>$V_{CS}=0.3 , \text{V, } V_S=0 , \text{V, } V_{FB}=0 , \text{V, } V_{DD}=V_{DD-ON}\rightarrow V_{DD-OVP}\rightarrow 10 , \text{V, } C_{\text{GATE}}=1 , \text{nF}$</td>
<td>300</td>
<td>600</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$V_{DD-OVP}$</td>
<td>VDD Over-Voltage-Protection Level</td>
<td>$T_J=25, ^\circ\text{C}$</td>
<td>27.5</td>
<td>29.0</td>
<td>29.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{D-VD-OVP}$</td>
<td>VDD Over-Voltage-Protection Debounce Time</td>
<td></td>
<td>70</td>
<td>105</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td><strong>Oscillator Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{MAX}$</td>
<td>FMAX Pin Current</td>
<td></td>
<td>18</td>
<td>20</td>
<td>22</td>
<td>μA</td>
</tr>
<tr>
<td>$f_{BNK-MAX}$</td>
<td>Maximum Blanking Frequency</td>
<td>$R_{FMAX}=0$</td>
<td>130</td>
<td>140</td>
<td>150</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{BNK-MIN}$</td>
<td>Minimum Blanking Frequency</td>
<td>$R_{FMAX}=48.3 , \text{k}\Omega$</td>
<td>50</td>
<td>60</td>
<td>65</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{OSC-MIN-DCM}$</td>
<td>Minimum Frequency for DCM</td>
<td>$V_{SS}=0 , \text{V}$</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>kHz</td>
</tr>
<tr>
<td>$f_{OSC-MIN-CRM}$</td>
<td>Minimum Frequency for CrM</td>
<td>$V_{SS}=1 , \text{V, } T_J=25, ^\circ\text{C}$</td>
<td>11</td>
<td>20</td>
<td>29</td>
<td>kHz</td>
</tr>
<tr>
<td>$\Delta f_{FM}$</td>
<td>Forced Frequency Modulation Range$^{(4)}$</td>
<td>$V_{FB} &gt; V_{FB-Burst-H}$</td>
<td>225</td>
<td>265</td>
<td>305</td>
<td>ns</td>
</tr>
<tr>
<td>$\Delta f_{FM}$</td>
<td>Forced Frequency Modulation Period$^{(4)}$</td>
<td></td>
<td>2.1</td>
<td>2.5</td>
<td>2.9</td>
<td>ms</td>
</tr>
<tr>
<td><strong>Feedback Input Section</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Z_{FB}$</td>
<td>FB Pin Input Impedance</td>
<td></td>
<td>39</td>
<td>42</td>
<td>45</td>
<td>kΩ</td>
</tr>
<tr>
<td>$A_{V}$</td>
<td>Internal Voltage Attenuator of FB Pin$^{(4)}$</td>
<td>$V_{HV}=120 , \text{V}<em>{\text{DC}, } V</em>{DD}=0 , \text{V}$</td>
<td>1/3</td>
<td>1/3.5</td>
<td>1/4</td>
<td>V/V</td>
</tr>
<tr>
<td>$V_{FB-Open}$</td>
<td>FB Pin Pull-Up Voltage</td>
<td>FB Pin Open</td>
<td>4.75</td>
<td>5.25</td>
<td>5.90</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB-Burst-H}$</td>
<td>FB Threshold to Enable/Disable Gate Drive in Burst Mode</td>
<td>$V_{FB}$ Rising</td>
<td>1.15</td>
<td>1.25</td>
<td>1.35</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB-Burst-L}$</td>
<td></td>
<td>$V_{FB}$ Falling</td>
<td>1.1</td>
<td>1.2</td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB-BNK-H}$</td>
<td>Frequency Fold-back Starting/Stopping</td>
<td>$V_{FB}$</td>
<td>1.75</td>
<td>2.05</td>
<td>2.35</td>
<td>V</td>
</tr>
<tr>
<td>$V_{FB-BNK-L}$</td>
<td></td>
<td></td>
<td>1.2</td>
<td>1.5</td>
<td>1.8</td>
<td>V</td>
</tr>
</tbody>
</table>

Continued on the following page...
**Electrical Characteristics**

$V_{DD}=15\,V$ and $T_{J}=40\sim125\,^\circ C$ unless noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{VS_MAX}$</td>
<td>Maximum $V_S$ Source Current Capability</td>
<td></td>
<td>3</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{VS_BNK1}$</td>
<td>$V_S$ Sampling Blanking Time 1 after GATE Pin Pull-Low</td>
<td>$V_{FB} &lt; 2.0,V$</td>
<td>0.9</td>
<td>1.1</td>
<td>1.37</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{VS_BNK2}$</td>
<td>$V_S$ Sampling Blanking Time 2 after GATE Pin Pull-Low</td>
<td>$V_{FB} &gt; 2.2,V$, $T_J = 25^\circ C$</td>
<td>1.6</td>
<td>1.8</td>
<td>2.1</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{ZCD_to_PWM}$</td>
<td>Delay from VS Voltage Zero Crossing to PWM ON(5)</td>
<td>$V_{VS}=0,V$, $C_{GATE}=1,nF$</td>
<td>175</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$I_{VS_Brownout}$</td>
<td>$V_S$ Source Current Threshold to Enable Brownout</td>
<td>Set $I_{VS}=2.4,mA$ at 264 $V_{rms}$, Brownout=55 $V_{rms}$</td>
<td>370</td>
<td>450</td>
<td>520</td>
<td>μA</td>
</tr>
<tr>
<td>$t_{D_Brownout}$</td>
<td>Brownout Debounce Time</td>
<td></td>
<td>12.5</td>
<td>16.5</td>
<td>21.0</td>
<td>ms</td>
</tr>
<tr>
<td>$V_{VS_OVP}$</td>
<td>Output Over-Voltage-Protection with $V_S$ Sampling Voltage</td>
<td></td>
<td>2.8</td>
<td>2.9</td>
<td>3.0</td>
<td>V</td>
</tr>
<tr>
<td>$N_{VS_OVP}$</td>
<td>Output Over-Voltage-Protection Debounce Cycle Counts</td>
<td></td>
<td>2</td>
<td>Cycle</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{VS_UVP-H}$</td>
<td>Output Under-Voltage-Protection with $V_S$ Sampling Voltage</td>
<td>$T_J=25^\circ C$</td>
<td>0.76</td>
<td>0.80</td>
<td>0.84</td>
<td>V</td>
</tr>
<tr>
<td>$V_{VS_UVP-L}$</td>
<td>Output Under-Voltage-Protection with $V_S$ Sampling Voltage</td>
<td>$T_J=25^\circ C$</td>
<td>0.625</td>
<td>0.650</td>
<td>0.675</td>
<td>V</td>
</tr>
<tr>
<td>$N_{VS_UVP}$</td>
<td>Output Over-Voltage-Protection Debounce Cycle Counts</td>
<td></td>
<td>2</td>
<td>Cycle</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{VS_UVP_BLANK}$</td>
<td>Output Under-Voltage Protection Blanking Time at Startup</td>
<td>$V_{S_SH} &lt; V_{VS_UVP}$</td>
<td>25</td>
<td>40</td>
<td>55</td>
<td>ms</td>
</tr>
<tr>
<td>$N_{VDD_Hiccup}$</td>
<td>Auto-Restart 2 Cycles Mode Counts</td>
<td></td>
<td>2</td>
<td>Cycle</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{OTP}$</td>
<td>Threshold Temperature for Over-Temperature-Protection(4)</td>
<td></td>
<td>140</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**Current-Sense Section**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CS_LIM}$</td>
<td>Current Limit Threshold Voltage</td>
<td>FB Pin Open</td>
<td>0.85</td>
<td>0.9</td>
<td>0.95</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IMIN}$</td>
<td>IMIN Pin Current</td>
<td></td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{CS_IMIN_MIN}$</td>
<td>Minimum Current Sense Voltage</td>
<td>$V_{S_SH}=2.5,V$, $R_{IMIN}=250,k\Omega$</td>
<td>0.14</td>
<td>0.18</td>
<td>0.23</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CS_IMIN_MAX}$</td>
<td>Maximum Current Sense Voltage</td>
<td>$V_{S_SH}=2.5,V$, $R_{IMIN}=0,Ω$</td>
<td>0.40</td>
<td>0.44</td>
<td>0.50</td>
<td>V</td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>GATE Output Turn-Off Delay</td>
<td></td>
<td>100</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{LEB}$</td>
<td>Leading-Edge Blanking Time</td>
<td></td>
<td>150</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Continued on the following page...
### Electrical Characteristics

$V_{DD}=15\,\text{V}$ and $T_J=-40\sim125\,\text{°C}$ unless noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I$_{COMP-H}$</td>
<td>High Line Compensation Current</td>
<td>$V_{IN} = 264,\text{V}_{\text{rms}}$</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>I$_{COMP-L}$</td>
<td>Low Line Compensation Current</td>
<td>$V_{IN} = 90,\text{V}_{\text{rms}}$</td>
<td>32</td>
<td>36</td>
<td>40</td>
<td>$\mu\text{A}$</td>
</tr>
</tbody>
</table>

**Constant Current Correction Section**

- **I$_{COMP-H}$**: High Line Compensation Current. ($V_{IN} = 264\,\text{V}_{\text{rms}}$)
  - Min: 90 $\mu\text{A}$
  - Typ: 100 $\mu\text{A}$
  - Max: 110 $\mu\text{A}$
- **I$_{COMP-L}$**: Low Line Compensation Current. ($V_{IN} = 90\,\text{V}_{\text{rms}}$)
  - Min: 32 $\mu\text{A}$
  - Typ: 36 $\mu\text{A}$
  - Max: 40 $\mu\text{A}$

**Constant Current Estimator**

- **$V_{REF_{-CC}}$**: Constant Current Control Reference Voltage ($V_{DD}=15\,\text{V}$)
  - Min: 1.2 V
- **$A_{PK}$**: Peak Value Amplifying Gain ($V_{DD}=15\,\text{V}$)
  - Min: 3.6 V/V
- **$V_{FB_{-CC\_Open}}$**: FB CC Pull-Up Voltage ($V_{DD}=15\,\text{V}$)
  - Min: 4.0 V
- **$A_{V_{-CC}}$**: Internal Voltage Attenuator of FB CC ($V_{DD}=15\,\text{V}$)
  - Min: 0.444 V/V

**GATE Section**

- **$V_{GATE-L}$**: Gate Output Voltage Low
  - Min: 0 V
  - Typ: 1.5 V
- **$V_{DD_{-PMOS\_ON}}$**: Internal Gate PMOS Driver ON
  - Min: 7.0 V
  - Typ: 7.5 V
  - Max: 8.0 V
- **$V_{DD_{-PMOS\_OFF}}$**: Internal Gate PMOS Driver OFF
  - Min: 9.0 V
  - Typ: 9.5 V
  - Max: 10.0 V
- **$t_r$**: Rising Time
  - Min: 100 ns
  - Typ: 135 ns
  - Max: 180 ns
- **$t_f$**: Falling Time
  - Min: 30 ns
  - Typ: 50 ns
  - Max: 70 ns
- **$V_{GATE\_CLAMP}$**: Gate Output Clamping Voltage
  - Min: 6.8 V
  - Typ: 7.5 V
  - Max: 8.2 V
- **$V_{ON_{-MAX}}$**: Maximum On Time
  - Min: 18 $\mu$s
  - Typ: 20 $\mu$s
  - Max: 23 $\mu$s

**Note:**
4. Guaranteed by design.
Typical Performance Characteristics

Figure 5. Turn-On Threshold Voltage ($V_{DD-ON}$) vs. Temperature

Figure 6. Turn-Off Threshold Voltage ($V_{DD-OFF}$) vs. Temperature

Figure 7. Operating Supply Current ($I_{DD-OP}$) vs. Temperature

Figure 8. Burst-Mode Operating Supply Current ($I_{DD-Burst}$) vs. Temperature

Figure 9. Maximum Blanking Frequency ($f_{BNK-MAX}$) vs. Temperature

Figure 10. Minimum Blanking Frequency ($f_{BNK-MIN}$) vs. Temperature
Typical Performance Characteristics (Continued)

**Figure 11.** Minimum Frequency for CrM \( (f_{OSC-MIN-CrM}) \) vs. Temperature

**Figure 12.** Frequency Fold-back Starting \( (V_{FB-BNK-H}) \) vs. Temperature

**Figure 13.** Frequency Fold-back Stopping \( (V_{FB-BNK-L}) \) vs. Temperature

**Figure 14.** \( V_S \) Sampling Blanking Time 1 \( (t_{VS-BNK1}) \) vs. Temperature

**Figure 15.** \( V_S \) Sampling Blanking Time 2 \( (t_{VS-BNK2}) \) vs. Temperature

**Figure 16.** Output Over-Voltage-Protection \( (V_{VS-OVP}) \) vs. Temperature
Typical Performance Characteristics (Continued)

Figure 17. Output Under-Voltage Protection ($V_{VS-UVP-H}$) vs. Temperature

Figure 18. Output Under-Voltage Protection ($V_{VS-UVP-L}$) vs. Temperature

Figure 19. Maximum Current Sense Voltage ($V_{CS-IMIN-MAX}$) vs. Temperature

Figure 20. Minimum Current Sense Voltage ($V_{CS-IMIN-MIN}$) vs. Temperature

Figure 21. Current Limit Threshold Voltage ($V_{CS-LIM}$) vs. Temperature

Figure 22. Maximum On Time ($t_{ON-MAX}$) vs. Temperature
Functional Description

FAN602 is an offline PWM controller which operates in a quasi-resonant (QR) mode and significantly enhances system efficiency and power density. Its control method is based on the load condition (valley switching with fixed blanking time at heavy load and valley switching with variable blanking time at medium load) to maximize the efficiency. FMAX pin allows programming the maximum blanking frequency. It offers constant output voltage (CV) regulation through opto-coupler feedback circuitry.

Line voltage compensation gain can be programmed by using an external resistor to minimize the effect of line voltage variation on output current regulation due to turn-off delay of the side drive circuit. FAN602 incorporates HV startup and accurate brown-in through HV pin. The brown-in voltage is programmed by using an external HV pin resistor. The minimum peak current (VCC_min) which controls the burst mode entry/exit and improves light-load efficiency, is programmable via an external resistor connected to the IMIN pin.

Basic Operation Principle

Quasi-resonant switching is a method to reduce primary MOSFET switching losses especially in high line. In order to perform QR turn-on of the primary MOSFET, the valley of the resonance occurring between transformer magnetizing inductance (L_m) and MOSFET effective output capacitance (C_{oss-eff}) must be detected.

$$C_{oss-eff} = C_{oss-MOSFET} + C_{trans} + C_{parasitic}$$

(1)

$$t_{resonance} = 2\pi \cdot \sqrt{L_m \cdot C_{oss-eff}}$$

(2)

For heavy load condition (50%~100% of full load), the blanking time to the valley detection is fixed such that the switching time is between t_{BNK MIN} and f_{BNK RESONANCE}. The upper limit of the blanking frequency is programmed by FMAX pin. For the medium load condition (25%~50% of full load), the blanking time is modulated as a function of load current such that the upper limit of the blanking frequency varies from f_{BNK MAX} as load decreases where the blanking frequency reduction stop point is f_{BNK MIN}.

Valley Detection

There will be a logic propagation delay from VS Zero-Crossing Detection (V_{S-ZCD}) to IC GATE turn on and a MOSFET gate drives propagation delay from GATE pin to MOSFET turn on. We can assume the sum of these propagation delays to be t_{ZCD-B-PWM}, as shown in Figure 27. However, if 1/2 t_r is larger than t_{ZCD-B-PWM}, the switching occurs away from the valley causing higher losses. The time period of resonant ringing is dependent on L_m and C_{oss-eff}. Typically, the time period of resonance ringing is around 1~1.5 µs depending on the system parameters. Hence, the switching may occur at a point different from the valley depending on the system. When PCB layout is poor, it may cause noise on the VS pin. The VS pin needs to be in parallel with the capacitor (CVS) less than 10 pF to filter the noise.

The Maximum Blanking Frequency Selection

The FAN602 allows adjusting the maximum blanking frequency (f_{BNK MAX}) of operation through an external resistor on the FMAX pin. As shown in Figure 24, an internal current source of 20 µA creates a voltage V_{FMAX} across the resistance, R_{FMAX}. This voltage sets the oscillator reference voltage which determines f_{BNK MIN}.
Output Voltage Detection

Figure 30 shows the VS voltage is sampled (\(V_{S-SH}\)) after \(t_{VS-BNK}\) of GATE turn-off so that the ringing does not introduce any error in the sampling. FAN602 dynamically varies \(t_{VS-BNK}\) with load. At heavy load, \(t_{VS-BNK} = \frac{1}{2} t_{F}\) (1.8 \(\mu\)s) when \(V_{FB} > 2.2\) V. At light-load, \(t_{VS-BNK} = \frac{1}{2} t_{F}\) (1.1 \(\mu\)s) when \(V_{FB} < 2\) V. This dynamic variation ensures that VS sampling occurs after ringing due to leakage inductance has stopped and before secondary current goes to zero.

\[
V_{S-SH} = V_{o} \cdot \frac{N_{a}}{N_{s}} \cdot \frac{R_{VS2}}{R_{VS1} + R_{VS2}}
\]

\[\text{(3)}\]

Burst Mode Operation

FAN602 features burst mode operation with a programmable burst mode entry load condition by using minimum peak current (\(V_{CS-IMIN}\)) control which enables light-load efficiency to be optimized for a given application. The IMIN pin can be programmed with external resistor \(R_{IMIN}\) to select the minimum \(V_{CS}\) threshold level for burst mode entry. Figure 31 shows the implementation of IMIN in FAN602.

Figure 32 shows when \(V_{FB}\) drops below \(V_{FB-\text{Burst-L}}\), the PWM output shuts off and the output voltage drops at a rate which is depended on the load current level. This causes the feedback voltage to rise. Once \(V_{FB}\) exceeds \(V_{FB-\text{Burst-H}}\), FAN602 resumes switching. As shown in Figure 33, when the FB voltage drops below the corresponding \(V_{CS-IMIN}\), the peak currents in switching cycles are fixed to \(V_{CS-IMIN}\) regardless of FB voltage. Thus, more power is delivered to the load than required and once FB voltage is pulled low below \(V_{FB-\text{Burst-L}}\), switching stops again. In this manner, the burst mode operation alternately enables and disables switching of the MOSFET to reduce the switching losses.

For adaptive output application, the minimum peak current is modulated in accordance with the \(V_{S-SH}\) such that the minimum peak current is proportional to the square root of output voltage. For easy circuit implementation, curve fitting is used as shown in Figure 34.

\[
V_{CS-IMIN} = \frac{(V_{S-SH} - I_{MIN} \times R_{IMIN})}{10} + 0.2
\]

\[\text{(4)}\]
Deep Burst Mode

FAN602 enters deep burst mode if FB voltage stays lower than $V_{FB\text{-Burst-L}}$ for more than $t_{\text{Deep-Burst-Entry}}$ (640 ms). Once FAN602 enters deep burst mode, the operating current is reduced to $I_{D\text{D-Burst}}$ (300 μA) to minimize power consumption. Once feedback voltage is more than $V_{FB\text{-Burst-H}}$, power-on-reset occurs within a time period of $t_{\text{Deep-Burst-Exit}}$ (25 μs) and IC resumes switching with normal operating current, $I_{D\text{D-OP}}$.

Line Voltage Detection

The FAN602 indirectly senses the line voltage through the VS pin while the MOSFET is turned on, as illustrated in Figure 35 and Figure 36. During MOSFET turn-on period, the auxiliary winding voltage, $V_{AUX}$, is proportional to the input bulk capacitor voltage, $V_{BLK}$, due to the transformer coupling between the primary and auxiliary windings. During the MOSFET conduction time, the line voltage detector clamps the VS pin voltage to $V_{S\text{-Clamp}}$ (0 V), and then the current $I_{VS}$ flowing out of VS pin is expressed as:

$$I_{VS} = \frac{V_{BLK} \cdot N_A}{R_{VS1} \cdot N_S}$$  \hspace{1cm} (5)

The $I_{VS}$ current, reflecting the line voltage information, is used for brownout protection and CC control correction weighting.

Line Voltage Detection Circuit

The $I_{VS}$ current, reflecting the line voltage information, is used for brownout protection and CC control correction weighting.
CV / CC PWM Operation Principle

Figure 37 shows a simplified CV / CC PWM control circuit of the FAN602. The Constant Voltage (CV) regulation is implemented in the same manner as the conventional isolated power supply, where the output voltage is sensed using a voltage divider and compared with the internal reference of the shunt regulator to generate a compensation signal. The compensation signal is transferred to the primary side through an optocoupler and scaled down by attenuator $A_v$ to generate a COMV signal. This COMV signal is applied to the PWM comparator to determine the duty cycle.

The Constant Current (CC) regulation is implemented internally with primary-side control. The output current estimator calculates the output current using the transformer primary-side current and diode current discharge time. By comparing the estimated output current with internal reference signal, a COMI signal is generated to determine the duty cycle.

These two control signals, COMV and COMI, are compared with an internal sawtooth waveform ($V_{SAW}$) by two PWM comparators to determine the duty cycle. Figure 38 illustrates the outputs of two comparators, combined with an OR gate, to determine the MOSFET turn-off instant. Either of COMV or COMI, the lower signal determines the duty cycle. As shown in Figure 38, during CV regulation, COMV determines the duty cycle while COMI is saturated to HIGH level. During CC regulation, COMI determines the duty cycle while COMV is saturated to HIGH level.

Primary-Side Constant Current Operation

Figure 39 shows the key waveforms of a flyback converter operating in DCM. The output current is estimated by calculating the average of output diode current in one switching cycle:

$$ I_o = \frac{1}{2} \frac{1}{R_{CS}} \frac{V_{CS-PK} \cdot T_{dis} \cdot N_P}{T_S} = \frac{1}{2} \frac{1}{R_{CS}} \frac{V_{REF,CC} \cdot N_P}{A_{PK}} \eta $$

(6)

When the diode current reaches zero, the transformer winding voltage begins to drop sharply and VS pin voltage drops as well. When VS pin voltage drops below the $V_{S-SH}$ by more than 500 mV, Zero Current Detection (ZCD) of diode current is obtained.

The output current can be programmed by setting the current sensing resistor as:

$$ R_{CS} = \frac{1}{2} \frac{1}{I_o} \frac{V_{REF,CC}}{A_{PK}} \frac{N_P}{N_S} \eta $$

(7)

Where $V_{REF,CC}$ is the internal voltage for CC control and $A_{PK}$ is the IC design parameter, 3.6 for FAN602.

![Figure 37. Simplified PWM Control Circuit](image)

![Figure 38. PWM Operation for CV/CC Regulation](image)

Line Voltage Compensation

The output current estimation is also affected by the turn-off delay of the MOSFET as illustrated in Figure 40. The actual MOSFET’s turn-off time is delayed due to the MOSFET gate charge and gate driver’s capability, resulting in peak current detection error as:

$$ \Delta I_{DS-PK} = \frac{V_{BLK}}{L_m} \cdot t_{OFF,DLV} $$

(8)

Where $L_m$ is the transformer’s primary side magnetizing inductance. Since the output current error is proportional to the line voltage, the FAN602 incorporates line voltage compensation to improve output current estimation accuracy. Line information is obtained through the line voltage detector as shown in Figure 35. $I_{COMP}$ is an internal current source, which is proportional to line voltage. The line compensation gain is programmed by
using CS pin series resistor, $R_{CS,COMP}$, depending on the MOSFET turn-off delay, $t_{OFF.DLY}$. $I_{COMP}$ creates a voltage drop, $V_{OFFSET}$, across $R_{CS,COMP}$. This line compensation offset is proportional to the DC link capacitor voltage, $V_{BLK}$, and turn-off delay, $t_{OFF.DLY}$. Figure 41 demonstrates the effect of the line compensation. When PCB layout is poor, it may cause noise on the CS pin. The CS pin needs to be in parallel with the capacitor ($C_{COMP}$) less than 20 pF to filter the noise.

**Figure 40. Effect of MOSFET Turn-off Delay**

**Figure 41. Line Voltage Compensation**

**CCM Prevention**

When input or output voltage drops, the secondary side current does not reduce to zero within $t_{OSC-MIN-DCM}$ (time period for $f_{OSC-MIN-DCM}$). FAN602 does not initiate turn-on. FAN602 turns on the primary MOSFET after VS-ZCD and ensures boundary conduction mode switching. Thus FAN602 does not allow the converter to enter CCM. During CCM prevention, FAN602 can reduce the frequency down to $f_{OSC-MIN-CM}$ (20 kHz). This phenomenon is explained in Figure 42.

**HV Startup and Brown-In**

Figure 43 shows the High-Voltage (HV) startup circuit. An internal JFET provides a high voltage current source, whose characteristics are shown in Figure 44. To improve reliability and surge immunity, it is typical to use a $R_{HV}$ resistor between the HV pin and the bulk capacitor voltage. The actual current flowing into the HV pin at a given bulk capacitor voltage and startup resistor value is determined by the intersection point of characteristics I-V line and the load line as shown in Figure 44.

During startup, the internal startup circuit is enabled and the bulk capacitor voltage supplies the current, $I_{HV}$, to charge the hold-up capacitor, $C_{VDD}$, through $R_{HV}$. When the $V_{DD}$ voltage reaches $V_{DD,ON}$, the sampling circuit shown in Figure 43 is turned on for $t_{HV,ON}$ (100 μs) to sample the bulk capacitor voltage. Voltage across $R_{LS}$ is compared with reference which generates a signal to start switching. If brown-in condition is not detected during this time, switching does not start. Equation (9) can be used to program the brown-in of the system. If line voltage is lower than the programmed brown-in voltage, FAN602 goes in auto-restart mode.

\[
V_{IN} = \frac{R_{LS} + R_{JEFT} + R_{HV}}{R_{LS}} \times V_{REF}
\]

Once switching starts, the internal HV startup circuit is disabled. During normal switching, the line voltage information is obtained from the $I_{VS}$ signal. Once the HV startup circuit is disabled, the energy stored in $C_{VDD}$ supplies the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, $C_{VDD}$ should be properly designed to prevent $V_{DD}$ from dropping below $V_{DD-OFF}$ threshold (typically 5.5 V) before the auxiliary winding builds up enough voltage to supply $V_{DD}$. During startup, the IC current is limited to $I_{DSS}$ (300 μA).
HV startup circuit enable, then IC enters Extend Auto-Restart period with two cycles as shown Figure 46. During Extend Auto-Restart period, VDD voltage swings between VDD-ON and VDD-HV-ON without gate switching, and IC operation current is reduced to IDD-Burst of 300 μA for slowing down the VDD capacitor discharging slope. As Extend Auto-Restart period ends, normal operation resumes.

Figure 43. HV Startup Circuit

Figure 44. Characteristics of HV pin

Protections

The FAN602 protection functions include VDD Over-Voltage-Protection (VDD-OVP), brownout protection, VS Over-Voltage Protection (VS-OVP), VS Under-Voltage-Protection (VS-UVP), and IC internal Over-Temperature Protection (OTP). The VDD-OVP, brownout protection VS-OVP and OTP are implemented with Auto-Restart mode. The VS-UVP is implemented with Extend Auto-Restart mode.

When the Auto-Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing VDD to drop because of IC operating current IDD-OP (2 mA). When VDD drops to the VDD turn-off voltage of VDD-OFF (5.5 V), operation current reduces to IDD-Deep-Burst (300 μA). When the VDD voltage drops further to VDD-HV-ON, the protection is reset and the supply current drawn from HV pin begins to charge the VDD hold-up capacitor. When VDD reaches the turn-on voltage of VDD-ON (17.2 V), FAN602 resumes normal operation. In this manner, the Auto-Restart mode alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated as shown in Figure 45.

When the Extend Auto-Restart Mode protection is triggered via VS under-voltage protection (VS-UVP), switching is terminated and the MOSFET remains off, causing VDD to drop. While VDD drops to VDD-HV-ON for

VDD Over-Voltage-Protection (VDD-OVP)

VDD over-voltage protection prevents IC damage from over-voltage stress. It is operated in Auto-Restart mode. When the VDD voltage exceeds VDD-OVP (29.0 V) for the de-bounce time, tD-VDD-OVP (70 μs), due to abnormal condition, the protection is triggered. This protection is typically caused by an open circuit of secondary side feedback network.

Figure 45. Auto-Restart Mode Operation

Figure 46. Extend Auto-Restart Mode Operation
Brownout Protection

Line voltage information is also used for brownout protection. When the \( I_{\text{VS}} \) current out of the VS pin during the MOSFET conduction time is less than 450 \( \mu \)A for longer than 16.5 ms, the brownout protection is triggered. The input bulk capacitor voltage to trigger brownout protection is given as

\[
V_{BLK,BO} = 450 \mu \text{A} \frac{R_{VS1}}{N_A/N_p} \tag{10}
\]

IC Internal Over-Temperature-Protection (OTP)

The internal temperature-sensing circuit disables the PWM output if the junction temperature exceeds 140°C \((T_{\text{OTP}})\) and the FAN602 enters Auto-Restart Mode protection.

VS Over-Voltage-Protection (VS-OVP)

VS over-voltage protection prevents damage caused by output over-voltage condition. It is operated in Auto-Restart mode. Figure 47 shows the internal circuit of VS-OVP protection. When abnormal system conditions occur, which cause VS sampling voltage to exceed \( V_{\text{VS-OVP}} \) (2.9 V) for more than 2 consecutive switching cycles \((N_{\text{VS-OVP}})\), PWM pulses are disabled and FAN602 enters Auto-Restart protection. VS over-voltage conditions are usually caused by open circuit of the secondary-side feedback network or a fault condition in the VS pin voltage divider resistors. For VS pin voltage divider design, \( R_{\text{VS1}} \) is obtained from Equation (10), and \( R_{\text{VS2}} \) is determined by the desired VS-OVP protection function as:

\[
R_{\text{VS2}} = R_{\text{VS1}} \cdot \frac{1}{\frac{V_{\text{VS-OVP}}}{V_{\text{VS-OVP}}} \frac{N_A}{N_S} - 1} \tag{11}
\]

VS Under-Voltage-Protection (VS-UVP)

In the event of an output short, output voltage will drop and the primary peak current will increase. To prevent operation for a long time in this condition, FAN602 incorporates under-voltage protection through VS pin. Figure 48 shows the internal circuit for VS-UVP. By sampling the auxiliary winding voltage on the VS pin at the end of diode conduction time, the output voltage is indirectly sensed. When VS sampling voltage is less than \( V_{\text{VS-UVP}} \) (0.65 V) and longer than de-bounce cycles \( N_{\text{VS-UVP}} \), VS-UVP is triggered and the FAN602 enters Extend Auto-Restart Mode.

To avoid VS-UVP triggering during the startup sequence, a startup blanking time, \( t_{\text{VS-UVP-BLANK}} \) (45 ms), is included for system power on. For VS pin voltage divider design, \( R_{\text{VS1}} \) is obtained from Equation (10) and

\[
V_{O-\text{UVP}} = \frac{N_2}{N_A} \left( 1 + \frac{R_{\text{VS1}}}{R_{\text{VS2}}} \right) V_{\text{VS-UVP}} \tag{12}
\]

Pulse-by-Pulse Current Limit

During startup or overload condition, the feedback loop is saturated to high and is unable to control the primary peak current. To limit the current during such conditions, FAN602 has pulse-by-pulse current limit protection which forces the GATE to turn off when the CS pin voltage reaches the current limit threshold, \( V_{\text{CS-LIM}} \) (0.9 V).

Secondary-Side Diode Shot Protection

When the secondary-side diode is damaged, the slope of primary-side peak current will be sharp within leading-edge blanking time. To limit the current during such conditions, FAN602 has secondary side diode short protection which forces the GATE to turn off when the CS pin voltage reaches 1.6 V. After one switching cycle, it will operate in Auto-Restart mode as shown in Figure 49.

Current Sense Short Protection

Current sense short protection prevents damage caused by CS pin open or short to ground. After two switching cycle, it will operate in Auto-Restart mode. Figure 49 shows the internal circuit of current sense short protection. When abnormal system conditions occur, which cause CS pin voltage lower than 0.2 V after debounce time \( (\text{ICS-short}) \) for more than 2 consecutive switching cycles, PWM pulses are disabled and FAN602 enters Auto-Restart protection. The \( \text{ICS-short} \) is an internal current source, which is proportional to line voltage. The debounce time \( (\text{ICS-short}) \) is created by \( \text{ICS-short} \), capacitor (2 pF) and threshold voltage (2.4 V). This debounce time \( (\text{ICS-short}) \) is inversely proportional to the DC link capacitor voltage, \( V_{\text{BLK}} \).
NOTES:
A. THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MS-012.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRRS.
D. LAND PATTERN STANDARD: SOIC127P600X175.10M
E. DRAWING FILENAME: MKT-M10ArevB