Li-Ion Switching Charger, High Efficiency, 1.55 A, with Integrated Power Path, USB-OTG, in a Small Solution Size

FAN54063

Description
The FAN54063 is a 1.55 A USB−compliant switch−mode charger featuring integrated power path operation, USB OTG boost support, JEITA temperature control, and production test mode support, in a small 25 bump, 0.4 mm pitch WLCSP package.

To facilitate fast system startup, the IC includes an integrated power path circuit, which disconnects the battery from the system rail, ensuring that the system can power up quickly following a VBUS connection. The power path circuit ensures that the system rail stays up when the charger is plugged in, even if the battery is dead.

The charging parameters and operating modes are programmable through an I2C Interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of external passive components.

The FAN54063 provides battery charging in three phases: conditioning, constant current and constant voltage. The IC automatically restarts the charge cycle when the battery falls below a voltage threshold. If the input source is removed, the IC enters a high−impedance mode blocking battery current from leaking to the input. Charger status is reported back to the host through the I2C port.

Dynamic input voltage control prevents a weak adapter’s voltage from collapsing, ensuring charging capability from such adapters.

The FAN54063 is available in a space saving 2.4 mm x 2.0 mm WLCSP package.

Features
• Fully Integrated, High−Efficiency Switch−Mode Charger for Single−Cell Li−Ion and Li−Polymer Batteries
• Integrated Power Path Circuit Ensures Fast System Startup with a Dead Battery when VBUS is Connected
• 1.55 A Maximum Charge Current
• Programmable High Accuracy Float Voltage:
  ♦ ±0.5% at 25°C
  ♦ ±1% from 0 to 125°C
• ±5% Input and Charge Current Regulation Accuracy
• Temperature−Sense Input for JEITA Compliance
• Thermal Regulation and Shutdown
• 4.2 V at 2.3 A Production Test Support
• 5 V, 500 mA Boost Mode for USB OTG

Features (continued)
• 28 V Absolute Maximum Input Voltage
• 6 V Maximum Input Operating Voltage
• Programmable through High−Speed I2C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  ♦ Input Current
  ♦ Fast−Charge / Termination Current
  ♦ Float Voltage
  ♦ Termination Enable
• 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
• Small Footprint 1 µH External Inductor
• Safety Timer with Reset Control
• Dynamic Input Voltage Control
• Very Low Battery Current when Charger Inactive

Applications
• Cell Phones, Smart Phones, PDAs
• Tablet, Portable Media Players
• Gaming Device, Digital Cameras

MARKING DIAGRAM

See detailed ordering and shipping information on page 2 of this data sheet.
Figure 1. Typical Application

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Temperature Range</th>
<th>Package</th>
<th>PN Bits: IC_INFO[5:3]</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN54063UCX</td>
<td>−40 to 85°C</td>
<td>25-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.4 mm Pitch</td>
<td>010</td>
<td>Tape and Reel</td>
</tr>
</tbody>
</table>

Table 1. FEATURE SUMMARY

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Slave Address</th>
<th>Automatic Charge</th>
<th>Battery Absent Behavior</th>
<th>E1 Pin</th>
<th>Watchdog Timer Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN54063</td>
<td>1101011</td>
<td>No</td>
<td>On</td>
<td>POK_B</td>
<td>Disabled</td>
</tr>
</tbody>
</table>
Figure 2. IC and System Block Diagram

Table 2. RECOMMENDED EXTERNAL COMPONENTS

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Vendor</th>
<th>Parameter</th>
<th>Typ.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>1 μH, 20%, 4.0 A, 2016</td>
<td>Semco CIGT201610EH1R0M or Equivalent</td>
<td>L</td>
<td>1.0</td>
<td>μH</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DCR (series R)</td>
<td>33</td>
<td>mΩ</td>
</tr>
<tr>
<td>C_BAT, C_SYS</td>
<td>10 μF, 20%, 6.3 V, X5R, 0603</td>
<td>Murata: GRM188R60J106M</td>
<td>C</td>
<td>10</td>
<td>μF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TDK: C1608X5R0J106M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_MID</td>
<td>4.7 μF, 10%, 10 V, X5R, 0603</td>
<td>Murata: GRM188R61A475K</td>
<td>C (Note 1)</td>
<td>4.7</td>
<td>μF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TDK: C1608X5R1A475K</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_BUS</td>
<td>1.0 μF, 10%, 25 V, X5R, 0603</td>
<td>Murata GRM188R61E105K</td>
<td>C</td>
<td>1.0</td>
<td>μF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TDK: C1608X5R1E105M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_REF</td>
<td>1 μF, 10%, 6.3 V, X5R, 0402</td>
<td></td>
<td>C</td>
<td>1.0</td>
<td>μF</td>
</tr>
<tr>
<td>Q5 (optional)</td>
<td>PMOS, 12 V, 16 mΩ, MLP2x2</td>
<td>onsemi FDMA905P</td>
<td>R_DS(ON)</td>
<td>16</td>
<td>mΩ</td>
</tr>
</tbody>
</table>

1. 10 V rating is sufficient for $C_{MID}$ since PMID is protected from over-voltage surges on VBUS by Q3.
# Pin Configuration

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>SDA</td>
<td>I²C Interface Serial Data. This pin should not be left floating</td>
</tr>
<tr>
<td>B1</td>
<td>SCL</td>
<td>I²C Interface Serial Clock. This pin should not be left floating</td>
</tr>
<tr>
<td>C1</td>
<td>DIS</td>
<td>Disable. If this pin is held HIGH, Q1 and Q3 are turned off; creating a HIGH Z condition at VBUS and the PWM converter is disabled</td>
</tr>
<tr>
<td>D1</td>
<td>STAT</td>
<td>Status. Open–drain output indicating charge status. The IC pulls this pin LOW when charge is in progress and is also used to signal the host processor when a fault condition occurs</td>
</tr>
<tr>
<td>E1</td>
<td>POK_B</td>
<td>Power OK. Open–drain output that pulls LOW when VBUS is plugged in and the battery has risen above ( V_{LOWV} ). This signal is used to signal the host processor that it can begin to draw significant current</td>
</tr>
<tr>
<td>A2 – D2</td>
<td>PGND</td>
<td>Power Ground. Power return for gate drive and power transistors. The connection from this pin to the bottom of C(_{MD}) should be as short as possible</td>
</tr>
<tr>
<td>E2</td>
<td>AGND</td>
<td>Analog Ground. All IC signals are referenced to this node</td>
</tr>
<tr>
<td>A3 – C3</td>
<td>SW</td>
<td>Switching Node. Connect to output inductor</td>
</tr>
<tr>
<td>D3 – E3</td>
<td>SYS</td>
<td>System Supply. Output voltage of the switching charger and input to the power path controller. Bypass SYS to PGND with a 10 ( \mu F ) capacitor</td>
</tr>
<tr>
<td>A4 – C4</td>
<td>PMID</td>
<td>Power Input Voltage. Power input to the charger regulator, bypass point for the input current sense. Bypass with a minimum of a 4.7 ( \mu F ), 6.3 V capacitor to PGND</td>
</tr>
<tr>
<td>D4 – E4</td>
<td>VBAT</td>
<td>Battery Voltage. Connect to the positive (+) terminal of the battery pack. Bypass with a 10 ( \mu F ) capacitor to PGND. VBAT is a power path connection</td>
</tr>
<tr>
<td>A5 – B5</td>
<td>VBUS</td>
<td>Charger Input Voltage and USB–OTG Output Voltage. Bypass with a 1 ( \mu F ) capacitor to PGND</td>
</tr>
<tr>
<td>C5</td>
<td>GATE</td>
<td>External MOSFET Gate. This pin controls the gate of an optional external P–channel MOSFET transistor used to augment the internal power–path FET (Q4) during battery discharge. The source of the P–channel MOSFET should be connected to SYS and the drain should be connected to VBAT</td>
</tr>
<tr>
<td>D5</td>
<td>NTC</td>
<td>Thermistor Input. The IC compares this node with taps on a resistor divider from REF to inhibit auto–charging when the battery temperature is outside of permitted fast–charge limits</td>
</tr>
<tr>
<td>E5</td>
<td>REF</td>
<td>Reference Voltage. REF is a 1.8 V regulated output</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{BUS}</td>
<td>Voltage on VBUS Pin</td>
<td>−0.3</td>
<td>28.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Pulsed, 100 ms Maximum Non-Repetitive</td>
<td>−1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_I</td>
<td>Voltage on PMID, SW, SYS, VBAT, STAT, DIS Pins</td>
<td>−0.3</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>V_O</td>
<td>Voltage on Other Pins</td>
<td>−0.3</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(Note 2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ΔV_{BUS}</td>
<td>Maximum V_{BUS} Slope Above 5.5 V when Boost or Charger Active</td>
<td>4</td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge Protection Level</td>
<td></td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Human Body Model per JESD22−A114</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Charged Device Model per JESD22−C101</td>
<td></td>
<td>500</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IEC 61000−4−2 System ESD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>USB Connector Pins (V_{BUS} to GND)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Air Gap</td>
<td>15</td>
<td></td>
<td>kV</td>
</tr>
<tr>
<td></td>
<td>Contact</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>T_J</td>
<td>Junction Temperature</td>
<td>−40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>T_{STG}</td>
<td>Storage Temperature</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>T_L</td>
<td>Lead Soldering Temperature, 10 Seconds</td>
<td></td>
<td>260</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Lesser of 6.5 V or V_I + 0.3 V.
3. Guaranteed if C_{BUS} ≥ 1 μF and C_{MID} ≥ 4.7 μF.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{BUS}</td>
<td>Supply Voltage</td>
<td>4</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>V_{BAT(MAX)}</td>
<td>Maximum Battery Voltage when Boost enabled</td>
<td>4.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ΔV_{BUS}</td>
<td>Negative V_{BUS} Slew Rate during VBUS Short Circuit, C_{MID} ≤ 4.7 μF, see VBUS Short While Charging</td>
<td>T_{A} ≤ 60°C</td>
<td>4</td>
<td>V/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_{A} ≥ 60°C</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>T_A</td>
<td>Ambient Temperature</td>
<td>−30</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>T_J</td>
<td>Junction Temperature (see Thermal Regulation and Shutdown)</td>
<td>−30</td>
<td>120</td>
<td>°C</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL PROPERTIES

Junction–to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T_{J(max)} at a given ambient temperature T_{A}.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typical</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>θ_{JA}</td>
<td>Junction–to–Ambient Thermal Resistance</td>
<td>50</td>
<td>°C/W</td>
</tr>
<tr>
<td>θ_{JB}</td>
<td>Junction–to–PCB Thermal Resistance</td>
<td>20</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
ELECTRICAL SPECIFICATIONS
Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for $T_J$ and $T_A$: $V_{BUS} = 5.0$ V; $HZ\_MODE = "0"; OPA\_MODE = "0"$ (Charge Mode); $SCL, SDA = 0$ or $1.8$ V; and typical values are for $T_J = 25^\circ$C. Min. and Max. values are not tested in production, but are determined by characterization.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{VBUS}$</td>
<td>VBUS Current</td>
<td>PWM Switching</td>
<td>$V_BAT &gt; V_{OREG}$</td>
<td>$V_BAT &gt; V_{LOWV}$</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V_{BUSLIM} = 500$ mA</td>
<td></td>
<td>6</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$0^\circ$C &lt; $T_J &lt; 85^\circ$C, $HZ_MODE = &quot;1&quot;$ or $DIS$ pin HIGH,</td>
<td></td>
<td></td>
<td>190</td>
<td>280</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_BAT &gt; V_{LOWV}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{BAT_HZ}$</td>
<td>Battery Discharge Current in High–Impedance Mode</td>
<td>$DIS$ pin HIGH, or $HZ_MODE = &quot;1&quot;$, $V_BAT = 4.35$ V</td>
<td>&lt;1.25</td>
<td>10.00</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>$I_{BUS_HZ}$</td>
<td>Battery Leakage Current to $V_{BUS}$ in High–Impedance Mode</td>
<td>$DIS$ pin HIGH or $HZ_MODE = &quot;1&quot;$, $V_BAT = 4.35$ V, $V_{BUS}$ Shorted to Ground</td>
<td>-5.0</td>
<td>-0.2</td>
<td>$\mu$A</td>
<td></td>
</tr>
</tbody>
</table>

CHARGER VOLTAGE REGULATION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OREG}$</td>
<td>Charge Voltage Range</td>
<td></td>
<td>3.51</td>
<td>4.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Charge Voltage Accuracy</td>
<td>$T_A = 25^\circ$C, $V_{OREG} = 4.35$ V</td>
<td>-0.5</td>
<td>+0.5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_J = 0$ to $125^\circ$C</td>
<td>-1</td>
<td>+1</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

CHARGING CURRENT REGULATION (FAST CHARGE)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OCHRG}$</td>
<td>Output Charge Current Range</td>
<td>$IO_LEVEL = &quot;0&quot;$</td>
<td>550</td>
<td>1550</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$IO_LEVEL = &quot;1&quot;$ (default)</td>
<td>165</td>
<td>200</td>
<td>230</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Charge Current Accuracy</td>
<td>$IO_LEVEL = &quot;0&quot;$</td>
<td>-5</td>
<td>+5</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

WEAK BATTERY DETECTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{LOWV}$</td>
<td>Weak Battery Threshold Range</td>
<td></td>
<td>3.4</td>
<td>3.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Weak Battery Threshold Accuracy</td>
<td></td>
<td>-5</td>
<td>+5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Weak Battery Deglitch Time</td>
<td></td>
<td>32</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PWM CHARGING THRESHOLD

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BATMIN}$</td>
<td>Rising PWM Charging Threshold</td>
<td></td>
<td>3.1</td>
<td>3.2</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BATFALL}$</td>
<td>Falling PWM Charging Threshold</td>
<td></td>
<td>3.0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

LOGIC LEVELS: DIS, SDA, SCL

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>High–Level Input Voltage</td>
<td></td>
<td>1.05</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low–Level Input Voltage</td>
<td></td>
<td></td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>Input Bias Current</td>
<td>Input Tied to GND or $V_{BUS}$</td>
<td>0.01</td>
<td>1.00</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>$R_{PD}$</td>
<td>DIS Pull–Down Resistance</td>
<td>$V_{DIS} = 0.4$ V</td>
<td></td>
<td>300</td>
<td>k$\Omega$</td>
<td></td>
</tr>
</tbody>
</table>

CHARGE TERMINATION DETECTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{TERM}$</td>
<td>Termination Current Range</td>
<td>$I_{TERM}$ Setting ≤ 100 mA</td>
<td>50</td>
<td>400</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{TERM}$ Setting ≥ 200 mA</td>
<td>-5</td>
<td>+5</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Termination Current Deglitch Time</td>
<td>(Note 4)</td>
<td>32</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
ELECTRICAL SPECIFICATIONS (continued)
Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for $T_J$ and $T_A$: $V_{BUS} = 5.0$ V; $HZ\_MODE = "0"$; $OPA\_MODE = "0"$ (Charge Mode); $SCL, SDA = 0$ or $1.8$ V; and typical values are for $T_J = 25$°C. Min. and Max. values are not tested in production, but are determined by characterization.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{PP}$</td>
<td>Power Path Maximum Charge Current</td>
<td>$IO_LEVEL = &quot;1&quot;$ (default)</td>
<td>165</td>
<td>200</td>
<td>235</td>
<td>mA</td>
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<tr>
<td></td>
<td></td>
<td>$IO_LEVEL = &quot;0&quot;, IBUSLIM \leq &quot;01&quot;$</td>
<td>165</td>
<td>200</td>
<td>235</td>
<td>mA</td>
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<tr>
<td></td>
<td></td>
<td>$IO_LEVEL = &quot;0&quot;, IBUSLIM &gt;&quot;01&quot;, IO_CHARGE \leq &quot;02&quot;$</td>
<td>375</td>
<td>450</td>
<td>520</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$IO_LEVEL = &quot;0&quot;, IBUSLIM &gt;&quot;01&quot;, IO_CHARGE &gt;&quot;02&quot;$</td>
<td>610</td>
<td>730</td>
<td>840</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{THSYS}$</td>
<td>$V_{SYS}$ Threshold for Q4 and Gate Transition While Charging</td>
<td>$(SYS−VBAT)$ Falling</td>
<td>-6</td>
<td>-5</td>
<td>-3</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(SYS−VBAT)$ Rising</td>
<td>-1</td>
<td>1</td>
<td>2</td>
<td>mV</td>
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**POWER PATH (Q4) CONTROL (PRECHARGE)**

<table>
<thead>
<tr>
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<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BAT}(PTM)$</td>
<td>Production Test Output Voltage</td>
<td>$1 \text{ mA} &lt; I_{BAT} &lt; 2 \text{ A}, V_{BUS} = 5.5 \text{ V}$</td>
<td>4.116</td>
<td>4.200</td>
<td>4.284</td>
<td>V</td>
</tr>
<tr>
<td>$I_{BAT}(PTM)$</td>
<td>Production Test Output Current</td>
<td>20% Duty with Max. Period 10 ms</td>
<td>2.3</td>
<td></td>
<td></td>
<td>A</td>
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**PRODUCTION TEST MODE**

<table>
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<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$T1$</td>
<td>$T_1$ (0°C) Temperature Threshold</td>
<td></td>
<td>71.9</td>
<td>73.9</td>
<td>75.9</td>
<td>% of $V_{REF}$</td>
</tr>
<tr>
<td>$T2$</td>
<td>$T_2$ (10°C) Temperature Threshold</td>
<td></td>
<td>62.6</td>
<td>64.6</td>
<td>66.6</td>
<td>% of $V_{REF}$</td>
</tr>
<tr>
<td>$T3$</td>
<td>$T_3$ (45°C) Temperature Threshold</td>
<td></td>
<td>31.9</td>
<td>32.9</td>
<td>34.9</td>
<td>% of $V_{REF}$</td>
</tr>
<tr>
<td>$T4$</td>
<td>$T_4$ (60°C) Temperature Threshold</td>
<td></td>
<td>21.3</td>
<td>23.3</td>
<td>25.3</td>
<td>% of $V_{REF}$</td>
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**BATTERY TEMPERATURE MONITOR (NTC)**

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{BUSLIM}$</td>
<td>Charger Input Current Limit Threshold</td>
<td>$IBUSLIM = &quot;00&quot;$</td>
<td>450</td>
<td>475</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$IBUSLIM = &quot;01&quot;$</td>
<td>760</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$IBUSLIM = &quot;10&quot;$</td>
<td>972</td>
<td>1080</td>
<td>1188</td>
<td>mA</td>
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**INPUT POWER SOURCE DETECTION**

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<th>Parameter</th>
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<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN(MIN)_1}$</td>
<td>VBUS Input Voltage Rising</td>
<td>To Initiate and Pass VBUS Validation</td>
<td>4.35</td>
<td>4.45</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN(MIN)_2}$</td>
<td>Minimum VBUS during Charge</td>
<td>During Charging</td>
<td>3.71</td>
<td>3.94</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{VBUS_VALID}$</td>
<td>VBUS Validation Time</td>
<td></td>
<td>32</td>
<td></td>
<td></td>
<td>ms</td>
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**VBUS CONTROL LOOP**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BUSLIM}$</td>
<td>VBUS Loop Setpoint Accuracy</td>
<td></td>
<td>-3</td>
<td></td>
<td>+3</td>
<td>%</td>
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**INPUT CURRENT LIMIT**

<table>
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<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$V_{REF}$</td>
<td>Bias Regulator Voltage</td>
<td>Charge Mode</td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Short-Circuit Current Limit</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>mA</td>
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**VREF BIAS GENERATOR**

<table>
<thead>
<tr>
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<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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<tbody>
<tr>
<td>$V_{RCH}$</td>
<td>Recharge Threshold</td>
<td>$V_{BAT} Below V_{OREG}$</td>
<td>100</td>
<td>120</td>
<td>150</td>
<td>mV</td>
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<tr>
<td></td>
<td>Deglitch Time</td>
<td>$V_{BAT}$ Falling Below $V_{RCH}$ Threshold</td>
<td>130</td>
<td></td>
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<td>ms</td>
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**BATTERY RECHARGE THRESHOLD**

<table>
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<tr>
<th>Symbol</th>
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<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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<tbody>
<tr>
<td>$I_{(OL)}$</td>
<td>Output Low</td>
<td>$I_{SINK} = 10$ mA</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>$I_{(OH)}$</td>
<td>Output High Leakage Current</td>
<td>$V_{OUT_OUTPUT} = 5$ V</td>
<td>1</td>
<td></td>
<td></td>
<td>μA</td>
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ELECTRICAL SPECIFICATIONS (continued)
Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A: V_BUS = 5.0 V; HZ_MODE = "0"; OPA_MODE = "0" (Charge Mode); SCL, SDA = 0 or 1.8 V; and typical values are for T_J = 25 °C. Min. and Max. values are not tested in production, but are determined by characterization.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
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<th>Max.</th>
<th>Unit</th>
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<td><strong>BATTERY DETECTION</strong></td>
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<tr>
<td>IDetect</td>
<td>Battery Detection Current before Charge Done (Sink Current) (Note 5)</td>
<td>Begins after Termination Detected and ( V_{BAT} \leq V_{OREG} - V_{RCH} )</td>
<td>–1.9</td>
<td>mA</td>
<td></td>
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<tr>
<td>tDETECT</td>
<td>Battery Detection Time</td>
<td></td>
<td>262</td>
<td>ms</td>
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<td><strong>SLEEP COMPARATOR</strong></td>
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<tr>
<td>VSLP</td>
<td>Sleep–Mode Entry Threshold, ( V_{BUS} - V_{BAT} )</td>
<td>( VIN(MIN) \leq V_{BAT} \leq V_{OREG}, V_{BUS} ) Falling</td>
<td>0</td>
<td>V</td>
<td></td>
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<tr>
<td><strong>POWER SWITCHES (see Figure 2)</strong></td>
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<tr>
<td>RDS(ON)</td>
<td>Q3 On Resistance (VBUS to PMID)</td>
<td>( I_{BUSLIM} = 500 ) mA</td>
<td>180</td>
<td>340</td>
<td>mΩ</td>
<td></td>
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<tr>
<td></td>
<td>Q1 On Resistance (PMID to SW)</td>
<td></td>
<td>130</td>
<td>225</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Q2 On Resistance (SW to GND)</td>
<td></td>
<td>150</td>
<td>225</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Q4 On Resistance (SYS to VBAT)</td>
<td>( V_{BAT} = 4.35 ) V</td>
<td>70</td>
<td>100</td>
<td>mΩ</td>
<td></td>
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<tr>
<td>ISYNC</td>
<td>Synchronous to Non–Synchronous Current Cut–Off Threshold (Note 6)</td>
<td>Low–Side MOSFET (Q2) Cycle–by–Cycle Current Limit</td>
<td>180</td>
<td>mA</td>
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<td><strong>CHARGER PWM MODULATOR</strong></td>
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<td>ISW</td>
<td>Oscillator Frequency</td>
<td></td>
<td>2.7</td>
<td>3.0</td>
<td>3.3</td>
<td>MHz</td>
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<tr>
<td>DMAX</td>
<td>Maximum Duty Cycle</td>
<td></td>
<td></td>
<td>100</td>
<td>%</td>
<td></td>
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<tr>
<td>DMIN</td>
<td>Minimum Duty Cycle</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
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<td><strong>BOOST MODE OPERATION (OPA_MODE=1)</strong></td>
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<tr>
<td>VBOOST</td>
<td>Boost Output Voltage at VBUS</td>
<td>2.5 V &lt; ( V_{BAT} &lt; 4.5 ) V, ( I_{LOAD} ) from 0 to 200 mA</td>
<td>4.80</td>
<td>5.07</td>
<td>5.20</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.0 V &lt; ( V_{BAT} &lt; 4.5 ) V, ( I_{LOAD} ) from 0 to 500 mA</td>
<td>4.77</td>
<td>5.07</td>
<td>5.20</td>
<td>V</td>
</tr>
<tr>
<td>IBAT(BOOST)</td>
<td>Boost Mode Quiescent Current</td>
<td>PFM Mode, ( V_{BAT} = 3.6 ) V, ( I_{LOAD} = 0 ) A</td>
<td>250</td>
<td>350</td>
<td>μA</td>
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<tr>
<td>ILIMPK(BST)</td>
<td>Q2 Peak Current Limit</td>
<td></td>
<td>1550</td>
<td>1800</td>
<td>2100</td>
<td>mA</td>
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<tr>
<td>UVLOBST</td>
<td>Minimum Battery Voltage for Boost Operation</td>
<td>While Boost Active</td>
<td>2.32</td>
<td>V</td>
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<td></td>
<td>To Start Boost Regulator</td>
<td>2.48</td>
<td>2.70</td>
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<td><strong>VBUS LOAD RESISTANCE</strong></td>
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<td>RVBUS</td>
<td>VBUS to PGND Resistance</td>
<td>Normal Operation</td>
<td>500</td>
<td>kΩ</td>
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<td></td>
<td>VBUS Validation</td>
<td>100</td>
<td>Ω</td>
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<td><strong>PROTECTION AND TIMERS</strong></td>
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<td>VBUSOVP</td>
<td>VBUS Over–Voltage Shutdown</td>
<td>VBUS Rising</td>
<td>6.09</td>
<td>6.29</td>
<td>6.49</td>
<td>V</td>
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<tr>
<td></td>
<td></td>
<td>Hysteresis</td>
<td>VBUS Falling</td>
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<td>mV</td>
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<td>ILIMPK(CHG)</td>
<td>Q1 Cycle–by–Cycle Peak Current Limit</td>
<td>Charge Mode</td>
<td>3</td>
<td>A</td>
<td></td>
<td></td>
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<tr>
<td>VSHORT</td>
<td>Battery Short–Circuit Threshold</td>
<td>( V_{BAT} ) Rising</td>
<td>1.95</td>
<td>2.00</td>
<td>2.07</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
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<td>ISHORT</td>
<td>Linear Charging Current</td>
<td>( V_{BAT} &lt; V_{SHORT} )</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
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<tr>
<td>TSHUTDWN</td>
<td>Thermal Shutdown Threshold (Note 4)</td>
<td>T_J Rising</td>
<td>145</td>
<td>°C</td>
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<tr>
<td></td>
<td></td>
<td>Hysteresis (Note 4)</td>
<td>T_J Falling</td>
<td>25</td>
<td>°C</td>
<td></td>
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<tr>
<td>TC5</td>
<td>Thermal Regulation Threshold (Note 4)</td>
<td>Charge Current Reduction Begins</td>
<td>120</td>
<td>°C</td>
<td></td>
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<tr>
<td>INT</td>
<td>Detection Interval</td>
<td></td>
<td>2</td>
<td>s</td>
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</tbody>
</table>
ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for $T_J$ and $T_A$: $V_{BUS} = 5.0 \text{ V}$; $HZ_{MODE} = \text{"0"}$; $OPA_{MODE} = \text{"0"}$ (Charge Mode); $SCL$, $SDA = 0$ or $1.8 \text{ V}$; and typical values are for $T_J = 25^\circ \text{C}$. Min. and Max. values are not tested in production, but are determined by characterization.

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$T_{32S}$</td>
<td>32–Second Timer (Note 7)</td>
<td>Charger Enabled</td>
<td>20.5</td>
<td>25.2</td>
<td>28.0</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Charger Disabled</td>
<td>18.0</td>
<td>25.2</td>
<td>34.0</td>
<td></td>
</tr>
<tr>
<td>$\Delta t_{LF}$</td>
<td>Low–Frequency Timer Accuracy</td>
<td>Charger Inactive</td>
<td>−23</td>
<td>27</td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by design; not tested in production.
5. Negative current is current flowing from the battery to ground (discharging the battery).
6. Q2 always turns on for 60 ns, then turns off if current is below $I_{SYNC}$.
7. This tolerance (%) applies to all timers on the IC, including soft–start and deglitching timers.

**I\textsuperscript{2}C TIMING SPECIFICATIONS** Guaranteed by design.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SCL}$</td>
<td>SCL Clock Frequency</td>
<td>Standard Mode</td>
<td>100</td>
<td></td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>400</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
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<tr>
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<td></td>
<td>High–Speed Mode, $C_B \leq 100 \text{ pF}$</td>
<td>3400</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, $C_B \leq 400 \text{ pF}$</td>
<td>1700</td>
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<td></td>
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<tr>
<td>$t_{BUF}$</td>
<td>Bus–free Time between STOP and START Conditions</td>
<td>Standard Mode</td>
<td>4.7</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
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<td></td>
<td></td>
<td>Fast Mode</td>
<td>1.3</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>0.5</td>
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</tr>
<tr>
<td>$t_{HD;STA}$</td>
<td>START or Repeated START Hold Time</td>
<td>Standard Mode</td>
<td>4</td>
<td></td>
<td>s</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>600</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>260</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode</td>
<td>160</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{LOW}$</td>
<td>SCL LOW Period</td>
<td>Standard Mode</td>
<td>4.7</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>1.3</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>0.5</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, $C_B \leq 100 \text{ pF}$</td>
<td>160</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, $C_B &lt; 400 \text{ pF}$</td>
<td>320</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{HIGH}$</td>
<td>SCL HIGH Period</td>
<td>Standard Mode</td>
<td>4</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>600</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>260</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, $C_B &lt; 100 \text{ pF}$</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, $C_B &lt; 400 \text{ pF}$</td>
<td>120</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{SU;STA}$</td>
<td>Repeated START Setup Time</td>
<td>Standard Mode</td>
<td>4.7</td>
<td></td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>600</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Conditions</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>--------------------------------</td>
<td>-------------------------------------------------</td>
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<td>------</td>
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<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{SU;DAT}</td>
<td>Data Setup Time</td>
<td>Standard Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td></td>
<td></td>
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<td>Fast Mode Plus</td>
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<tr>
<td></td>
<td></td>
<td>High-Speed Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_{HD;DAT}</td>
<td>Data Hold Time</td>
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<td>μs</td>
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<tr>
<td></td>
<td></td>
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<td>0</td>
<td>900</td>
<td></td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>0</td>
<td>450</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 100 pF</td>
<td>0</td>
<td>70</td>
<td></td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 400 pF</td>
<td>0</td>
<td>150</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{RCL}</td>
<td>SCL Rise Time</td>
<td>Standard Mode</td>
<td>20+0.1C_B</td>
<td>1000</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>20+0.1C_B</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>20+0.1C_B</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 100 pF</td>
<td>10</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 400 pF</td>
<td>20</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{FCL}</td>
<td>SCL Fall Time</td>
<td>Standard Mode</td>
<td>20+0.1C_B</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>20+0.1C_B</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>20+0.1C_B</td>
<td>120</td>
<td></td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 100 pF</td>
<td>10</td>
<td>40</td>
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<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 400 pF</td>
<td>20</td>
<td>80</td>
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<td>ns</td>
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<tr>
<td>t_{RCL1}</td>
<td>Rise Time of SCL after a Repeated START Condition and after ACK Bit</td>
<td>High-Speed Mode, C_B &lt; 100 pF</td>
<td>10</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 400 pF</td>
<td>20</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{RDA}</td>
<td>SDA Rise Time</td>
<td>Standard Mode</td>
<td>20+0.1C_B</td>
<td>1000</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>20+0.1C_B</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>20+0.1C_B</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 100 pF</td>
<td>10</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 400 pF</td>
<td>20</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{FDA}</td>
<td>SDA Fall Time</td>
<td>Standard Mode</td>
<td>20+0.1C_B</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>20+0.1C_B</td>
<td>300</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>20+0.1C_B</td>
<td>120</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 100 pF</td>
<td>10</td>
<td>80</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, C_B &lt; 400 pF</td>
<td>20</td>
<td>160</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{SU;STO}</td>
<td>Stop Condition Setup Time</td>
<td>Standard Mode</td>
<td>4</td>
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<td>μs</td>
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<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>600</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode Plus</td>
<td>120</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode</td>
<td>160</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>C_B</td>
<td>Capactive Load for SDA and SCL</td>
<td></td>
<td></td>
<td></td>
<td>400</td>
<td>pF</td>
</tr>
</tbody>
</table>
Figure 5. \(I^2C\) Interface Timing for Fast and Slow Modes

- \(SCL\) and \(SDA\)
- \(t_{F}\); \(t_{HD}; STA\)
- \(t_{LOW}\)
- \(t_{R}\); \(t_{HD}; DAT\)
- \(t_{HIGH}\)
- \(T_{SU}; DAT\)
- \(t_{HD}; STO\)
- \(t_{BUF}\)

Note A: First rising edge of \(SCL_{H}\) after Repeated Start and after each ACK bit.

Figure 6. \(I^2C\) Interface Timing for High-Speed Mode

- \(SDA_{H}\) and \(SCL_{H}\)
- \(t_{FDA}\)
- \(t_{RCL}\)
- \(t_{FCL}\)
- \(t_{RDA}\)
- \(t_{SU; DAT}\)

\[\begin{align*}
\square & = \text{MCS Current Source Pull-up} \\
\frown & = \text{R\textsubscript{p} Resistor Pull-up}
\end{align*}\]
CHARGE MODE TYPICAL CHARACTERISTICS

Unless otherwise specified, circuit of Figure 1, \( V_{\text{OREG}} = 4.35 \text{ V} \), \( I_{\text{OCHARGE}} = 950 \text{ mA} \), \( I_{\text{O_LEVEL}} = 0 \), \( V_{\text{BUS}} = 5.0 \text{ V} \), and \( T_{\text{A}} = 25^\circ \text{C} \).

**Figure 7.** Battery Charge Current vs. \( V_{\text{BUS}} \) with \( I_{\text{BUSLIM}} = 500 \text{ mA} \)

**Figure 8.** Battery Charge Current vs. \( V_{\text{BUS}} \) with \( I_{\text{BUSLIM}} = 1100 \text{ mA} \), \( I_{\text{OCHRG}} = 1550 \text{ mA} \)

**Figure 9.** Efficiency vs. \( V_{\text{BUS}} \), \( I_{\text{BUSLIM}} = 500 \text{ mA} \), \( I_{\text{SYS}} = 0 \)

**Figure 10.** Efficiency vs. Charging Current, \( I_{\text{BUSLIM}} = \text{No Limit} \)

**Figure 11.** HZ Mode \( V_{\text{BUS}} \) Current vs. Temperature, \( 3.7 \text{ V}_{\text{BAT}} \)

**Figure 12.** \( V_{\text{REF}} \) vs. Load Current, Over Temperature
CHARGE MODE TYPICAL CHARACTERISTICS

Unless otherwise specified circuit of Figure 1, \( V_{OREG} = 4.34 \) V, \( I_{O,\text{CHARGE}} = 950 \) mA, \( IO_{\text{LEVEL}} = 0 \), \( V_{BUS} = 5.0 \) V, and \( T_A = 25^\circ \)C.

Figure 13. Charger Startup at \( V_{BUS} \) Plug-In, 500 mA \( I_{BUSLIM} \), 3.1 V \( \text{VBAT} \), 50 \( \Omega \) SYS Load, \( CE\# = 0 \), \( IO_{\text{LEVEL}} = 1 \)

Figure 14. Charger Startup at \( V_{BUS} \) Plug-In, 1100 mA \( I_{BUSLIM} \), 3.6 V \( \text{VBAT} \), 700 mA SYS Load, \( CE\# = 0 \), \( IO_{\text{LEVEL}} = 0 \)

Figure 15. Charger Startup at \( V_{BUS} \) Plug-In Using 300 mA Current Limited Source, 500 mA \( I_{BUSLIM} \), 3.1 V \( \text{VBAT} \), 200 mA SYS Load, \( CE\# = 0 \), \( IO_{\text{LEVEL}} = 0 \)

Figure 16. Charger Startup with HZ Bit Reset, 500 mA \( I_{BUSLIM} \), 950 mA \( I_{\text{CHARGE}} \), 50 \( \Omega \) SYS Load, \( CE\# = 0 \)
CHARGE MODE TYPICAL CHARACTERISTICS

Unless otherwise specified circuit of Figure 1, $V_{OREG} = 4.34\, V$, $I_{O\, CHARGE} = 950\, mA$, $IO\_LEVEL = 0$, $V_{BUS} = 5.0\, V$, and $T_A = 25\, ^\circ C$

Figure 17. Charger Enable (CE# = 1 to 0) with $V_{BUS}$ Applied, $I_{BUSLIM} = 500\, mA$, 200 mA SYS Load, IO\_LEVEL = 0

Figure 18. No Battery at $V_{BUS}$ Power-Up, 100 Ω SYS Load, 1 kΩ $V_{BAT}$ Load

Figure 19. Battery Removal / Insertion while Charging, TE = 0, 3.9 $V_{BAT}$, $I_{CHRG} = 950\, mA$, $I_{BUSLIM} = $ No Limit, 50 Ω SYS Load

Figure 20. Battery Removal / Insertion when Charging, TE = 1, 3.9 $V_{BAT}$, $I_{BUSLIM} = $ No Limit, 50 Ω SYS Load
GSM TYPICAL CHARACTERISTICS
A 2.0 A GSM pulse applied at $V_{BAT}$ with 5 ms rise/fall time. Simultaneous to GSM pulse, 50Ω additional load applied at SYS

Figure 21. 2.0 A GSM Pulse Response, $I_{BUSLIM} = 500$ mA Control, $I_{CHRG} = 950$ mA, 3.7 $V_{BAT}$, OREG = 4.35 V

Figure 22. 2.0 A GSM Pulse Response, $I_{BUSLIM} = 500$ mA, $I_{CHRG} = 950$ mA, 3.7 $V_{BAT}$, OREG = 4.35 V, 200 mA Source Current Limit
BOOST MODE TYPICAL CHARACTERISTICS

Unless otherwise specified, using circuit of Figure 1 with optional external PMOS, $V_{BAT} = 3.6 \, V$, $T_A = 25^\circ C$.

- Figure 23. Efficiency vs. $I_{BUS}$ over $V_{BAT}$
- Figure 24. Efficiency vs. $I_{BUS}$ Over–Temperature, $3.6 \, V_{BAT}$
- Figure 25. Regulation vs. $I_{BUS}$ over $V_{BAT}$
- Figure 26. Output Ripple vs. $I_{BUS}$ over $V_{BAT}$
- Figure 27. Quiescent Current ($I_Q$) vs. $V_{BAT}$ Over–Temperature
- Figure 28. Battery Discharge Current vs. $V_{BAT}$, Hz/ Sleep Mode
BOOST MODE TYPICAL CHARACTERISTICS

Unless otherwise specified, using circuit of Figure 1 with optional external PMOS, $V_{BAT} = 3.6 \text{ V}$, $T_A = 25^\circ \text{C}$.

Figure 29. OTG Startup, 50 $\Omega$ Load, 3.6 $V_{BAT}$
External / Additional 10 $\mu$F on $V_{BUS}$

Figure 30. OTG $V_{BUS}$ Overload Response

Figure 31. Load Transient, 20–200–20 mA $I_{BUS}$,
$\tau_{\text{RISE/FALL}} = 100 \text{ ns}$

Figure 32. Line Transient, 50 $\Omega$ Load,
3.9–3.3–3.9 $V_{BAT}$, $\tau_{\text{RISE/FALL}} = 10 \mu\text{s}$
CIRCUIT DESCRIPTION / OVERVIEW

When charging batteries with a current−limited input source, such as USB, a switching charger’s high efficiency over a wide range of output voltages minimizes charging time.

FAN54063 combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5 V to USB On−The−Go (OTG) peripherals. The FAN54063 employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The FAN54063 has four operating modes:
1. Charge Mode:
   Charges a single−cell Li−ion or Li−polymer battery
2. Boost Mode:
   Provides 5 V power to USB−OTG with an integrated synchronous rectification boost regulator, using the battery as input
3. High−Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery
4. Production Test Mode:
   This mode provides 4.2 V output on VBAT and supplies a load current of up to 2.3 A

CHARGE MODE AND REGISTERS

Charge Mode
In Charge Mode, FAN54063 employs six regulation loops:
1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I2C interface
2. Charging Current: Limits the maximum charging current. This current is sensed using an internal sense MOSFET
3. VBUS Voltage: This loop is designed to prevent the input supply from being dragged below VBUSLIM (typically 4.5 V) when the input power source is current limited. An example of this would be a travel charger. This loop cuts back the current when VBUS approaches VBUSLIM, allowing the input source to run in current limit
4. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery’s internal impedance works in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the current through Q4 drops below the ITERM threshold
5. Pre−charge: When VBAT is below VBATMIN, Q4 operates as a linear current source and modulates its current to ensure that the voltage on SYS stays above 3.4 V
6. Temperature: If the IC’s junction temperature reaches 120°C, charge current is reduced until the IC’s temperature is below 120°C

PWM Controller in Charge Mode
The IC uses a current−mode PWM controller to regulate the output voltage and battery charge currents. The synchronous rectifier (Q2) has a negative current limit that turns off Q2 at 180 mA to prevent current flow from the battery.

Battery Charging Curve
If the battery voltage is below VSHORT, a linear current source pre−charges the battery until VBAT reaches VSHORT. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

During the current regulation phase of charging, IBUSLIM or the programmed charging current limits the amount of current available to charge the battery and power the system.

During the voltage regulation phase of charging, assuming that VOREG is programmed to the cell’s fully charged “float” voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to VOREG declines.

The FAN54063 is designed to work with a current−limited input source at VBUS as shown below:
The following charging parameters can be programmed by the host through I2C:

### Table 3. PROGRAMABLE CHARGING PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage Regulation</td>
<td>VOREG</td>
<td>REG02[7:2]</td>
</tr>
<tr>
<td>Battery Charging Current Limit</td>
<td>IOCHARGE</td>
<td>REG04[6:3]</td>
</tr>
<tr>
<td>Input Current Limit</td>
<td>IBUSLIM</td>
<td>REG01[7:6]</td>
</tr>
<tr>
<td>Charge Termination Limit</td>
<td>ITERM</td>
<td>REG04[2:0]</td>
</tr>
<tr>
<td>Weak Battery Voltage</td>
<td>VLOWV</td>
<td>REG01[5:4]</td>
</tr>
</tbody>
</table>

**Output Voltage Regulation (VOREG)**

The charger output or “float” voltage can be programmed by the OREG (REG02[7:2]) bits from 3.51 V to 4.45 V in 20 mV increments. The default setting is 3.55 V. See OREG Register Bit Definitions.(Table 17)

**Battery Charging Current Limit (IOCHARGE)**

When the IO_LEVEL bit is set (default), the IOCHARGE bits are ignored and charge current is set to 200 mA. See IOCHARGE Register Bit Definitions.(Table 17)

**Input Current Limiting (IBUSLIM)**

To minimize charging time without overloading VBUS current limitations, the IC’s input current limit can be programmed by the IBUSLIM (REG01[7:6]) bits. See IBUSLIM Register Bit Definitions.(Table 17)

**Termination Limit (ITERM)**

Charge current termination can be enabled or disabled using the TE (REG01[3]) bit. By default TE = “0”, therefore, termination is disabled and charging does not terminate at the programmed ITERM level.

When TE = “1”, and VBAT reaches VOREG, the charging current is reduced, limited by the battery’s ESR and its internal cell voltage. When the charge current falls below ITERM; PWM charging stops; but the STAT pin remains LOW. The STAT pin then goes HIGH and the STAT bits change to CHARGE DONE (10), provided the battery and charger are still connected. If VBAT falls to VCH below VOREG, the Fast Charge cycle starts again.

Post-charging can be enabled to “top–off” the battery to a lower termination current threshold than ITERM. The PC_EN bit (REG07[3]) must be set to “1” before the battery charging current reaches ITERM. The lower termination current is set by the PC_IT (REG07[2:0]) bits. Post-charging begins after normal charging is ended (as described above) with the PC_ON (REG11[2]) monitor bit set to “1”.

During post-charging, the STAT pin is HIGH, indicating that the charge current is below the ITERM level. Once the current reaches the threshold for post-charging completion (set by the PC_IT bits), PWM charging stops and the PC_ON bit changes back to “0”. If the charging current goes above ITERM without first falling to PC_IT, the PC_ON bit can be reset by using any of these methods: VBAT moving below and above VBATMIN, a VBUS POR, or the CE# or HZ_MODE bit cycled. If VBAT falls to VCH below VOREG, the Fast Charge cycle starts again.

See ITERM Register Bit Definitions.(Table 17)

**Weak Battery Voltage (VLOWV)**

The FAN54063 monitors the level of the battery with respect to a programmable VLOWV (REG01<5:4>) threshold (default 3.7 V). VLOWV defines the voltage level of the battery at which the system is guaranteed to be fully operational when only powered by the battery.

The POK_B pin pulls LOW once VBAT reaches VLOWV, and remains LOW as long as the IC is in Fast Charge. The IC will remain in Fast Charge as long as VBAT > 3.0 V. See VLOWV Register Bit Definitions.(Table 17)

**VBUS Control loop (VBUSLIM)**

The IC includes a control loop that limits input current in case a current–limited source is supplying VBUS. The control increases the charging current until either:
- IBUSLIM or IOCHARGE limit is reached OR
- VBUS = VBUSLIM

If VBUS collapses to VBUSLIM, the VBUS loop reduces its current to keep VBUS = VBUSLIM. When the VBUS control loop is limiting the charge current, the VLIM bit (REG05[3]) is set.

See VBUSLIM Register Bit Definitions.(Table 17)
CHARGER OPERATION

VBUS Plug In and Safety Timer
At VBUS plug in, the TMR_RST (Reg00[7]) bit must be set within 2 seconds of VBUS rising above V(INMIN)1 or all registers, except for SAFETY (REG06), are set to their default values. This functionality occurs regardless of the state of the CE# and WD_DIS bit. If plug in occurs with the device in a HZ or Charge Done state and the TMR_RST bit is not set within 2 seconds of VBUS rising above V(INMIN)1, all register, except for SAFETY, will reset when the device enters PWM Charging or Recharge.

By default, the safety timers do not run in the FAN54063. A Watchdog (t32S) timer can be enabled by setting the WD_DIS register bit, (Reg13[1]) to “0”. When WD_DIS = “0”, charging is controlled by the host with the t32S timer running to ensure that the host is alive. Setting the TMR_RST bit resets the t32S timer. If the t32S timer times out; all registers, except SAFETY, are set to their default values (including WD_DIS and CE#), the FAULT bits are set to “110”, and STAT is pulsed.

VBUS POR / Non–Compliant Charger Rejection
256 ms after VBUS is connected, the IC pulses the STAT pin and sets the VBUS_CON bit. Before starting to supply current, the IC applies a 100 Ω load from VBUS to GND. VBUS must remain above V(INMIN)1 and below VBUSOVP for tVBUSVALID (32 ms) before the IC initiates charging or supplies power to SYS.

The VBUS validation sequence always occurs before significant current is drawn from VBUS (for example, after a VBUS OVP fault or a recharge initiation). tVBUSVALID ensures that unfiltered 50/60 Hz chargers and other non–compliant chargers are rejected.

USB–Friendly Boot Sequence
The FAN54063 does not automatically initiate charging at VBUS POR. Instead, prior to receiving host commands, the buck is enabled to provide power to SYS while Q4 and Q5 remain off until register bit CE# (REG01[2]) is set to “0” through the I2C interface, allowing charging through Q4.

Startup with No Battery
The FAN54063 has Battery Absent Behavior enabled. At VBUS POR with the battery absent, the PWM will run, providing 3.55 V to the system from the input source with current limited by the default IBUSLIM setting. This allows the host processor to awaken and establish host control. Once this occurs, the host’s low level software can program the CE# bit to “0” and a linear current source closes the battery protection switch. When VBAT voltage rises above VBATMIN and sufficient power is available, PWM charging begins and the battery is charged through the BATFET, Q4. The IO_LEVEL (REG05[5]) bit is set to “1” by default which limits charge current to 200 mA.

With CE# = “1” once VBAT rises above VSHORT, DBAT_B is set. With CE# = “0” once VBAT rises above VBATMIN, DBAT_B is set.

Power Path Operation
As long as VBAT < VBATMIN, Q4 operates as a linear current source, (Precharge) with its current (Ip) limited to 200 mA when IO_LEVEL (REG05[5]) is set to its default value of “1”. If IO_LEVEL is set to “0” and IBUSLIM > “01”, charge current is limited to 450 mA when IOCHARGE ≤ 750 mA, and 730 mA when IOCHARGE > 750 mA. Providing the input current is not limited by the IBUSLIM setting or the current available from the source, during precharge, the IC regulates SYS to 3.55 V and provides the Ipp limited current to the battery.

System power always has the highest priority when power from the buck is limited ensuring SYS does not fall below 3.4 V. This is managed by folding back the current to charge the battery until charge current is reduced to 0 A.

After VBAT reaches VBATMIN, Q4 fully enhances and is used as a current–sense element to limit current (IOCHARGE) per the I2C register settings. This is accomplished by limiting the PWM modulator’s current (Fast Charge). If SYS drops more than 5 mV (VTHSYS) below VBAT and CE# = “0”, Q4 is turned on and GATE is pulled LOW. If CE# = “1”, only GATE is forced LOW. Once SYS voltage becomes higher than VBAT, GATE returns HIGH and Q4, once again, serves as the current–sense element to limit IOCHARGE.

If the DIS pin is HIGH or HZ_MODE = “1” while VBAT > VLOWV, Q4 is enabled and GATE is forced LOW to prevent the system from crashing. Upon entering SLEEP Mode (VBUS < VBAT), Q4 is turned on and GATE is held LOW.

Optional External Power Path Provisions
Q4 has a typical on–resistance of 70mΩ, which is sufficient for most applications. However, if high system load currents are expected, it is possible to augment Q4 with a parallel external PMOS element, connected as shown by dotted lines in Figure 2. Use of the optional external PMOS reduces the series voltage drop associated with battery discharge during SLEEP mode or supplemental mode operation. For example, the addition of onsemi’s FDMA905P can support discharge currents above 10 A.
POK_B (see Table 4)

The POK_B pin and the POK_B (REG11[5]) bit are intended to provide feedback to the processor that the battery is strong enough to allow the system to fully function. Whenever the IC is operating in precharge, POK_B is HIGH. On exiting Precharge, POK_B remains HIGH until VBAT > VLOWV. REG01[5:4] sets the VLOWV threshold. POK_B pulls LOW once VBAT reaches VLOWV, and remains LOW as long as the IC is in Fast Charge and the IC will remain in Fast Charge as long as VBAT > 3.0 V. If the battery voltage falls below 3.0 V the IC enters Precharge. If WD_DIS = “0” and the t32S timer expires during charging, the POK_B pin will go HIGH.

The POK_B bit can be set via I2C to change the state of the pin to HIGH. This setting of the bit and pin can be used to signal the system into a low-power state, preventing excessive loading from the system while attempting to recharge a depleted battery.

The STAT pin pulses any time the POK_B pin and bit change states.

### Table 4. Q4, Q5, POK_B vs. OPERATING MODE

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>VBUS</th>
<th>VBAT</th>
<th>CE#</th>
<th>PWM</th>
<th>VSYS</th>
<th>Q4</th>
<th>Q5</th>
<th>GATE</th>
<th>POK_B</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VBUS DISCONNECTED</strong></td>
<td>Off</td>
<td>&lt; VBAT or &lt; VMIN(MIN)/2</td>
<td>&gt; VSHORT</td>
<td>X</td>
<td>OFF</td>
<td>≤ VBAT</td>
<td>ON</td>
<td>ON</td>
<td>LOW</td>
</tr>
<tr>
<td><strong>VBUS PLUG IN WITH BATTERY PROTECTION SWITCH OPEN</strong></td>
<td></td>
<td></td>
<td>PWM</td>
<td></td>
<td>VOREG</td>
<td>OFF</td>
<td>OFF</td>
<td>HIGH</td>
<td>HIGH</td>
</tr>
<tr>
<td>30 mA Linear Charging (Note 8)</td>
<td></td>
<td></td>
<td>Valid</td>
<td>ON</td>
<td>3.55</td>
<td>OFF</td>
<td>OFF</td>
<td>HIGH</td>
<td>HIGH</td>
</tr>
<tr>
<td><strong>CHARGE MODE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Precharge</td>
<td>Valid</td>
<td>&gt; VSHORT and &lt; VBATMIN</td>
<td>0</td>
<td>ON</td>
<td>3.55</td>
<td>Linear</td>
<td>OFF</td>
<td>HIGH</td>
<td>HIGH</td>
</tr>
<tr>
<td>Precharge: lSYS + lPP &gt; lPWM, lBAT &lt; lPP</td>
<td>Valid</td>
<td>&lt; VBATMIN</td>
<td>0</td>
<td>ON</td>
<td>&lt; 3.55</td>
<td>Linear</td>
<td>OFF</td>
<td>HIGH</td>
<td>HIGH</td>
</tr>
<tr>
<td>Fast Charge</td>
<td>Valid</td>
<td>&gt; VBATMIN and &lt; VLOWV</td>
<td>0</td>
<td>ON</td>
<td>&gt; VBAT</td>
<td>ON</td>
<td>OFF</td>
<td>HIGH</td>
<td>HIGH</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&gt; VLOWV</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LOW</td>
</tr>
<tr>
<td><strong>BATTERY VOLTAGE FALLING FROM FAST CHARGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Precharge</td>
<td>Valid</td>
<td>VBATFALL</td>
<td>0</td>
<td>ON</td>
<td>3.55</td>
<td>ON</td>
<td>OFF</td>
<td>HIGH</td>
<td>HIGH</td>
</tr>
<tr>
<td><strong>BATTERY SUPPLEMENTING SYS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supplemental Mode : lSYS &gt; lPWM</td>
<td>Valid</td>
<td>&gt; VBATMIN and &gt; VSYS + VTHSYS</td>
<td>X</td>
<td>ON</td>
<td>&lt; VBAT</td>
<td>X</td>
<td>ON</td>
<td>LOW</td>
<td>X</td>
</tr>
</tbody>
</table>

8. When VBAT is open, VBAT can float to VSYS, and POK_B = HIGH when VBAT < VLOWV and POK_B = LOW when VBAT > VLOWV. Battery’s presence or not (VBAT open) can be monitored by reading NOBAT bit (REG11[3]).

9. 30 mA Linear Charging operating mode assumes the host has programmed CE# = “0” during PWM Operating Mode.
Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 5. STAT Pin Function

<table>
<thead>
<tr>
<th>EN_STAT</th>
<th>Charge State</th>
<th>STAT Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>OPEN</td>
</tr>
<tr>
<td>X</td>
<td>Normal Conditions</td>
<td>OPEN</td>
</tr>
<tr>
<td>1</td>
<td>Charging</td>
<td>LOW</td>
</tr>
<tr>
<td>X</td>
<td>Fault (Charging or Boost)</td>
<td>128 μs Pulse, then OPEN</td>
</tr>
</tbody>
</table>

The FAULT bits (REG00[2:0]) indicate the type of fault in Charge Mode.

Monitor Registers (REG10, REG11)

Additional status monitoring bits enable the host processor to have more visibility into the status of the IC. The monitor bits are real-time status indicators and are not internally debounced or otherwise time qualified.

The state of the MONITOR register bits listed in High-Impedance Mode is valid only when VBUS is valid.

Table 6. DIS PIN, HZ_MODE AND WD_DIS BIT OPERATION

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Functionality</th>
</tr>
</thead>
<tbody>
<tr>
<td>WD_DIS = 1 (default) and VBAT &gt; VLOW</td>
<td>Setting either the HZ_MODE bit through I²C or the DIS pin HIGH will disable the charger and put the IC into High-Impedance Mode. Resetting the HZ_MODE bit or the DIS pin to LOW will allow charging to resume.</td>
</tr>
<tr>
<td>WD_DIS = 0 and VBAT &gt; VLOW</td>
<td>Setting either the HZ_MODE bit through I²C or the DIS pin HIGH will stop the t32s timer from advancing (does not reset it), disable the charger, and put the IC into High-Impedance Mode. Resetting the HZ_MODE bit or the DIS pin LOW allows charging to resume. The t32s timer resuming counting down the remainder of time from where it was suspended, at HZ mode entry.</td>
</tr>
</tbody>
</table>
Note: At VBUS plug in, the TMR_RST (REG0[7]) bit must be set within 2 seconds of \( V_{BUS} \) rising above \( V_{(INMIN)} \) or all registers, except for SAFETY (REG06), are set to their default values.

Note: At VBUS plug in, the TMR_RST (REG0[7]) bit must be set within 2 seconds of \( V_{BUS} \) rising above \( V_{(INMIN)} \) or all registers, except for SAFETY (REG06), are set to their default values.

Note: Reset Charge Parameters is a condition that results in the \( O \) REG, IOCHARGE, IBUSLIM, ITERM, VLOWV, and the Safety register bits resetting. It does not reset the IO _LEVEL, EOC, and TE register bits.

Figure 35. Charge State Flow Chart
NON-CHARGING STATES

Sleep Mode
When VBUS falls below VBAT + VSLP and VBUS is above VIN(MIN), the IC enters Sleep Mode to prevent the battery from draining into VBUS. During Sleep Mode, reverse current is disabled by body switching Q1.

Idle State
The Idle State is related to the condition of the battery. During Idle mode the Switch Mode Power Supply (SMPS) is operating, but the battery is not being charged for one or more of the following conditions: the Safety Timer expires (CE# reset to 1), charging is complete, or the BATFET is disabled by the Charge Enable bit, CE# = “1”.

The PWM Buck continues to supply power to the system, but the Battery is no longer being charged and the BATFET is disabled.

Table 7. BATTERY TEMPERATURE THRESHOLDS
For use with 10 kΩ NTC, b = 3380, and RREF = 10 kΩ.

<table>
<thead>
<tr>
<th>Threshold</th>
<th>Temperature</th>
<th>% of VREF</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>0°C</td>
<td>73.9</td>
</tr>
<tr>
<td>T2</td>
<td>10°C</td>
<td>64.6</td>
</tr>
<tr>
<td>T3</td>
<td>45°C</td>
<td>32.9</td>
</tr>
<tr>
<td>T4</td>
<td>60°C</td>
<td>23.3</td>
</tr>
</tbody>
</table>

Table 8. CHARGE PARAMETERS VS. TBAT
For use with 10 kΩ NTC, b = 3380, and RREF = 10 kΩ.

<table>
<thead>
<tr>
<th>TBAT (°C)</th>
<th>ICHARGE</th>
<th>VFLOAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Below T1</td>
<td>Charging to VBAT Disabled</td>
<td></td>
</tr>
<tr>
<td>Between T1 and T2</td>
<td>ICHARGE / 2 (Note 10)</td>
<td>4.0 V</td>
</tr>
<tr>
<td>Between T2 and T3</td>
<td>ICHARGE</td>
<td>VOREG</td>
</tr>
<tr>
<td>Between T3 and T4</td>
<td>ICHARGE / 2 (Note 10)</td>
<td>4.0 V</td>
</tr>
<tr>
<td>Above T4</td>
<td>Charging to VBAT Disabled</td>
<td></td>
</tr>
</tbody>
</table>

10. If ICHARGE is programmed to less than 650 mA, the charge current is limited to 340 mA.

Thermistors with other β values can be used, with some shift in the corresponding temperature threshold, as shown in Table 9.

Table 9. THERMISTOR TEMPERATURE THRESHOLDS
RREF = RTHRM at 25°C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RTHRM(25°C)</th>
<th>Various Thermistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>β</td>
<td>3380</td>
<td>3940</td>
</tr>
<tr>
<td>T1</td>
<td>0°C</td>
<td>3°C</td>
</tr>
<tr>
<td>T2</td>
<td>10°C</td>
<td>12°C</td>
</tr>
<tr>
<td>T3</td>
<td>45°C</td>
<td>42°C</td>
</tr>
<tr>
<td>T4</td>
<td>60°C</td>
<td>55°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>10 kΩ</th>
<th>10 kΩ</th>
<th>47 kΩ</th>
<th>100 kΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>0°C</td>
<td>3°C</td>
<td>6°C</td>
<td>8°C</td>
</tr>
<tr>
<td>T2</td>
<td>10°C</td>
<td>12°C</td>
<td>13°C</td>
<td>14°C</td>
</tr>
<tr>
<td>T3</td>
<td>45°C</td>
<td>42°C</td>
<td>41°C</td>
<td>40°C</td>
</tr>
<tr>
<td>T4</td>
<td>60°C</td>
<td>55°C</td>
<td>53°C</td>
<td>51°C</td>
</tr>
</tbody>
</table>

The host processor can disable temperature-driven control of charging parameters by writing “1” to the TEMP_DIS bit. Since TEMP_DIS is reset whenever the IC resets its registers, the temperature controls are enforced whenever the IC is auto-charging, since auto-charge is always preceded by a reset of registers.

To disable the thermistor circuit, tie the NTC pin to GND. Before enabling the charger, the IC tests to see if NTC is shorted to GND. If NTC is shorted to GND, no thermistor readings occur and the NTC_OK and NTC1–NTC4 is reset.

The IC first measures the NTC immediately prior to entering any PWM charging state, then measures the NTC once per second, updating the result in NTC1–NTC4 bits (REG 12[3:0]).

### Table 10. NTC1–NTC4 DECODING

<table>
<thead>
<tr>
<th>TBAT (°C)</th>
<th>NTC4</th>
<th>NTC3</th>
<th>NTC2</th>
<th>NTC1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Above T4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Between T3 and T4</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Between T2 and T3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Below T1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

### Safety Register Settings

The IC contains a SAFETY register (REG06) that prevents the values of OREG (REG02[7:2]) and IOCHARGE (REG04[6:3]) from exceeding the values of VSAFE (REG06[3:0]) and ISAFE (REG06[7:4]) in the SAFETY register.

After VBAT rises above VSHORT, the SAFETY register is loaded with its default value and may be written to only before writing to any other register. The same 8-bit value should be written to the SAFETY register twice to set the register value. After writing to any other register, the SAFETY register is locked until VBAT falls below VSHORT.

If the host attempts to write a value higher than VSAFE or ISAFE to OREG or IOCHARGE, respectively; the VSAFE, ISAFE value appears as the OREG, IOCHARGE register value, respectively.

The Safety register is reset when the battery is below VSHORT and power is removed from VBUS.

See VSAFE and ISAFE Register Bit Definitions. (Table 17)

### Thermal Regulation and Shutdown

When the IC’s junction temperature reaches TCF (about 120°C), the charger reduces its output current to 550 mA to prevent overheating. If the temperature increases beyond TSHUTDOWN, charging is suspended, the FAULT bits are set to 101, and STAT is pulsed high. In Suspend Mode, all timers stop and the state of the IC’s logic is preserved. Charging resumes at programmed current after the die cools to about 120°C.

Note that as power dissipation increases, the effective $\theta_{JA}$ decreases due to the larger difference between the die temperature and ambient.

### Charge Mode Input Supply Protection

#### Input Supply Low-Voltage Detection

The IC continuously monitors VBUS during charging. If VBUS falls below VIN(MIN)2, the IC:

1. Terminates charging
2. Pulses the STAT pin, sets the STAT bits to “00”, and sets the FAULT bits to “011”

If VBUS recovers above the VIN(MIN)1 rising threshold after time tINT (about two seconds), the charging process is repeated. This function prevents the USB power bus from collapsing or oscillating when the IC is connected to a suspended USB port or a low-current-capable OTG device.

#### Input Over-Voltage Detection

When VBUS exceeds VBUSOVP, the IC:

1. Turns off Q3
2. Suspends charging
3. Sets the FAULT bits to “001”, sets the STAT bits to “11”, and pulses the STAT pin

When VBUS falls about 100 mV below VBUSOVP, the fault is cleared and charging resumes after VBUS is revalidated.

#### SYS Short During Discharge / Supplemental Mode

Caution should be taken to ensure the SYS pin is not shorted when connected to a battery. This condition can induce high current flow through the BATFET (Q4) and the external PMOS, if equipped, until the battery’s own safety circuit trips. The resulting high current can damage the IC.
Charge Mode Battery Detection & Protection

**VBAT Over−Voltage Protection**

The OREG voltage regulation loop prevents V_{BAT} from overshooting V_{OREG} by more than 50 mV when the battery is removed. When the PWM charger runs with no battery, the TE bit is not set and a battery is inserted that is charged to a voltage higher than V_{OREG}; PWM pulses stop. If no further pulses occur for 30 ms, the IC sets the FAULT bits to “100”, sets the STAT bits to “11”, and pulses the STAT pin.

**Battery Detection during Charging**

The IC can detect the presence, absence, or removal of a battery if the termination bit (TE) is set to “1” and CE# = “0”. During normal charging, once V_{BAT} is close to V_{OREG} and the charge current falls below I_{TERM}; the PWM charger continues to provide power to SYS and Q4 is turned off. It then turns on a discharge current, I_{DETECT}, for t_{DETECT}. If V_{BAT} is still above V_{OREG} − V_{RCCH}, the battery is present and the IC sets the STAT bits to “10” (Charge Done). If V_{BAT} is below V_{OREG} − V_{RCCH}, the battery is absent and the IC:
1. Sets the charging parameters to their default values
2. Sets the FAULT bits to “111” (Battery Absent) and sets the NOBAT bit
3. If EOC = “0”, the IC turns off the PWM for t_{INT}, then resumes charging and retries Battery Detection. If the battery is still absent, the process repeats with the “No Battery” fault re−enunciated
4. If EOC = “1”, the PWM remains on to provide power to SYS, but charge termination and the battery absent test are performed every t_{INT}

**Linear Charging**

If the battery voltage is below the short−circuit threshold (V_{SHORT}); a linear current source, I_{SHORT} charges V_{BAT} until V_{BAT} > V_{SHORT}.

**PRODUCTION TEST MODE (PTM)**

PTM provides 4.20 V at up to 2.3 A to V_{BAT} when V_{BUS} = 5.5 V ±5%.

The IC enters PTM when the PROD (REG05[6]) bit is set after the NOBAT (REG11[3]) bit has been set. The NOBAT bit indicates that the IC has detected battery absence. A battery absence detection test is performed automatically at current termination. The steps for entering PTM should include: set the TE (REG01[3]) bit high, set the CE# (REG01[2]) bit low, wait for the NOBAT bit to set HIGH, then set the PROD bit to “1” to enter PTM. Battery absence detection is completed within 500 ms from the time that CE# is set.

In PTM, the GATE bit (REG11[7]) is LOW, Q5 is on, and all auxiliary control loops are disabled. Only the OREG loop is active, which controls V_{BAT} to 4.20 V, regardless of the OREG register setting. Thermal shutdown remains active.

During PTM, high current pulses (load currents greater than 1.5 A) must be limited to 20% duty cycle with a minimum period of 10 ms.

---

**Table 11. ENABLING BOOST**

<table>
<thead>
<tr>
<th>HZ_MODE</th>
<th>OPA_MODE</th>
<th>BOOST</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>Enabled</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>Disabled</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

If WD_DIS = “0”, to remain in Boost Mode, the TMR_RST must be set by the host before the t_{32S} timer times out. If t_{32S} times out in Boost Mode; the IC resets all registers, pulses the STAT pin, sets the FAULT bits to 110, and resets the BOOST bit. VBUS POR or reading REG00 clears the fault condition.

**Boost PWM Control**

The IC uses a minimum on−time and computed minimum off−time to regulate V_{BUS}. The regulator achieves excellent transient response by employing current−mode modulation. This technique causes the regulator to exhibit a load line. The output voltage drops slightly as the output current rises. With a constant V_{BAT}, this appears as a constant output resistance.

The “droop” caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with no undershoot from the load line. This can be seen in Figure 31 and Figure 36.

**Figure 36. Output Resistance (R_{OUT})**

V_{BUS} as a function of I_{LOAD} can be computed when the regulator is in PWM Mode (continuous conduction) as:

\[ V_{OUT} = 5.07 - R_{OUT} \times I_{LOAD} \]  \hspace{1cm} (eq. 1)

At V_{BAT} = 3.0 V and I_{LOAD} = 300 mA, V_{BUS} drops to:

\[ V_{OUT} = 5.07 - 0.30 \times 0.3 = 4.98 V \]  \hspace{1cm} (eq. 2)

At V_{BAT} = 3.6 V and I_{LOAD} = 500 mA, V_{BUS} drops to:

\[ V_{OUT} = 5.07 - 0.24 \times 0.5 = 4.95 V \]  \hspace{1cm} (eq. 3)
PFM Mode
If $V_{BUS} > V_{REF\text{BOOST}}$ (nominally 5.07 V) when the minimum off–time ends, the regulator enters PFM Mode. Boost pulses are inhibited until $V_{BUS} < V_{REF\text{BOOST}}$. The minimum on–time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore, the regulator behaves like a constant on–time regulator, with the bottom of its output voltage ripple at 5.07 V in PFM Mode.

Table 12. BOOST PWM OPERATING STATES

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
<th>Invoked When</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIN</td>
<td>Linear Startup</td>
<td>$V_{BAT} &gt; V_{BUS}$</td>
</tr>
<tr>
<td>SS</td>
<td>Boost Soft–Start</td>
<td>$V_{BUS} &lt; V_{BST}$</td>
</tr>
<tr>
<td>BST</td>
<td>Boost Operating Mode</td>
<td>$V_{BAT} &gt; UVLO_{BST}$ and SS Completed</td>
</tr>
</tbody>
</table>

Startup
When the boost regulator is shut down, current flow is prevented from $V_{BAT}$ to $V_{BUS}$, as well as reverse flow from $V_{BUS}$ to $V_{BAT}$.

LIN State
When the boost is enabled by setting $\text{OPA}_\text{MODE} = 1$ and $\text{HZ}_\text{MODE} = 0$, if $V_{BAT} > UVLO_{BST}$, the regulator first attempts to bring PMID to within approximately 500 mV of $V_{BAT}$ using an internal 1100 mA limited current source from $V_{BAT}$. If PMID has not achieved $V_{BAT} - 500$ mV after 8 ms, a fault state is declared.

SS State
Once PMID > $V_{BAT} - 500$ mV, Q3 begins to close, connecting $V_{BUS}$ to PMID, and the boost regulator begins switching with a reduced peak current limit of 50% of it nominal current limit for up to 128 $\mu$s. After the 128 $\mu$s, the peak current limit is increased to 100%.

If the output fails to achieve 95% of its setpoint within 4 ms, while the peak current limit is 100%, a restart cycle is initiated. Up to 15 restart attempts will be made before a fault is declared.

Once the voltage reaches 95%, the device begins to increment the voltage in 50 mV steps, every 512 $\mu$s, until full regulation is achieved.

During the soft start state, the high–side FET (Q1) is operated asynchronously until PMID > $V_{BAT}$.

BST State
This is the normal operating mode of the regulator. The regulator uses a calculated $t_{OFF}$, modulated $t_{ON}$ scheme. The calculated $t_{OFF}$ is proportional to $V_{IN}/V_{OUT}$, which keeps the regulator’s switching frequency reasonably constant in CCM. $t_{ON,(MIN)}$ is proportional to $V_{BAT}$ and is a higher value if the inductor current reached 0 before $t_{OFF,(MIN)}$ in the prior cycle.

To ensure $V_{BUS}$ does not overshoot the regulation point, the boost switch remains off as long as $V_{BUS} > V_{REF\text{BOOST}}$.

If a USB peripheral hot insertion causes $V_{BUS}$ to dip below $V_{BAT}$, the device will commence a restart without faulting.

Boost Faults
If a BOOST fault occurs:
1. The STAT pin pulses
2. OPA_MODE bit is reset
3. The power stage is in High–Impedance Mode
4. The FAULT bits (REG0[2:0]) are set per Table 13.

Restart After Boost Faults
OPA_MODE is reset on boost faults. Boost Mode can only be re–enabled by setting the OPA_MODE bit.

Table 13. FAULT BITS DURING BOOST MODE

<table>
<thead>
<tr>
<th>Fault Bit</th>
<th>Fault (REG00h[2:0]) Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B2 B1 B0</td>
<td>Normal (no fault)</td>
</tr>
<tr>
<td>0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 0 1</td>
<td>$V_{BUS} &lt; VBUS_{DVP}$</td>
</tr>
<tr>
<td>0 1 0</td>
<td>$V_{BUS}$ fails to achieve the voltage required to advance to the next state during soft–start or sustained (&gt; 50 $\mu$s) current limit during the BST state</td>
</tr>
<tr>
<td>0 1 1</td>
<td>$V_{BAT} &lt; UVLO_{BST}$</td>
</tr>
<tr>
<td>1 0 0</td>
<td>NA: This code does not appear</td>
</tr>
<tr>
<td>1 0 1</td>
<td>Thermal shutdown</td>
</tr>
<tr>
<td>1 1 0</td>
<td>Timer fault; all registers reset</td>
</tr>
<tr>
<td>1 1 1</td>
<td>NA: This code does not appear</td>
</tr>
</tbody>
</table>
I2C INTERFACE

The FAN54063’s serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Mode I2C bus specifications. The FAN54063 SCL line is an input and the SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 14. I2C SLAVE ADDRESS BYTE

<table>
<thead>
<tr>
<th></th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In hex notation, the slave address assumes a 0 LSB. The hex slave address is D6 for all parts in the family. Other slave addresses can be accommodated upon request. Contact an onsemi representative.

Bus Timing

Shown in Figure 37, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

Transactions end with a STOP condition, which is SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 39.

![Figure 37. Data Transfer Timing](image)

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 38.

![Figure 38. Start Bit](image)

![Figure 39. Stop Bit](image)

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus Mode (less than 1 MHz clock); slaves do not ACK the transmission.

The master then generates a repeated start condition that causes all slaves on the bus to switch to HS Mode. The master then sends I2C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit is sent by the master. While in HS Mode, packets are separated by repeated start conditions (Figure 40).
Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus, and All addresses and data are MSB first.

Table 15. BIT DEFINITIONS FOR FIGURE 41 – FIGURE 44

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>START, see Figure 38</td>
</tr>
<tr>
<td>A</td>
<td>ACK. The slave drives SDA to 0 to acknowledge the preceding packet</td>
</tr>
<tr>
<td>A</td>
<td>NACK. The slave sends a 1 to NACK the preceding packet</td>
</tr>
<tr>
<td>R</td>
<td>Repeated START, see Figure 40</td>
</tr>
<tr>
<td>P</td>
<td>STOP, see Figure 39</td>
</tr>
</tbody>
</table>

Multi–Byte (Sequential) Read and Write Transactions

Sequential Write

The Slave Address, Reg Addr address, and the first data byte are transmitted to the FAN54063 in the same way as in a byte write Figure 41. However, instead of generating a Stop condition, the master transmits additional bytes that are written to consecutive sequential registers after the falling edge of the eighth bit. After the last byte written and its ACK bit received, the master issues a STOP bit. The IC contains an 8-bit counter that increments the address pointer after each byte is written.

Sequential Read

Sequential reads are initiated in the same way as a single-byte read, except that once the slave transmits the first data byte, the master issues an acknowledge instead of a STOP condition. This directs the slave’s I^2C logic to transmit the next sequentially addressed 8-bit word. The FAN54063 contains an 8-bit counter that increments the address pointer after each byte is read, which allows the entire memory contents to be read during one I^2C transaction.
REGISTER DESCRIPTIONS

The Twelve user-accessible IC registers are defined in Table 17.

Table 16. I2C REGISTER MAP

<table>
<thead>
<tr>
<th>Register</th>
<th>Name</th>
<th>REG#</th>
<th>BIT NAME</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CONTROL0</td>
<td>0H</td>
<td>TMR_RST</td>
<td>EN_STAT</td>
<td>STAT</td>
<td>BOOST</td>
<td>FAULT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CONTROL1</td>
<td>1H</td>
<td>IBUSLIM</td>
<td>VLOWV</td>
<td>TE</td>
<td>CE#</td>
<td>HZ_MODE</td>
<td>OPA_MODE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OREG</td>
<td>2H</td>
<td>OREG</td>
<td>DBAT_B</td>
<td>EOC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IC_INFO</td>
<td>3H</td>
<td>Vendor Code</td>
<td>PN</td>
<td>REVISION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IBAT</td>
<td>4H</td>
<td>RESET</td>
<td>IOCHARGE</td>
<td>TERM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VBUS_CONTROL</td>
<td>5H</td>
<td>Reserved</td>
<td>PROD</td>
<td>IO_LEVEL</td>
<td>VBUS_CON</td>
<td>VLIM</td>
<td>VBUSLIM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SAFETY</td>
<td>6H</td>
<td></td>
<td>ISAFE</td>
<td>VSAFE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>POST_CHARGING</td>
<td>7H</td>
<td>Reserved</td>
<td>Reserved</td>
<td>VBUS_LOAD</td>
<td>PC_EN</td>
<td>PC_IT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MONITOR0</td>
<td>10H</td>
<td>ITERM_CMP</td>
<td>VBAT_CMP</td>
<td>LINCHG</td>
<td>T_120</td>
<td>ICHG</td>
<td>IBUS</td>
<td>VBUS_VALID</td>
<td>CV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MONITOR1</td>
<td>11H</td>
<td>GATE</td>
<td>VBAT</td>
<td>POK_B</td>
<td>DIS_LEVEL</td>
<td>NOBAT</td>
<td>PC_ON</td>
<td>Reserved</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td></td>
<td>NTC</td>
<td>12H</td>
<td>Reserved</td>
<td>TEMP_DIS</td>
<td>NTC_OK</td>
<td>NTC4</td>
<td>NTC3</td>
<td>NTC2</td>
<td>NTC1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>WD_CONTROL</td>
<td>13H</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>EN_REG</td>
<td>WD_DIS</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RESTART</td>
<td>FA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 17. REGISTER BIT DEFINITIONS
This table defines the operation of each register bit. Default values are in bold text.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CONTROL0</td>
<td></td>
<td></td>
<td><strong>REGISTER ADDRESS: 00H</strong> <strong>DEFAULT VALUE = 0100 0000 (40h)</strong></td>
</tr>
<tr>
<td>7</td>
<td>TMR_RST</td>
<td>0</td>
<td>W</td>
<td>Writing a 1 resets the t32S timer; writing a 0 has no effect. Reading this bit always returns 0</td>
</tr>
<tr>
<td>6</td>
<td>EN_STAT</td>
<td>0</td>
<td>R/W</td>
<td>Prevents STAT pin from going LOW during charging; STAT pin still pulses to enunciate faults</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Enables STAT pin to be LOW when IC is charging</td>
</tr>
<tr>
<td>5:4</td>
<td>STAT</td>
<td>00</td>
<td>R</td>
<td><strong>Bit</strong> <strong>STAT Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>BOOST</td>
<td>0</td>
<td>R</td>
<td>IC is not in Boost Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>IC is in Boost Mode</td>
</tr>
<tr>
<td>2:0</td>
<td>FAULT</td>
<td>000</td>
<td>See</td>
<td><strong>Fault Bit</strong> <strong>Type</strong> <strong>FAULT Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>For Boost Mode faults, see Table 13.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CONTROL1</td>
<td></td>
<td></td>
<td><strong>REGISTER ADDRESS: 01H</strong> <strong>DEFAULT VALUE = 0011 0100 (34h)</strong></td>
</tr>
<tr>
<td>7:6</td>
<td>IBUSLIM</td>
<td>00</td>
<td>R/W</td>
<td>Input current limit Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td></td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>5:4</td>
<td>VLOWV</td>
<td>11</td>
<td>R/W</td>
<td>Weak battery voltage threshold Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>TE</td>
<td>0</td>
<td>R/W</td>
<td>Setting the TE bit to a 1 will enable Charge Termination.</td>
</tr>
<tr>
<td>2</td>
<td>CE#</td>
<td>1</td>
<td>R/W</td>
<td>This is an active low bit and by setting the bit to a “0” will enable Charging. When the bit is reset, it will return to the “1” state and charging will be disabled.</td>
</tr>
<tr>
<td>1</td>
<td>HZ_MODE</td>
<td>0</td>
<td>R/W</td>
<td>Setting this bit to a “1” puts the device in High Impedance mode. See Table 11</td>
</tr>
<tr>
<td>0</td>
<td>OPA_MODE</td>
<td>0</td>
<td>R/W</td>
<td>The device is in Charge Mode when the OPA_MODE bit = 0 and in Boost Operation when the bit = 1.</td>
</tr>
</tbody>
</table>
Table 17. REGISTER BIT DEFINITIONS (continued)
This table defines the operation of each register bit. Default values are in bold text.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:2</td>
<td>OREG</td>
<td>000010</td>
<td>R/W</td>
<td>Charger output &quot;float&quot; voltage, programmable from 3.51 to 4.45 V in 20 mV increments.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Dec          Hex</td>
</tr>
<tr>
<td>0</td>
<td>00</td>
<td>3.51</td>
<td>16</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>01</td>
<td>3.53</td>
<td>17</td>
<td>11</td>
</tr>
<tr>
<td>2</td>
<td>02</td>
<td>3.55</td>
<td>18</td>
<td>12</td>
</tr>
<tr>
<td>3</td>
<td>03</td>
<td>3.57</td>
<td>19</td>
<td>13</td>
</tr>
<tr>
<td>4</td>
<td>04</td>
<td>3.59</td>
<td>20</td>
<td>14</td>
</tr>
<tr>
<td>5</td>
<td>05</td>
<td>3.61</td>
<td>21</td>
<td>15</td>
</tr>
<tr>
<td>6</td>
<td>06</td>
<td>3.63</td>
<td>22</td>
<td>16</td>
</tr>
<tr>
<td>7</td>
<td>07</td>
<td>3.65</td>
<td>23</td>
<td>17</td>
</tr>
<tr>
<td>8</td>
<td>08</td>
<td>3.67</td>
<td>24</td>
<td>18</td>
</tr>
<tr>
<td>9</td>
<td>09</td>
<td>3.69</td>
<td>25</td>
<td>19</td>
</tr>
<tr>
<td>10</td>
<td>0A</td>
<td>3.71</td>
<td>26</td>
<td>1A</td>
</tr>
<tr>
<td>11</td>
<td>0B</td>
<td>3.73</td>
<td>27</td>
<td>1B</td>
</tr>
<tr>
<td>12</td>
<td>0C</td>
<td>3.75</td>
<td>28</td>
<td>1C</td>
</tr>
<tr>
<td>13</td>
<td>0D</td>
<td>3.77</td>
<td>29</td>
<td>1D</td>
</tr>
<tr>
<td>14</td>
<td>0E</td>
<td>3.79</td>
<td>30</td>
<td>1E</td>
</tr>
<tr>
<td>15</td>
<td>0F</td>
<td>3.81</td>
<td>31</td>
<td>1F</td>
</tr>
<tr>
<td>1</td>
<td>DBAT_B</td>
<td>0</td>
<td>R/W</td>
<td>Indicates that the IC detected a dead battery after VBUS_POR.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a “1” or a “0” to this bit does not affect charger operation. The bit state will not change until the next VBUS POR.</td>
</tr>
<tr>
<td>0</td>
<td>EOC</td>
<td>0</td>
<td>R/W</td>
<td>If TE = &quot;1&quot;, and no battery is detected at ITERM, the IC turns off the PWM for tINT, then resumes charging and retries Battery Detection. If the battery is still absent, the process repeats with the &quot;No Battery&quot; fault re-enunciated, and sets the charging parameters to the default values (see Charge State Flow Chart)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If no battery is detected when a full battery (end of charge) is reached, the PWM charger stays on, allowing the host processor to continue to run with no battery.</td>
</tr>
<tr>
<td>IC_INFO</td>
<td></td>
<td></td>
<td></td>
<td>REGISTER ADDRESS: 03H  DEFAULT VALUE = 1001 0XXX (9Xh)</td>
</tr>
<tr>
<td>7:6</td>
<td>Vendor Code</td>
<td>10</td>
<td>R</td>
<td>Identifies onsemi as the IC supplier</td>
</tr>
<tr>
<td>5:3</td>
<td>PN</td>
<td>010</td>
<td>R</td>
<td>Part number bits, see Ordering Information</td>
</tr>
<tr>
<td>2:0</td>
<td>REV</td>
<td>010</td>
<td>R</td>
<td>IC Revision bits</td>
</tr>
<tr>
<td>IBAT</td>
<td></td>
<td></td>
<td></td>
<td>REGISTER ADDRESS: 04H  DEFAULT VALUE = 1000 0001 (81h)</td>
</tr>
<tr>
<td>7</td>
<td>RESET</td>
<td>1</td>
<td>W</td>
<td>Conditions Functionality Settings the RESET bit clears all registers (except SAFETY and CE#) including WD_DIS and HZ_MODE. Setting the RESET bit clears all registers (except SAFETY) including WD_DIS, HZ_MODE and CE#. Setting the RESET bit clears all registers (except SAFETY and CE#) including WD_DIS and HZ_MODE. Writing a 0 has no effect; read returns 1</td>
</tr>
<tr>
<td>6:3</td>
<td>IOCHARGE</td>
<td>0000</td>
<td>R/W</td>
<td>Programs the typical charge current (550 mA default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Bit  I_OCHARGE (mA)</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1010–1111</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Table 17. REGISTER BIT DEFINITIONS (continued)
This table defines the operation of each register bit. Default values are in **bold** text.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IBAT</td>
<td></td>
<td></td>
<td><strong>REGISTER ADDRESS: 04H  DEFAULT VALUE = 1000 0001 (81h)</strong></td>
</tr>
<tr>
<td>2:0</td>
<td>ITERM</td>
<td>001</td>
<td>R/W</td>
<td>Sets the current used for charging termination</td>
</tr>
<tr>
<td></td>
<td>Bit ITERM (mA)</td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VBUS_CONTROL</td>
<td></td>
<td></td>
<td><strong>REGISTER ADDRESS: 05H  DEFAULT VALUE = 001X X100</strong></td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>0</td>
<td>R</td>
<td>This bit always returns 0</td>
</tr>
<tr>
<td>6</td>
<td>PROD</td>
<td>0</td>
<td>R/W</td>
<td>Charger operates in Normal Mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>Charger operates in Production Test Mode.</td>
</tr>
<tr>
<td>5</td>
<td>IO_LEVEL</td>
<td>0</td>
<td>R/W</td>
<td>Battery current is controlled by IOCHARGE and IBUSLIM bits while Fast Charging. During Precharge Mode, battery current is limited to 450 mA when IOCHARGE ≤ 750 mA and 730 mA when IOCHARGE &gt; 750 mA. IBUSLIM bits must be set to “10” or “11” or IO_LEVEL current will remain at 200 mA.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>Battery current control is set to 200 mA for Fast Charge and Precharge Mode.</td>
</tr>
<tr>
<td>4</td>
<td>VBUS_CON</td>
<td></td>
<td>R</td>
<td>1 Indicates that VBUS is above 4.4 V (rising) or 3.7 V (falling). When VBUS_CON changes from 0 to 1, a STAT pulse occurs.</td>
</tr>
<tr>
<td>3</td>
<td>VLIM</td>
<td>0</td>
<td>R</td>
<td>VBUS control loop is not active (VBUS is able to stay above VBUSLIM)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>VBUS control loop is active and VBUS is being regulated to VBUSLIM</td>
</tr>
<tr>
<td>2:0</td>
<td>VBUSLIM</td>
<td>100</td>
<td>R/W</td>
<td>VBUS control voltage reference</td>
</tr>
<tr>
<td></td>
<td>Bit VBUSLIM (V)</td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>4.213</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4.293</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>4.373</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>4.453</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4.533</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>4.613</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>4.693</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>4.773</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SAFETY</td>
<td></td>
<td></td>
<td><strong>REGISTER ADDRESS: 06H  DEFAULT VALUE = 0100 1010 (4Ah)</strong></td>
</tr>
<tr>
<td>7:4</td>
<td>ISAFE</td>
<td>0100</td>
<td>R/W</td>
<td>Sets the maximum IOCHARGE value used by the control circuit</td>
</tr>
<tr>
<td></td>
<td>Bit IOCHARGE(MAX) (mA)</td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>550</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>650</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>750</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>850</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>950</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1,050</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1,050</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1,250</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1,350</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1,450</td>
<td></td>
</tr>
<tr>
<td>1010–1111</td>
<td>1,550</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 17. REGISTER BIT DEFINITIONS (continued)
This table defines the operation of each register bit. Default values are in bold text.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAFETY</td>
<td>VSAFE</td>
<td>1010</td>
<td>R/W</td>
<td>Sets the maximum VOREG used by the control circuit</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>00</td>
<td>R/W</td>
<td>Sets the maximum VOREG used by the control circuit</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0</td>
<td>4.21</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>4.23</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>4.25</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>4.27</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>4.29</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>4.31</td>
</tr>
<tr>
<td>3</td>
<td>6</td>
<td>4.33</td>
</tr>
<tr>
<td>3</td>
<td>7</td>
<td>4.35</td>
</tr>
<tr>
<td>3</td>
<td>8</td>
<td>4.37</td>
</tr>
<tr>
<td>3</td>
<td>9</td>
<td>4.39</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>4.41</td>
</tr>
<tr>
<td>3</td>
<td>11</td>
<td>4.43</td>
</tr>
<tr>
<td>3</td>
<td>12</td>
<td>4.45</td>
</tr>
</tbody>
</table>

POST_CHARGING
REGISTER ADDRESS: 07H
DEFAULT VALUE = 0000 0001 (01h)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reserved</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>Reserved</td>
<td>00</td>
<td>R</td>
<td>These bits always return 0</td>
</tr>
<tr>
<td>5:4</td>
<td>VBUS_LOAD</td>
<td>00</td>
<td>R/W</td>
<td>After charger termination, in the charge done state, these bits control VBUS loading to improve detection of AC power removal from the AC adapter.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[5:4] VBUS Loading in Charge Done State:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00  None</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>01  Load VBUS for 4 ms every two seconds</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10  Load VBUS for 131 ms every two seconds</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>11  Load VBUS for 135 ms every two seconds</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0</td>
<td>None</td>
</tr>
<tr>
<td>5</td>
<td>01</td>
<td>Load VBUS for 4 ms every two seconds</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>Load VBUS for 131 ms every two seconds</td>
</tr>
<tr>
<td>5</td>
<td>11</td>
<td>Load VBUS for 135 ms every two seconds</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>0</td>
<td>Post charging or background charging feature is disabled</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>Post charging or background charging feature is enabled</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0</td>
<td>Sets the termination current for post charging</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>01</td>
<td>50 mA</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>100 mA</td>
</tr>
<tr>
<td>2</td>
<td>11</td>
<td>200 mA</td>
</tr>
<tr>
<td>2</td>
<td>101</td>
<td>300 mA</td>
</tr>
<tr>
<td>2</td>
<td>110</td>
<td>350 mA</td>
</tr>
<tr>
<td>2</td>
<td>111</td>
<td>400 mA</td>
</tr>
</tbody>
</table>

MONITOR0
REGISTER ADDRESS: 10H
DEFAULT VALUE = XXXX XXXX

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ITERM_CMP</td>
<td>R</td>
</tr>
<tr>
<td>6</td>
<td>VBAT_CMP</td>
<td>R</td>
</tr>
<tr>
<td>5</td>
<td>LINCHG</td>
<td>R</td>
</tr>
<tr>
<td>4</td>
<td>T_120</td>
<td>R</td>
</tr>
<tr>
<td>3</td>
<td>ICHG</td>
<td>R</td>
</tr>
<tr>
<td>2</td>
<td>IBUS</td>
<td>R</td>
</tr>
<tr>
<td>1</td>
<td>VBUS_VALID</td>
<td>R</td>
</tr>
<tr>
<td>0</td>
<td>CV</td>
<td>R</td>
</tr>
</tbody>
</table>

MONITOR1
REGISTER ADDRESS: 11H
DEFAULT VALUE = XX1X XX00

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>GATE</td>
<td>R</td>
</tr>
<tr>
<td>6</td>
<td>VBAT</td>
<td>R</td>
</tr>
</tbody>
</table>

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Table 17. REGISTER BIT DEFINITIONS (continued)
This table defines the operation of each register bit. Default values are in **bold** text.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>POK_B</td>
<td>1</td>
<td>R/W</td>
<td>POK_B indicates the state of the POK_B pin (see section on POK_B). This bit can be set to a 1 if VBAT has fallen below VLOWV, in turn the open drain POK_B pin will be Hi-Z.</td>
</tr>
<tr>
<td>4</td>
<td>DIS_LEVEL</td>
<td>R</td>
<td></td>
<td>This pin indicates the state of the DIS pin. A “1” indicates the DIS pin is high and the device is in a Hi-Z state on the input and the PWM controller is not running.</td>
</tr>
<tr>
<td>3</td>
<td>NOBAT</td>
<td>R</td>
<td></td>
<td>A “1” on this bit indicates that the device has determined there is no battery connected.</td>
</tr>
<tr>
<td>2</td>
<td>PC_ON</td>
<td>R</td>
<td></td>
<td>A “1” on this bit indicates that Post charging (background charging) is in progress.</td>
</tr>
<tr>
<td>1:0</td>
<td>Reserved</td>
<td>00</td>
<td>R</td>
<td>These bits always return 0.</td>
</tr>
</tbody>
</table>

NTC
REGISTER ADDRESS: 12H  DEFAULT VALUE = 000X XXXX

<table>
<thead>
<tr>
<th>7:6</th>
<th>Reserved</th>
<th>00</th>
<th>R</th>
<th>These bits always return 0.</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>TEMP_DIS</td>
<td>0</td>
<td>R/W</td>
<td>NTC Temperature measurement results affect charge parameters.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>R/W</td>
<td>NTC Temperature measurement results do not affect charge. Temperature measurements continue to be updated every second in the NTC1–4 monitor bits.</td>
</tr>
<tr>
<td>4</td>
<td>NTC_OK</td>
<td>R</td>
<td></td>
<td>0 if NTC is either shorted to GND, open, or shorted to REF.</td>
</tr>
<tr>
<td>3</td>
<td>NTC4</td>
<td>R</td>
<td></td>
<td>1 indicates that NTC is above the T4 threshold. See Battery Temperature (NTC) Monitor</td>
</tr>
<tr>
<td>2</td>
<td>NTC3</td>
<td>R</td>
<td></td>
<td>1 indicates that NTC is above the T3 threshold.</td>
</tr>
<tr>
<td>1</td>
<td>NTC2</td>
<td>R</td>
<td></td>
<td>1 indicates that NTC is above the T2 threshold.</td>
</tr>
<tr>
<td>0</td>
<td>NTC1</td>
<td>R</td>
<td></td>
<td>1 indicates that NTC is above the T1 threshold.</td>
</tr>
</tbody>
</table>

WD_CONTROL
REGISTER ADDRESS: 13H  DEFAULT VALUE = 0110 1110 (6Eh)

<table>
<thead>
<tr>
<th>7</th>
<th>Reserved</th>
<th>0</th>
<th>R</th>
<th>This bit always returns 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Reserved</td>
<td>1</td>
<td>R</td>
<td>This bit always returns 1</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
<td>1</td>
<td>R</td>
<td>This bit always returns 1</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
<td>0</td>
<td>R</td>
<td>This bit always returns 0</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>1</td>
<td>R</td>
<td>This bit always returns 1</td>
</tr>
<tr>
<td>2</td>
<td>EN_VREG</td>
<td>1</td>
<td>R/W</td>
<td>The EN_VREG defaults to a “1” enabling the regulator. To disable the regulator, set the bit to a “0”.</td>
</tr>
<tr>
<td>1</td>
<td>WD_DIS</td>
<td>1</td>
<td>R/W</td>
<td>A “1” disables the Watchdog (t32s) timer. Setting the bit to a “0” will enable the timers (See Safety Timer Section for further information).</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td>0</td>
<td>R</td>
<td>This bit always returns 0</td>
</tr>
</tbody>
</table>

RESTART
REGISTER ADDRESS: FAH  DEFAULT VALUE = 1111 1111 (FFh)

| 7:0 | RESTART | W |      | Writing B5h restarts charging when the IC is in the charge done state. This register reads back FF. |
PCB LAYOUT RECOMMENDATION

Bypass capacitors should be placed as close to the IC as possible. In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins. Power and ground pins should be routed directly to their bypass capacitors using the top copper layer. The copper area connecting to the IC should be maximized to improve thermal performance.

![Figure 45. PCB Layout Recommendation](image)

PRODUCT–SPECIFIC DIMENSIONS

<table>
<thead>
<tr>
<th>Product</th>
<th>D</th>
<th>E</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN54063UCX</td>
<td>2.40±0.030</td>
<td>2.00±0.030</td>
<td>0.180</td>
<td>0.380</td>
</tr>
</tbody>
</table>
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

WLCSP25 2.4x2.0x0.586
CASE 567SQ
ISSUE 0

DATE 30 NOV 2016

NOTES:
A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547–625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

DOCUMENT NUMBER: 98AON16612G
DESCRIPTION: WLCSP25 2.4x2.0x0.586