USB-Compliant Single-Cell Li-Ion Switching Charger with USB-OTG Boost Regulator

FAN54015

Description

The FAN54015 combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I2C Interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of external passive components.

The FAN54015 provides battery charging in three phases: conditioning, constant current and constant voltage.

To ensure USB compliance and minimize charging time, the input current limit can be changed through the I2C by the host processor. Charge termination is determined by a programmable minimum current level. A safety timer with reset control provides a safety backup for the I2C host. Charge status is reported to the host through the I2C port.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode, preventing leakage from the battery to the input. Charge current is reduced when the die temperature reaches 120°C, protecting the device and PCB from damage.

The FAN54015 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery and uses the same external components used for charging the battery.

Features

• Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
• Faster Charging than Linear
• Charge Voltage Accuracy: ±0.5% at 25°C
• ±1% from 0 to 125°C
• ±5% Input Current Regulation Accuracy
• ±5% Charge Current Regulation Accuracy
• 20 V Absolute Maximum Input Voltage
• 6 V Maximum Input Operating Voltage
• 1.45 A Maximum Charge Rate
• Programmable through High-Speed I2C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  ♦ Input Current
  ♦ Fast-Charge / Termination Current
  ♦ Charger Voltage
  ♦ Termination Enable

Features (continued)

• 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
• Small Footprint 1 mH External Inductor
• Safety Timer with Reset Control
• 1.8 V Regulated Output from VBUS for Auxiliary Circuits
• Dynamic Input Voltage Control
• Low Reverse Leakage to Prevent Battery Drain to VBUS
• 5 V, 500 mA Boost Mode for USB OTG for 3.0 V to 4.5 V Battery Input
• Available in a 1.96 x 1.87 mm, 20-bump, 0.4 mm Pitch WLCSP Package
• These are Pb-Free Devices

Applications

• Cell Phones, Smart Phones, PDAs
• Tablet, Portable Media Players
• Gaming Device, Digital Cameras
Table 1. FEATURE SUMMARY

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Slave Address</th>
<th>Automatic Charge</th>
<th>Special Charger (Note 1)</th>
<th>Safety Limits</th>
<th>Battery Absent Behavior</th>
<th>E2 Pin</th>
<th>VREG (E3 Pin)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN54015UCX</td>
<td>1101010</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>ON</td>
<td>DISABLE</td>
<td>1.8 V</td>
</tr>
</tbody>
</table>

1. A “special charger” is a current–limited charger that is not a USB compliant source.

Figure 2. IC and System Block Diagram
Table 2. RECOMMENDED EXTERNAL COMPONENTS

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Vendor</th>
<th>Parameter</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>1 μH ±20%, 1.6 A, DCR = 55 mΩ, 2520</td>
<td>Murata: LQM2HPN1R0</td>
<td>L</td>
<td>1.0</td>
<td>mH</td>
</tr>
<tr>
<td></td>
<td>1 μH ±30%, 1.4 A, DCR = 85 mΩ, 2016</td>
<td>Murata: LQM2MPN1R0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CBAT</td>
<td>10 μF, 20%, 6.3 V, X5R, 0603</td>
<td>Murata: GRM188R60J106M TDK: C1608X5R0J106M</td>
<td>C (Note 2)</td>
<td>4.7</td>
<td>mF</td>
</tr>
<tr>
<td>CMID</td>
<td>4.7 μF, 10%, 6.3 V, X5R, 0603</td>
<td>Murata: GRM188R60J475K TDK: C1608X5R0J475K</td>
<td>C</td>
<td>10</td>
<td>mF</td>
</tr>
<tr>
<td>CBUS</td>
<td>1.0 μF, 10%, 25 V, X5R, 0603</td>
<td>Murata GRM188R61E105K TDK:C1608X5R1E105M</td>
<td>C</td>
<td>1.0</td>
<td>mF</td>
</tr>
</tbody>
</table>

2. A 6.3 V rating is sufficient for CMID because PMID is protected from over-voltage surges on VBUS by Q3 (Figure 2).

Figure 3. WLCSP–20 Pin Assignments

PIN DEFINITIONS

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1, A2</td>
<td>VBUS</td>
<td>Charger Input Voltage and USB–OTG output voltage. Bypass with a 1 μF capacitor to PGND.</td>
</tr>
<tr>
<td>A3</td>
<td>NC</td>
<td>No Connect. No external connection is made between this pin and the IC’s internal circuitry.</td>
</tr>
<tr>
<td>A4</td>
<td>SCL</td>
<td>I2C Interface Serial Clock. This pin should not be left floating.</td>
</tr>
<tr>
<td>B1–B3</td>
<td>PMID</td>
<td>Power Input Voltage. Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 μF, 6.3 V capacitor to PGND.</td>
</tr>
<tr>
<td>B4</td>
<td>SDA</td>
<td>I2C Interface Serial Data. This pin should not be left floating.</td>
</tr>
<tr>
<td>C1 – C3</td>
<td>SW</td>
<td>Switching Node. Connect to output inductor.</td>
</tr>
<tr>
<td>C4</td>
<td>STAT</td>
<td>Status. Open–drain output indicating charge status. The IC pulls this pin LOW when charging.</td>
</tr>
<tr>
<td>D1 – D3</td>
<td>PGND</td>
<td>Power Ground. Power return for gate drive and power transistors. The connection from this pin to the bottom of CMBD should be as short as possible.</td>
</tr>
<tr>
<td>D4</td>
<td>OTG</td>
<td>On–The–Go. Enables boost regulator in conjunction with OTG_EN and OTG_PL bits (see Table 16). On VBUS Power–On Reset (POR), this pin sets the input current limit for</td>
</tr>
<tr>
<td></td>
<td></td>
<td>t15MIN charging.</td>
</tr>
<tr>
<td>E1</td>
<td>CSIN</td>
<td>Current–Sense Input. Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1 μF capacitor to PGND.</td>
</tr>
<tr>
<td>E2</td>
<td>DISABLE</td>
<td>Charge Disable. If this pin is HIGH, charging is disabled. When LOW, charging is controlled by the I2C registers. When this pin is HIGH, the 15–minute timer is reset. This pin does not affect the 32–second timer.</td>
</tr>
<tr>
<td>E3</td>
<td>VREG</td>
<td>Regulator Output. Connect to a 1 μF capacitor to PGND. This pin can supply up to 2mA of DC load current. The output voltage is PMID, which is limited to 1.8 V.</td>
</tr>
<tr>
<td>E4</td>
<td>VBAT</td>
<td>Battery Voltage. Connect to the positive (+) terminal of the battery pack. Bypass with a 0.1 μF capacitor to PGND if the battery is connected through long leads.</td>
</tr>
</tbody>
</table>
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{BUS} )</td>
<td>VBUS Voltage</td>
<td>1.4</td>
<td>20.0</td>
<td>V</td>
</tr>
<tr>
<td>( V_{STAT} )</td>
<td>STAT Voltage</td>
<td>-0.3</td>
<td>16.0</td>
<td>V</td>
</tr>
<tr>
<td>( V_I )</td>
<td>PMID Voltage</td>
<td>-</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Voltage on Other Pins</td>
<td>-0.3</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>( \frac{dV_{BUS}}{dt} )</td>
<td>Maximum VBUS Slope above 5.5 V when Boost or Charger are Active</td>
<td>-</td>
<td>4</td>
<td>V/\mu s</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge Protection Level</td>
<td>2000</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( T_J )</td>
<td>Junction Temperature</td>
<td>-60</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{STG} )</td>
<td>Storage Temperature</td>
<td>-65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>( T_L )</td>
<td>Lead Soldering Temperature, 10 Seconds</td>
<td></td>
<td>+260</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Lesser of 6.5 V or \( V_I + 0.3 \) V.

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{BUS} )</td>
<td>Supply Voltage</td>
<td>4</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{BAT(MAX)} )</td>
<td>Maximum Battery Voltage when Boost enabled</td>
<td>-</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td>( \frac{dV_{BUS}}{dt} )</td>
<td>Negative VBUS Slew Rate during VBUS Short Circuit, ( C_{MID} \leq 4.7 ) ( \mu F ) (see ( VBUS ) Short While Charging)</td>
<td>( T_A \leq 60^\circ C )</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>( \frac{dV_{BUS}}{dt} )</td>
<td></td>
<td>( T_A \geq 60^\circ C )</td>
<td>-</td>
<td>2</td>
</tr>
<tr>
<td>( T_A )</td>
<td>Ambient Temperature</td>
<td>-30</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>( T_J )</td>
<td>Junction Temperature (see Thermal Regulation and Protection section)</td>
<td>-30</td>
<td>+120</td>
<td>°C</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### THERMAL PROPERTIES

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{JA} )</td>
<td>Junction–to–Ambient Thermal Resistance</td>
<td>60</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \theta_{JB} )</td>
<td>Junction–to–PCB Thermal Resistance</td>
<td>20</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

Junction–to–ambient thermal resistance is a function of application and board layout. This data is measured with four–layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature \( T_J(max) \) at a given ambient temperature \( T_A \). For measured data, see Table 11.
### ELECTRICAL SPECIFICATIONS

(Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for \(T_J\) and \(T_A\); \(V_{BUS} = 5.0\) V; \(HZ\_MODE\); \(OPA\_MODE = 0\); (Charge Mode); SCL, SDA, OTG = 0 or 1.8 V; and typical values are for \(T_J = 25°C\))

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{VBUS})</td>
<td>VBUS Current</td>
<td>(V_{BUS} &gt; V_{BUS(min)}); PWM Switching</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{BUS} &gt; V_{BUS(min)}); PWM Enabled, Not Switching (Battery OVP Condition); (I_{IN}) Setting = 100 mA</td>
<td>–</td>
<td>2.5</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{LKG})</td>
<td>VBAT to VBUS Leakage Current</td>
<td>(0°C &lt; T_J &lt; 85°C), (HZ_MODE = 1), (V_{BAT} &lt; V_{LOWV}, 32S) Mode</td>
<td>–</td>
<td>63</td>
<td>90</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(I_{BAT})</td>
<td>Battery Discharge Current in High-Impedance Mode</td>
<td>(0°C &lt; T_J &lt; 85°C), (HZ_MODE = 1), (V_{BAT} = 4.2) V, (V_{BUS} = 0) V, DISABLE = 1, (0°C &lt; T_J &lt; 85°C), (V_{BAT} = 4.2) V</td>
<td>–</td>
<td>–</td>
<td>20</td>
<td>(\mu)A</td>
</tr>
</tbody>
</table>

### CHARGER VOLTAGE REGULATION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OREG})</td>
<td>Charge Voltage Range</td>
<td></td>
<td>3.5</td>
<td>–</td>
<td>4.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Charge Voltage Accuracy</td>
<td>(T_A = 25°C)</td>
<td>–0.5%</td>
<td>–</td>
<td>+0.5%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_J = 0) to (125°C)</td>
<td>–1%</td>
<td>–</td>
<td>+1%</td>
<td></td>
</tr>
</tbody>
</table>

### CHARGING CURRENT REGULATION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{OCHRG})</td>
<td>Output Charge Current Range</td>
<td>(V_{LOWV} &lt; V_{BAT} &lt; V_{OREG}, R_{SENSE} = 68) m(\Omega)</td>
<td>550</td>
<td>–</td>
<td>1450</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(20) m(V) (\leq I_{REG} \leq 40) m(V)</td>
<td>92</td>
<td>97</td>
<td>102</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Charge Current Accuracy Across (R_{SENSE})</td>
<td>(V_{IREG} &gt; 40) m(V)</td>
<td>94</td>
<td>97</td>
<td>100</td>
<td>%</td>
</tr>
</tbody>
</table>

### WEAK BATTERY DETECTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{LOWV})</td>
<td>Weak Battery Threshold Range</td>
<td></td>
<td>3.4</td>
<td>–</td>
<td>3.7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Weak Battery Threshold Accuracy</td>
<td></td>
<td>–5</td>
<td>–</td>
<td>+5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Weak Battery Deglitch Time</td>
<td>Rising Voltage</td>
<td>–</td>
<td>30</td>
<td>–</td>
<td>ms</td>
</tr>
</tbody>
</table>

### LOGIC LEVELS: DISABLE, SDA, SCL, OTG

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IH})</td>
<td>High-Level Input Voltage</td>
<td></td>
<td>1.05</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Low-Level Input Voltage</td>
<td></td>
<td>–</td>
<td>–</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IN})</td>
<td>Input Bias Current</td>
<td>Input Tied to GND or (V_{IN})</td>
<td>–</td>
<td>0.01</td>
<td>1.00</td>
<td>(\mu)A</td>
</tr>
</tbody>
</table>

### CHARGE TERMINATION DETECTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{(TERM)})</td>
<td>Termination Current Range</td>
<td>(V_{BAT} &gt; V_{OREG} – V_{ACH}, R_{SENSE} = 68) m(\Omega)</td>
<td>50</td>
<td>–</td>
<td>400</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Termination Current Accuracy</td>
<td>([V_{CSIN} – V_{BAT}]) from (3) m(V) to (20) m(V)</td>
<td>–25</td>
<td>–</td>
<td>+25</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>([V_{CSIN} – V_{BAT}]) from (20) m(V) to (40) m(V)</td>
<td>–5</td>
<td>–</td>
<td>+5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Termination Current Deglitch Time</td>
<td>(2) m(V) Overdrive</td>
<td>–</td>
<td>30</td>
<td>–</td>
<td>ms</td>
</tr>
</tbody>
</table>

### 1.8 V LINEAR REGULATOR

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{REG})</td>
<td>1.8 V Regulator Output</td>
<td>(I_{REG}) from 0 to 2 mA</td>
<td>1.7</td>
<td>1.8</td>
<td>1.9</td>
<td>V</td>
</tr>
</tbody>
</table>

### INPUT POWER SOURCE DETECTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IN(MIN1)})</td>
<td>VBUS Input Voltage Rising</td>
<td>To Initiate and Pass VBUS Validation</td>
<td>–</td>
<td>4.29</td>
<td>4.42</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IN(MIN2)})</td>
<td>Minimum VBUS During Charge</td>
<td>During Charging</td>
<td>–</td>
<td>3.71</td>
<td>3.94</td>
<td>V</td>
</tr>
<tr>
<td>(I_{VBUS, VALID})</td>
<td>VBUS Validation Time</td>
<td></td>
<td>–</td>
<td>30</td>
<td>–</td>
<td>ms</td>
</tr>
</tbody>
</table>

### SPECIAL CHARGER (VBUS)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{SP})</td>
<td>Special Charger Setpoint Accuracy</td>
<td></td>
<td>–3</td>
<td>–</td>
<td>+3</td>
<td>%</td>
</tr>
</tbody>
</table>
**ELECTRICAL SPECIFICATIONS** (Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for \( T_J \) and \( T_A \); \( V_{\text{BUS}} = 5.0 \text{ V} \); HZ_MODE; OPA_MODE = 0; (Charge Mode); SCL, SDA, OTG = 0 or 1.8 V; and typical values are for \( T_J = 25^\circ \text{C} \)) (continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{\text{INLIM}} )</td>
<td>Input Current Limit Threshold</td>
<td>( I_{\text{IN}} ) Set to 100 mA</td>
<td>88</td>
<td>93</td>
<td>98</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_{\text{IN}} ) Set to 500 mA</td>
<td>450</td>
<td>475</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{\text{REF}} )</td>
<td>Bias Regulator Voltage</td>
<td>( V_{\text{BUS}} &gt; V_{\text{IN(MIN)}} ) or ( V_{\text{BAT}} &gt; V_{\text{BAT(MIN)}} )</td>
<td>–</td>
<td>–</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Short–Circuit Current Limit</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{\text{RCH}} )</td>
<td>Recharge Threshold</td>
<td>Below ( V_{\text{OREG}} )</td>
<td>100</td>
<td>120</td>
<td>150</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Deglitch Time</td>
<td>( V_{\text{BAT}} ) Falling Below ( V_{\text{RCH}} ) Threshold</td>
<td>–</td>
<td>130</td>
<td>–</td>
</tr>
<tr>
<td>( V_{\text{STAT(OL)}} )</td>
<td>STAT Output Low</td>
<td>( I_{\text{STAT}} = 10 \text{ mA} )</td>
<td>–</td>
<td>–</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{STAT(OH)}} )</td>
<td>STAT High Leakage Current</td>
<td>( V_{\text{STAT}} = 5 \text{ V} )</td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_{\text{DETECT}} )</td>
<td>Battery Detection Current before Charge Done (Sink Current) (Note 4)</td>
<td>Begins after Termination Detected and ( V_{\text{BAT}} \leq V_{\text{OREG}} - V_{\text{RCH}} )</td>
<td>–</td>
<td>–</td>
<td>–0.80</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Battery Detection Time</td>
<td>–</td>
<td>–</td>
<td>262</td>
<td>ms</td>
</tr>
<tr>
<td>( V_{\text{SLP}} )</td>
<td>Sleep–Mode Entry Threshold, ( V_{\text{BUS}} - V_{\text{BAT}} )</td>
<td>( 2.3 \text{ V} \leq V_{\text{BAT}} \leq V_{\text{OREG}} - V_{\text{BUS}} ) Falling</td>
<td>0</td>
<td>0.04</td>
<td>0.10</td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{SLP_EXIT}} )</td>
<td>Deglitch Time for ( V_{\text{BUS}} ) Rising Above ( V_{\text{BAT}} ) by ( V_{\text{SLP}} )</td>
<td>Rising Voltage</td>
<td>–</td>
<td>30</td>
<td>–</td>
<td>ms</td>
</tr>
<tr>
<td>( R_{\text{DS(ON)}} )</td>
<td>Q3 On Resistance (( V_{\text{BUS}} ) to ( \text{PMID} ))</td>
<td>( I_{\text{IN(LIMIT)}} = 500 \text{ mA} )</td>
<td>–</td>
<td>180</td>
<td>250</td>
<td>m( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q1 On Resistance (PMID to SW)</td>
<td>–</td>
<td>130</td>
<td>225</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q2 On Resistance (SW to GND)</td>
<td>–</td>
<td>150</td>
<td>225</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{SW}} )</td>
<td>Oscillator Frequency</td>
<td>2.7</td>
<td>3.0</td>
<td>3.3</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( D_{\text{MAX}} )</td>
<td>Maximum Duty Cycle</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( D_{\text{MIN}} )</td>
<td>Minimum Duty Cycle</td>
<td>–</td>
<td>0</td>
<td>–</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{SYNC}} )</td>
<td>Synchronous to Non–Synchronous Current Cut–Off Threshold (Note 5)</td>
<td>Low–Side MOSFET (Q2) Cycle–by–Cycle Current Limit</td>
<td>–</td>
<td>140</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{\text{BOOST}} )</td>
<td>Boost Output Voltage at ( V_{\text{BUS}} )</td>
<td>( 2.5 \text{ V} &lt; V_{\text{BAT}} &lt; 4.5 \text{ V}, I_{\text{LOAD}} ) from 0 to 200 mA</td>
<td>4.80</td>
<td>5.07</td>
<td>5.17</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 3.0 \text{ V} &lt; V_{\text{BAT}} &lt; 4.5 \text{ V}, I_{\text{LOAD}} ) from 0 to 500 mA</td>
<td>4.77</td>
<td>5.07</td>
<td>5.17</td>
<td>V</td>
</tr>
<tr>
<td>( I_{\text{BAT(BOOST)}} )</td>
<td>Boost Mode Quiescent Current</td>
<td>PFM Mode, ( V_{\text{BAT}} = 3.6 \text{ V}, I_{\text{OUT}} = 0 )</td>
<td>–</td>
<td>140</td>
<td>300</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( I_{\text{LIMPK(BST)}} )</td>
<td>Q2 Peak Current Limit</td>
<td>1272</td>
<td>1590</td>
<td>1908</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( U_{\text{VLO(BST)}} )</td>
<td>Minimum Battery Voltage for Boost Operation</td>
<td>While Boost Active</td>
<td>–</td>
<td>2.42</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>To Start Boost Regulator</td>
<td>–</td>
<td>2.58</td>
<td>2.70</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{VBUS}} )</td>
<td>( V_{\text{BUS}} ) to PGND Resistance</td>
<td>Normal Operation</td>
<td>–</td>
<td>1500</td>
<td>–</td>
<td>k( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Charger Validation</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>( \Omega )</td>
</tr>
</tbody>
</table>
ELECTRICAL SPECIFICATIONS (Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; VBUS = 5.0 V; HZ_MODE; OPA_MODE = 0; (Charge Mode); SCL, SDA, OTG = 0 or 1.8 V; and typical values are for T_J = 25°C) (continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBUSOVP</td>
<td>VBUS Over-Voltage Shutdown</td>
<td>VBUS Rising</td>
<td>6.09</td>
<td>6.29</td>
<td>6.49</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>VBUS Falling</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>I_LMPK(CHG)</td>
<td>Q1 Cycle–by–Cycle Peak Current Limit</td>
<td>Charge Mode</td>
<td>–</td>
<td>2.3</td>
<td>–</td>
<td>A</td>
</tr>
<tr>
<td>VSHORT</td>
<td>Battery Short–Circuit Threshold</td>
<td>VBAT Rising</td>
<td>1.95</td>
<td>2.00</td>
<td>2.05</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>VBAT Falling</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>I_SHORT</td>
<td>Linear Charging Current</td>
<td>VBAT &lt; V_SHORT</td>
<td>20</td>
<td>30</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td>T_SHUTDOWN</td>
<td>Thermal Shutdown Threshold (Note 6)</td>
<td>T_J Rising</td>
<td>–</td>
<td>145</td>
<td>–</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysteresis (Note 6)</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>T_CF</td>
<td>Thermal Regulation Threshold</td>
<td>Charge Current Reduction Begins</td>
<td>–</td>
<td>120</td>
<td>–</td>
<td>°C</td>
</tr>
<tr>
<td>t_INT</td>
<td>Detection Interval</td>
<td>–</td>
<td>2.1</td>
<td>–</td>
<td>–</td>
<td>s</td>
</tr>
<tr>
<td>t_32S</td>
<td>32–Second Timer (Note 7)</td>
<td>Charger Enabled</td>
<td>20.5</td>
<td>25.2</td>
<td>28.0</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Charger Disabled</td>
<td>18.0</td>
<td>25.2</td>
<td>34.0</td>
<td></td>
</tr>
<tr>
<td>t_15MIN</td>
<td>15–Minute Timer</td>
<td>15–Minute Mode</td>
<td>12.0</td>
<td>13.5</td>
<td>15.0</td>
<td>min</td>
</tr>
<tr>
<td>ΔtLF</td>
<td>Low-Frequency Timer Accuracy</td>
<td>Charger Inactive</td>
<td>–25</td>
<td>–</td>
<td>25</td>
<td>%</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Negative current is current flowing from the battery to VBUS (discharging the battery).
5. Q2 always turns on for 60 ns, then turns off if current is below I_SYNC.
6. Guaranteed by design; not tested in production.
7. This tolerance (%) applies to all timers on the IC, including soft–start and deglitching timers.

I2C TIMING SPECIFICATIONS (Guaranteed by design)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fSCL</td>
<td>SCL Clock Frequency</td>
<td>Standard Mode</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>–</td>
<td>–</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, C_B ≤ 100 pF</td>
<td>–</td>
<td>–</td>
<td>3400</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, C_B ≤ 400 pF</td>
<td>–</td>
<td>–</td>
<td>1700</td>
<td></td>
</tr>
<tr>
<td>tBUF</td>
<td>Bus–Free Time between STOP and START Conditions</td>
<td>Standard Mode</td>
<td>–</td>
<td>4.7</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>–</td>
<td>1.3</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>tHD;STA</td>
<td>START or Repeated START Hold Time</td>
<td>Standard Mode</td>
<td>–</td>
<td>4</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>–</td>
<td>600</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode</td>
<td>–</td>
<td>160</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>tLOW</td>
<td>SCL LOW Period</td>
<td>Standard Mode</td>
<td>–</td>
<td>4.7</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>–</td>
<td>1.3</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, C_B ≤ 100 pF</td>
<td>–</td>
<td>160</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, C_B ≤ 400 pF</td>
<td>–</td>
<td>320</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>tHIGH</td>
<td>SCL HIGH Period</td>
<td>Standard Mode</td>
<td>–</td>
<td>4</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>–</td>
<td>600</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, C_B ≤ 100 pF</td>
<td>–</td>
<td>60</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High–Speed Mode, C_B ≤ 400 pF</td>
<td>–</td>
<td>120</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>tSU;STA</td>
<td>Repeated START Setup Time</td>
<td>Standard Mode</td>
<td>–</td>
<td>4.7</td>
<td>–</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>–</td>
<td>600</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>----------</td>
<td>----------------------------------</td>
<td>-------------------------------------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode</td>
<td>−</td>
<td>160</td>
<td>−</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Standard Mode</td>
<td>−</td>
<td>250</td>
<td>−</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>−</td>
<td>100</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode</td>
<td>−</td>
<td>10</td>
<td>−</td>
<td></td>
</tr>
<tr>
<td>tSU;DAT</td>
<td>Data Setup Time</td>
<td>Standard Mode</td>
<td>0</td>
<td>−</td>
<td>3.45</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>0</td>
<td>−</td>
<td>900</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 100) pF</td>
<td>0</td>
<td>−</td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 400) pF</td>
<td>0</td>
<td>−</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>tHD;DAT</td>
<td>Data Hold Time</td>
<td>Standard Mode</td>
<td>−</td>
<td>−</td>
<td>3.45</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>0</td>
<td>−</td>
<td>900</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 100) pF</td>
<td>0</td>
<td>−</td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 400) pF</td>
<td>0</td>
<td>−</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>tRCL</td>
<td>SCL Rise Time</td>
<td>Standard Mode</td>
<td>20 + 0.1 (C_B)</td>
<td>1000</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>20 + 0.1 (C_B)</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 100) pF</td>
<td>−</td>
<td>10</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 400) pF</td>
<td>−</td>
<td>20</td>
<td>160</td>
<td></td>
</tr>
<tr>
<td>tFCL</td>
<td>SCL Fall Time</td>
<td>Standard Mode</td>
<td>20 + 0.1 (C_B)</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>20 + 0.1 (C_B)</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 100) pF</td>
<td>−</td>
<td>10</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 400) pF</td>
<td>−</td>
<td>20</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>tRDA tRCL</td>
<td>SDA Rise Time</td>
<td>Standard Mode</td>
<td>20 + 0.1 (C_B)</td>
<td>1000</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Rise Time of SCL after a Repeated START Condition and after ACK Bit</td>
<td>Fast Mode</td>
<td>20 + 0.1 (C_B)</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 100) pF</td>
<td>−</td>
<td>10</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 400) pF</td>
<td>−</td>
<td>20</td>
<td>160</td>
<td></td>
</tr>
<tr>
<td>tFDA</td>
<td>SDA Fall Time</td>
<td>Standard Mode</td>
<td>20 + 0.1 (C_B)</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>20 + 0.1 (C_B)</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 100) pF</td>
<td>−</td>
<td>10</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode, (C_B \leq 400) pF</td>
<td>−</td>
<td>20</td>
<td>160</td>
<td></td>
</tr>
<tr>
<td>tSU;STO</td>
<td>Stop Condition Setup Time</td>
<td>Standard Mode</td>
<td>−</td>
<td>4</td>
<td>−</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast Mode</td>
<td>−</td>
<td>600</td>
<td>−</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High-Speed Mode</td>
<td>−</td>
<td>160</td>
<td>−</td>
<td>ns</td>
</tr>
<tr>
<td>(C_B)</td>
<td>Capacitive Load for SDA, SCL</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>400</td>
<td>pF</td>
</tr>
</tbody>
</table>
Figure 4. I²C Interface Timing for Fast and Slow Modes

Figure 5. I²C Interface Timing for High-Speed Mode

Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.
FAN54015

CHARGE MODE TYPICAL CHARACTERISTICS
(Unless otherwise specified, circuit of Figure 1, \(V_{\text{OREG}} = 4.2\) V, \(V_{\text{BUS}} = 5.0\) V, and \(T_A = 25\)°C)

Figure 6. Battery Charge Current vs. \(V_{\text{BUS}}\) with \(I_{\text{INLIM}} = 100\) mA

Figure 7. Battery Charge Current vs. \(V_{\text{BUS}}\) with \(I_{\text{INLIM}} = 500\) mA

Figure 8. Charger Efficiency, No \(I_{\text{INLIM}}\), \(I_{\text{OCHARGE}} = 1450\) mA

Figure 9. Charger Efficiency vs. \(V_{\text{BUS}}\), \(I_{\text{INLIM}} = 500\) mA

Figure 10. Auto-Charge Startup at \(V_{\text{BUS}}\) Plug-in, \(I_{\text{INLIM}} = 100\) mA, \(\text{OTG} = 1\), \(V_{\text{BAT}} = 3.4\) V

Figure 11. Auto-Charge Startup at \(V_{\text{BUS}}\) Plug-in, \(I_{\text{INLIM}} = 500\) mA, \(\text{OTG} = 1\), \(V_{\text{BAT}} = 3.4\) V

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CHARGE MODE TYPICAL CHARACTERISTICS

(Unless otherwise specified, circuit of Figure 1, \( V_{OREG} = 4.2 \) V, \( V_{BUS} = 5.0 \) V, and \( T_A = 25^\circ C \) (continued))

**Figure 12.** AutoCharge Startup with 300mA Limited Charger / Adaptor, \( I_{INLIM} = 500 \) mA, OTG = 1, \( V_{BAT} = 3.4 \) V

**Figure 13.** Charger Startup with HZ_MODE Bit Reset, \( I_{INLIM} = 500 \) mA, \( I_{OCHARGE} = 1050 \) mA, \( OREG = 4.2 \) V, \( V_{BAT} = 3.6 \) V

**Figure 14.** Battery Removal / Insertion During Charging, \( V_{BAT} = 3.9 \) V, \( I_{OCHARGE} = 1050 \) mA, No \( I_{INLIM} \), TE = 0

**Figure 15.** Battery Removal / Insertion During Charging, \( V_{BAT} = 3.9 \) V, \( I_{OCHARGE} = 1050 \) mA, No \( I_{INLIM} \), TE = 1
CHARGE MODE TYPICAL CHARACTERISTICS
(Unless otherwise specified, circuit of Figure 1, \( \text{VOREG} = 4.2 \text{ V} \), \( \text{VBUS} = 5.0 \text{ V} \), and \( \text{T_A} = 25^\circ \text{C} \)) (continued)

**Figure 16. VBUS Current in High–Impedance Mode with Battery Open**

**Figure 17. V\text{REG} 1.8 V Output Regulation**

**Figure 18. No Battery, V\text{BUS} at Power Up**
BOOST MODE TYPICAL CHARACTERISTICS
(Unless otherwise specified, using circuit of Figure 1, $V_{\text{BAT}} = 3.6 \text{ V}, T_A = 25^\circ \text{C}$)

Figure 19. Efficiency vs. $V_{\text{BAT}}$

Figure 20. Efficiency Over Temperature

Figure 21. Output Regulation vs. $V_{\text{BAT}}$

Figure 22. Output Regulation Over Temperature

Figure 23. Quiescent Current

Figure 24. High–Impedance Mode Battery Current
BOOST MODE TYPICAL CHARACTERISTICS
(Unless otherwise specified, using circuit of Figure 1, $V_{BAT} = 3.6\, \text{V}$, $T_A = 25^\circ\text{C}$)

Figure 25. Output Ripple vs. $V_{BAT}$

Figure 26. Output Ripple vs. Temperature

Figure 27. Boost PWM Waveform

Figure 28. Boost PFM Waveform
BOOST MODE TYPICAL CHARACTERISTICS
(Unless otherwise specified, using circuit of Figure 1, \( V_{BAT} = 3.6 \) V, \( T_A = 25^\circ \)C)

Figure 29. Startup, 3.6 \( V_{BAT} \), 44 \( \Omega \) Load, Additional 10 \( \mu \)F, X5R Across \( V_{BUS} \)

Figure 30. \( V_{BUS} \) Fault Response, 3.6 \( V_{BAT} \)

Figure 31. Load Transient, 5 − 155 − 5 mA, \( t_R = t_F = 100 \) ns

Figure 32. Load Transient, 5 − 255 − 5 mA, \( t_R = t_F = 100 \) ns
CIRCUIT DESCRIPTION / OVERVIEW

When charging batteries with a current−limited input source, such as USB, a switching charger’s high efficiency over a wide range of output voltages minimizes charging time.

FAN54015 combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5 V to USB On−The−Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The FAN54015 has three operating modes:

1. Charge Mode:
   Charges a single−cell Li−ion or Li−polymer battery.
2. Boost Mode:
   Provides 5 V power to USB−OTG with an integrated synchronous rectification boost regulator using the battery as input.
3. High−Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery.

NOTE: Default settings are denoted by bold typeface.

Charge Mode

In Charge Mode, FAN54015 employs four regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I2C interface.
2. Charging Current: Limits the maximum charging current. This current is sensed using an external RSENSE resistor.
3. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery’s internal impedance and RSENSE work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across RSENSE drops below the ITERM threshold.
4. Temperature: If the IC’s junction temperature reaches 120°C, charge current is reduced until the IC’s temperature stabilizes at 120°C.

The charger output or “float” voltage can be programmed by the OREG bits from 3.5 V to 4.44 V in 20 mV increments, as shown in Table 3.
Table 3. OREG BITS (OREG[7:2]) VS. CHARGER VOUT (VOREG) FLOAT VOLTAGE

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Hex</th>
<th>VOREG</th>
<th>Decimal</th>
<th>Hex</th>
<th>VOREG</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00</td>
<td>3.50</td>
<td>32</td>
<td>20</td>
<td>4.14</td>
</tr>
<tr>
<td>1</td>
<td>01</td>
<td>3.52</td>
<td>33</td>
<td>21</td>
<td>4.16</td>
</tr>
<tr>
<td>2</td>
<td>02</td>
<td>3.54</td>
<td>34</td>
<td>22</td>
<td>4.18</td>
</tr>
<tr>
<td>3</td>
<td>03</td>
<td>3.56</td>
<td>35</td>
<td>23</td>
<td>4.20</td>
</tr>
<tr>
<td>4</td>
<td>04</td>
<td>3.58</td>
<td>36</td>
<td>24</td>
<td>4.22</td>
</tr>
<tr>
<td>5</td>
<td>05</td>
<td>3.60</td>
<td>37</td>
<td>25</td>
<td>4.24</td>
</tr>
<tr>
<td>6</td>
<td>06</td>
<td>3.62</td>
<td>38</td>
<td>26</td>
<td>4.26</td>
</tr>
<tr>
<td>7</td>
<td>07</td>
<td>3.64</td>
<td>39</td>
<td>27</td>
<td>4.28</td>
</tr>
<tr>
<td>8</td>
<td>08</td>
<td>3.66</td>
<td>40</td>
<td>28</td>
<td>4.30</td>
</tr>
<tr>
<td>9</td>
<td>09</td>
<td>3.68</td>
<td>41</td>
<td>29</td>
<td>4.32</td>
</tr>
<tr>
<td>10</td>
<td>0A</td>
<td>3.70</td>
<td>42</td>
<td>2A</td>
<td>4.34</td>
</tr>
<tr>
<td>11</td>
<td>0B</td>
<td>3.72</td>
<td>43</td>
<td>2B</td>
<td>4.36</td>
</tr>
<tr>
<td>12</td>
<td>0C</td>
<td>3.74</td>
<td>44</td>
<td>2C</td>
<td>4.38</td>
</tr>
<tr>
<td>13</td>
<td>0D</td>
<td>3.76</td>
<td>45</td>
<td>2D</td>
<td>4.40</td>
</tr>
<tr>
<td>14</td>
<td>0E</td>
<td>3.78</td>
<td>46</td>
<td>2E</td>
<td>4.42</td>
</tr>
<tr>
<td>15</td>
<td>0F</td>
<td>3.80</td>
<td>47</td>
<td>2F</td>
<td>4.44</td>
</tr>
<tr>
<td>16</td>
<td>10</td>
<td>3.82</td>
<td>48</td>
<td>30</td>
<td>4.44</td>
</tr>
<tr>
<td>17</td>
<td>11</td>
<td>3.84</td>
<td>49</td>
<td>31</td>
<td>4.44</td>
</tr>
<tr>
<td>18</td>
<td>12</td>
<td>3.86</td>
<td>50</td>
<td>32</td>
<td>4.44</td>
</tr>
<tr>
<td>19</td>
<td>13</td>
<td>3.88</td>
<td>51</td>
<td>33</td>
<td>4.44</td>
</tr>
<tr>
<td>20</td>
<td>14</td>
<td>3.90</td>
<td>52</td>
<td>34</td>
<td>4.44</td>
</tr>
<tr>
<td>21</td>
<td>15</td>
<td>3.92</td>
<td>53</td>
<td>35</td>
<td>4.44</td>
</tr>
<tr>
<td>22</td>
<td>16</td>
<td>3.94</td>
<td>54</td>
<td>36</td>
<td>4.44</td>
</tr>
<tr>
<td>23</td>
<td>17</td>
<td>3.96</td>
<td>55</td>
<td>37</td>
<td>4.44</td>
</tr>
<tr>
<td>24</td>
<td>18</td>
<td>3.98</td>
<td>56</td>
<td>38</td>
<td>4.44</td>
</tr>
<tr>
<td>25</td>
<td>19</td>
<td>4.00</td>
<td>57</td>
<td>39</td>
<td>4.44</td>
</tr>
<tr>
<td>26</td>
<td>1A</td>
<td>4.02</td>
<td>58</td>
<td>3A</td>
<td>4.44</td>
</tr>
<tr>
<td>27</td>
<td>1B</td>
<td>4.04</td>
<td>59</td>
<td>3B</td>
<td>4.44</td>
</tr>
<tr>
<td>28</td>
<td>1C</td>
<td>4.06</td>
<td>60</td>
<td>3C</td>
<td>4.44</td>
</tr>
<tr>
<td>29</td>
<td>1D</td>
<td>4.08</td>
<td>61</td>
<td>3D</td>
<td>4.44</td>
</tr>
<tr>
<td>30</td>
<td>1E</td>
<td>4.10</td>
<td>62</td>
<td>3E</td>
<td>4.44</td>
</tr>
</tbody>
</table>

A new charge cycle begins when one of the following occurs:
- The battery voltage falls below $V_{OREG} - V_{RCH}$
- VBUS Power on Reset (POR) clears and the battery voltage is below the weak battery threshold ($V_{LOWV}$).
- CE or HZ_MODE is reset through I2C write to CONTROL1 (R1) register.

Charge Current Limit (I\textsubscript{O\textsubscript{CHARGE}})

Table 4. PROGRAMMABLE CHARGING PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage Regulation</td>
<td>V\textsubscript{OREG}</td>
<td>REG2[7:2]</td>
</tr>
<tr>
<td>Battery Charging Current Limit</td>
<td>I\textsubscript{O\textsubscript{CHARGE}}</td>
<td>REG4[6:4]</td>
</tr>
<tr>
<td>Input Current Limit</td>
<td>I\textsubscript{IN\textsubscript{LIM}}</td>
<td>REG1[7:6]</td>
</tr>
<tr>
<td>Charge Termination Limit</td>
<td>I\textsubscript{TERM}</td>
<td>REG4[2:0]</td>
</tr>
<tr>
<td>Weak Battery Voltage</td>
<td>V\textsubscript{LOWV}</td>
<td>REG1[5:4]</td>
</tr>
</tbody>
</table>

Table 5. I\textsubscript{O\textsubscript{CHARGE}} (REG4[6:4]) CURRENT AS FUNCTION OF I\textsubscript{O\textsubscript{CHARGE}} BITS AND R\textsubscript{S\textsubscript{ENSE}} RESISTOR VALUES

<table>
<thead>
<tr>
<th>DEC</th>
<th>BIN</th>
<th>HEX</th>
<th>VR\textsubscript{SENSE} \textsubscript{(mV)}</th>
<th>I\textsubscript{O\textsubscript{CHARGE}} \textsubscript{(mA)}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00</td>
<td>00</td>
<td>37.4</td>
<td>550</td>
</tr>
<tr>
<td>1</td>
<td>001</td>
<td>01</td>
<td>44.2</td>
<td>650</td>
</tr>
<tr>
<td>2</td>
<td>010</td>
<td>02</td>
<td>51.0</td>
<td>750</td>
</tr>
<tr>
<td>3</td>
<td>011</td>
<td>03</td>
<td>57.8</td>
<td>850</td>
</tr>
<tr>
<td>4</td>
<td>100</td>
<td>04</td>
<td>71.4</td>
<td>1050</td>
</tr>
<tr>
<td>5</td>
<td>101</td>
<td>05</td>
<td>78.2</td>
<td>1150</td>
</tr>
<tr>
<td>6</td>
<td>110</td>
<td>06</td>
<td>91.8</td>
<td>1350</td>
</tr>
<tr>
<td>7</td>
<td>111</td>
<td>07</td>
<td>98.6</td>
<td>1450</td>
</tr>
</tbody>
</table>

The following charging parameters can be programmed by the host through I2C:

Table 6. I\textsubscript{TERM} CURRENT AS FUNCTION OF I\textsubscript{TERM} BITS (REG4[2:0]) AND R\textsubscript{S\textsubscript{ENSE}} RESISTOR VALUES

<table>
<thead>
<tr>
<th>I\textsubscript{TERM}</th>
<th>VR\textsubscript{SENSE} \textsubscript{(mV)}</th>
<th>I\textsubscript{TERM} \textsubscript{(mA)}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3.3</td>
<td>49</td>
</tr>
<tr>
<td>1</td>
<td>6.6</td>
<td>97</td>
</tr>
<tr>
<td>2</td>
<td>9.9</td>
<td>146</td>
</tr>
<tr>
<td>3</td>
<td>13.2</td>
<td>194</td>
</tr>
<tr>
<td>4</td>
<td>16.5</td>
<td>243</td>
</tr>
<tr>
<td>5</td>
<td>19.8</td>
<td>291</td>
</tr>
<tr>
<td>6</td>
<td>23.1</td>
<td>340</td>
</tr>
<tr>
<td>7</td>
<td>26.4</td>
<td>388</td>
</tr>
</tbody>
</table>

Termination Current Limit

Current charge termination is enabled when TE (REG1[3]) = 1. Typical termination current values are given in Table 6.

When the charge current falls below $I_{TERM}$, PWM charging stops and the STAT bits change to READY (00) for about 500 ms while the IC determines whether the battery and charging source are still connected. STAT then changes to CHARGE DONE (10), provided the battery and charger are still connected.
PWM Controller in Charge Mode

The IC uses a current–mode PWM controller to regulate the output voltage and battery charge currents. The synchronous rectifier (Q2) has a current limit that which off the FET when the current is negative by more than 140 mA peak. This prevents current flow from the battery.

Safety Timer

Section references Figure 39.

At the beginning of charging, the IC starts a 15–minute timer (t15MIN). When this times out, charging is terminated. Writing to any register through I2C stops and resets the t15MIN timer, which in turn starts a 32–second timer (t32S). Setting the TMR_RST bit (REG0[7]) resets the t32S timer. If the t32S timer times out; charging is terminated, the registers are set to their default values, and charging resumes using the default values with the t15MIN timer running.

Normal charging is controlled by the host with the t32S timer running to ensure that the host is alive. Charging with the t15MIN timer running is used for charging that is unattended by the host. If the t15MIN timer expires; the IC turns off the charger, sets the CE bit, and indicates a timer fault (110) on the FAULT bits (REG0[2:0]). This sequence prevents overcharge if the host fails to reset the t32S timer.

VBUS POR / Non–Compliant Charger Rejection

When the IC detects that VBUS has risen above VIN(MIN)1 (4.4 V), the IC applies a 100 Ω load from VBUS to GND. To clear the VBUS POR (Power–On–Reset) and begin charging, VBUS must remain above VIN(MIN)1 and below VBUSOVP for TVBUS_VALID (30 ms) before the IC initiates charging. The VBUS validation sequence always occurs before charging is initiated or re–initiated (for example, after a VBUS OVP fault or a VRCH recharge initiation).

tVBUS_VALID ensures that unfiltered 50 / 60 Hz chargers and other non–compliant chargers are rejected.

USB–Friendly Boot Sequence

At VBUS POR, when the battery voltage is above the weak battery threshold (VLOWV), the IC operates in accordance with its I2C register settings. If VBAT < VLOWV, the IC sets all registers to their default values and enables the charger using an input current limit controlled by the OTG pin (100 mA if OTG is LOW and 500 mA if OTG is HIGH). This feature can revive a battery whose voltage is too low to ensure reliable host operation. Charging continues in the absence of host communication even after the battery has reached VOREG, whose default value is 3.54 V, and the charger remains active until t15MIN times out. Once the host processor begins writing to the IC, charging parameters are set by the host, which must continually reset the t32S timer to continue charging using the programmed charging parameters. If t32S times out, the register defaults are loaded, the FAULT bits are set to 110, STAT is pulsed HIGH, and charging continues with default charge parameters.

Input Current Limiting

To minimize charging time without overloading VBUS current limitations, the IC’s input current limit can be programmed by the IINLIM bits (REG1[7:6]).

<table>
<thead>
<tr>
<th>IINLIM REG1[7:6]</th>
<th>Input Current Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>100 mA</td>
</tr>
<tr>
<td>01</td>
<td>500 mA</td>
</tr>
<tr>
<td>10</td>
<td>800 mA</td>
</tr>
<tr>
<td>11</td>
<td>No limit</td>
</tr>
</tbody>
</table>

The OTG pin establishes the input current limit when t15MIN is running.
Figure 35. Charger VBUS PO
Figure 36. Charge Mode
FLOW CHARTS (continued)

Figure 37. Charge Configuration

Figure 38. HZ–State

Figure 39. Timer Flow Chart
Special Charger

The FAN54015 has additional functionality to limit input current in case a current–limited “special charger” is supplying VBUS. These slowly increase the charging current until either:

- $I_{INLIM}$ or $I_{OCHARGE}$ is reached
- $V_{BUS} = V_{SP}$

If $V_{BUS}$ collapses to $V_{SP}$ when the current is ramping up, the FAN54015 charge with an input current that keeps $V_{BUS} = V_{SP}$. When the $V_{SP}$ control loop is limiting the charge current, the SP bit (REG5[4]) is set.

Table 8. $V_{SP}$ AS FUNCTION OF SP BITS (REG5[2:0])

<table>
<thead>
<tr>
<th>SP (REG5[2:0])</th>
<th>DEC</th>
<th>BIN</th>
<th>HEX</th>
<th>$V_{SP}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>00</td>
<td>00</td>
<td>4.213</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>01</td>
<td>01</td>
<td>4.293</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>02</td>
<td>02</td>
<td>4.373</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>03</td>
<td>03</td>
<td>4.453</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>04</td>
<td>04</td>
<td>4.533</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>05</td>
<td>05</td>
<td>4.613</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>06</td>
<td>06</td>
<td>4.693</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>07</td>
<td>07</td>
<td>4.773</td>
</tr>
</tbody>
</table>

Safety Settings

FAN54015 contain a SAFETY register (REG6) that prevents the values in OREG (REG2[7:2]) and IOCHARGE (REG4[6:4]) from exceeding the values of the VSAFE and ISAFE values.

After $V_{BAT}$ exceeds $V_{SHORT}$, the SAFETY register is loaded with its default value and may be written only before any other register is written. The entire desired Safety register value should be written twice to ensure the register bits are set. After writing to any other register, the SAFETY register is locked until $V_{BAT}$ falls below $V_{SHORT}$.

The ISAFE (REG6[6:4]) and VSAFE (REG6[3:0]) registers establish values that limit the maximum values of $I_{OCHARGE}$ and $V_{OREG}$ used by the control logic. If the host attempts to write a value higher than VSAFE or ISAFE to OREG or IOCHARGE, respectively; the VSAFE, ISAFE value appears as the OREG, IOCHARGE register value, respectively.
Thermal Regulation and Protection
When the IC’s junction temperature reaches $T_{CF}$ (about 120°C), the charger reduces its output current to 550 mA to prevent overheating. If the temperature increases beyond $T_{SHUTDOWN}$, charging is suspended, the FAULT bits are set to 010, and STAT is pulsed HIGH. In Suspend Mode, all timers stop and the state of the IC’s logic is preserved. Charging resumes at programmed current after the die cools to about 120°C.

Additional $\theta_J$ data points, measured using the FAN54015 evaluation board, are given in Table 11 (measured with $T_A = 25^\circ$C). Note that as power dissipation increases, the effective $\theta_J$ decreases due to the larger difference between the die temperature and ambient.

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>$\theta_J$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.504</td>
<td>54°C/W</td>
</tr>
<tr>
<td>0.844</td>
<td>50°C/W</td>
</tr>
<tr>
<td>1.506</td>
<td>46°C/W</td>
</tr>
</tbody>
</table>

Charge Mode Input Supply Protection

Sleep Mode
When the IC’s junction temperature reaches $T_{CF}$ (about 120°C), the charger reduces its output current to 550 mA to prevent overheating. If the temperature increases beyond $T_{SHUTDOWN}$, charging is suspended, the FAULT bits are set to 010, and STAT is pulsed HIGH. In Suspend Mode, all timers stop and the state of the IC’s logic is preserved. Charging resumes at programmed current after the die cools to about 120°C.

Additional $\theta_J$ data points, measured using the FAN54015 evaluation board, are given in Table 11 (measured with $T_A = 25^\circ$C). Note that as power dissipation increases, the effective $\theta_J$ decreases due to the larger difference between the die temperature and ambient.

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>$\theta_J$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.504</td>
<td>54°C/W</td>
</tr>
<tr>
<td>0.844</td>
<td>50°C/W</td>
</tr>
<tr>
<td>1.506</td>
<td>46°C/W</td>
</tr>
</tbody>
</table>

Charge Mode Battery Detection & Protection

VBUS Short While Charging
If VBUS is shorted with a very low impedance while the IC is charging with $I_{INLIM} = 100$ mA, the IC may not meet datasheet specifications until power is removed. To trigger this condition, VBUS must be driven from 5 V to GND with a high slew rate. Achieving this slew rate requires a 0 Ω short to the USB cable less than 10 cm from the connector.

Battery Detection During Charging
The IC can detect the presence, absence, or removal of a battery if the termination bit (TE) is set. During normal charging, once VBAT is close to $V_{OREG}$ and the termination charge current is detected, the IC terminates charging and sets the STAT bits to 10. It then turns on a discharge current, $I_{DETECT}$, for $t_{DET}$: If $V_{BAT}$ is still above $V_{OREG} - V_{RCH}$, the battery is present and the IC sets the FAULT bits to 000. If $V_{BAT}$ is below $V_{OREG} - V_{RCH}$, the battery is absent and the IC:
1. Sets the registers to their default values.
2. Sets the FAULT bits to 111.
3. Resumes charging with default values after $t_{INT}$.

Battery Short–Circuit Protection
If the battery voltage is below the short–circuit threshold (VSHORT); a linear current source, ISHORT, supplies VBAT until $V_{BAT} > V_{SHORT}$.

System Operation with No Battery
The FAN54015 continues charging after VBUS POR with the default parameters, regulating the VBAT line to 3.54 V until the host processor issues commands or the 15–minute timer expires. In this way, the FAN54015 can start the system without a battery.

The FAN54015 soft–start function can interfere with the system supply with battery absent. The soft–start activates whenever $V_{OREG}$, $I_{INLIM}$, or OCHARGE are set from a lower to higher value. During soft–start, the $I_{IN}$ limit drops to 100 mA for about 1 ms unless $I_{INLIM}$ is set to 11 (no limit). This could cause the system processor to fail to start. To avoid this behavior, use the following sequence.
1. Set the OTG pin HIGH. When VBUS is plugged in, $I_{INLIM}$ is set to 500 mA until the system processor powers up and can set parameters through I2C.
2. Program the Safety Register.
3. Set $I_{INLIM}$ to 11 (no limit).
4. Set OREG to the desired value (typically 4.18).
5. Reset the IO_LEVEL bit, then set IOCHARGE.
6. Set $I_{INLIM}$ to 500 mA if a USB source is connected.
During the initial system startup, while the charger IC is being programmed, the system current is limited to 500 mA for 1 ms during steps 4 and 5. This is the value of the soft−start ICHARGE current used when IINLIM is set to No Limit.

If the system is powered up without a battery present, the CV bit should be set. When a battery is inserted, the CV bit is cleared.

Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 12. STAT PIN FUNCTION

<table>
<thead>
<tr>
<th>EN_STAT</th>
<th>Charge State</th>
<th>STAT Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>OPEN</td>
</tr>
<tr>
<td>X</td>
<td>Normal Conditions</td>
<td>OPEN</td>
</tr>
<tr>
<td>1</td>
<td>Charging</td>
<td>LOW</td>
</tr>
<tr>
<td>X</td>
<td>Fault (Charging or Boost)</td>
<td>128 μs Pulse, then OPEN</td>
</tr>
</tbody>
</table>

The FAULT bits (R0[2:0]) indicate the type of fault in Charge Mode (see Table 13).

Table 13. FAULT STATUS BITS DURING CHARGE MODE

<table>
<thead>
<tr>
<th>Fault Bit</th>
<th>Fault Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B2 B1 B0</td>
<td></td>
</tr>
<tr>
<td>0 0 0</td>
<td>Normal (No Fault)</td>
</tr>
<tr>
<td>0 0 1</td>
<td>VBUS OVP</td>
</tr>
<tr>
<td>0 1 0</td>
<td>Sleep Mode</td>
</tr>
<tr>
<td>0 1 1</td>
<td>Poor Input Source</td>
</tr>
<tr>
<td>1 0 0</td>
<td>Battery OVP</td>
</tr>
<tr>
<td>1 0 1</td>
<td>Thermal Shutdown</td>
</tr>
<tr>
<td>1 1 0</td>
<td>Timer Fault</td>
</tr>
<tr>
<td>1 1 1</td>
<td>No Battery</td>
</tr>
</tbody>
</table>

Table 14. DISABLE PIN AND CE BIT FUNCTIONALITY

<table>
<thead>
<tr>
<th>Charging</th>
<th>DISABLE Pin</th>
<th>CE</th>
<th>HZ_MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENABLE</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>DISABLE</td>
<td>X</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>DISABLE</td>
<td>X</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>DISABLE</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Raising the DISABLE pin stops t32S from advancing, but does not reset it. If the DISABLE pin is raised during t15MIN charging, the t15MIN timer is reset.

Operational Mode Control

OPA_MODE (REG1[0]) and the HZ_MODE (REG1[1]) bits in conjunction with the FAULT state define the operational mode of the charger.

Table 15. OPERATION MODE CONTROL

<table>
<thead>
<tr>
<th>HZ_MODE</th>
<th>OPA_MODE</th>
<th>FAULT</th>
<th>Operation Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Charge</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>1</td>
<td>Charge Configure</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Boost</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>High Impedance</td>
</tr>
</tbody>
</table>

The IC resets the OPA_MODE bit whenever the boost is deactivated, whether due to a fault or being disabled by setting the HZ_MODE bit.

BOOST MODE

Boost Mode can be enabled if the IC is in 32–Second Mode with the OTG pin and OPA_MODE bits as indicated in Table 16. The OTG pin ACTIVE state is 1 if OTG_PL = 1 and 0 when OTG_PL = 0.

If boost is active using the OTG pin, Boost Mode is initiated even if the HZ_MODE = 1. The HZ_MODE bit overrides the OPA_MODE bit.

Table 16. ENABLING BOOST

<table>
<thead>
<tr>
<th>OTG_EN</th>
<th>OTG Pin</th>
<th>HZ_MODE</th>
<th>OPA_MODE</th>
<th>BOOST</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ACTIVE</td>
<td>X</td>
<td>X</td>
<td>Enabled</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>Enabled</td>
</tr>
<tr>
<td>X</td>
<td>ACTIVE</td>
<td>X</td>
<td>0</td>
<td>Disabled</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>1</td>
<td>X</td>
<td>Disabled</td>
</tr>
<tr>
<td>1</td>
<td>ACTIVE</td>
<td>1</td>
<td>1</td>
<td>Disabled</td>
</tr>
<tr>
<td>0</td>
<td>ACTIVE</td>
<td>0</td>
<td>0</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

To remain in Boost Mode, the TMR_RST must be set by the host before the t32S timer times out. If t32S times out in Boost Mode; the IC resets all registers, pulses the STAT pin, sets the FAULT bits to 110, and resets the BOOST bit. VBUS POR or reading R0 clears the fault condition.
Boost PWM Control

The IC uses a minimum on-time and computed minimum off-time to regulate VBUS. The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line.

During PWM Mode, the output voltage drops slightly as the input current rises. With a constant VBAT, this appears as a constant output resistance.

The "droop" caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with no undershoot from the load line. This can be seen in Figure 31 and Figure 40.

![Figure 40. Output Resistance (R_{OUT})](image)

\[ V_{OUT} = 5.07 - R_{OUT} \cdot I_{LOAD} \]  
(eq. 1)

At V_{BAT} = 3.3 V, and I_{LOAD} = 200 mA, V_{BUS} would drop to:
\[ V_{OUT} = 5.07 - 0.26 \cdot 0.2 = 5.018 \text{ V} \]  
(eq. 2)

At V_{BAT} = 2.7 V, and I_{LOAD} = 200 mA, V_{BUS} would drop to:
\[ V_{OUT} = 5.07 - 0.327 \cdot 0.2 = 5.005 \text{ V} \]  
(eq. 3)

PFM Mode

If V_{BUS} > V_{REFBOOST} (nominally 5.07 V) when the minimum off-time has ended, the regulator enters PFM Mode. Boost pulses are inhibited until V_{BUS} < V_{REFBOOST}. The minimum on-time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore the regulator behaves like a constant on-time regulator, with the bottom of its output voltage ripple at 5.07 V in PFM Mode.

Table 17. Boost PWM Operating States

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
<th>Invoked When</th>
</tr>
</thead>
<tbody>
<tr>
<td>LIN</td>
<td>Linear Startup</td>
<td>V_{BAT} &gt; V_{BUS}</td>
</tr>
<tr>
<td>SS</td>
<td>Boost Soft–Start</td>
<td>V_{BUS} &lt; V_{BST}</td>
</tr>
<tr>
<td>BST</td>
<td>Boost Operating Mode</td>
<td>V_{BAT} &gt; UVLO_{BST} and SS Completed</td>
</tr>
</tbody>
</table>

Startup

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS}, as well as reverse flow from V_{BUS} to V_{BAT}.

LIN State

When EN rises, if V_{BAT} > UVLO_{BST}, the regulator first attempts to bring PMID within 400 mV of V_{BAT} using an internal 450 mA current source from VBAT (LIN State). If PMID has not achieved V_{BAT} – 400 mV after 560 μs, a FAULT state is initiated.

SS State

When PMID > V_{BAT} – 400 mV, the boost regulator begins switching with a reduced peak current limit of about 50% of its normal current limit. The output slews up until V_{BUS} is within 5% of its setpoint; at which time, the regulation loop is closed and the current limit is set to 100%.

If the output fails to achieve 95% of its setpoint (V_{BST}) within 128 μs, the current limit is increased to 100%. If the output fails to achieve 95% of its setpoint after this second 384 μs period, a fault state is initiated.

BST State

This is the normal operating mode of the regulator. The regulator uses a minimum t_{OFF} – minimum t_{ON} modulation scheme. The minimum t_{OFF} is proportional to V_{IN} / V_{OUT}, which keeps the regulator’s switching frequency reasonably constant in CCM. t_{ON(MIN)} is proportional to V_{BAT} and is a higher value if the inductor current reached 0 before t_{OFF(MIN)} in the prior cycle.

To ensure the VBUS does not pump significantly above the regulation point, the boost switch remains off as long as FB > V_{REF}.

Boost Faults

If a BOOST fault occurs:
1. The STAT pin pulses.
2. OPA_MODE bit is reset.
3. The power stage is in High–Impedance Mode.
4. The FAULT bits (REG0[2:0]) are set per Table 18.
Restart After Boost Faults

If boost was enabled with the OPA_MODE bit and OTG_EN = 0, Boost Mode can only be enabled through subsequent I²C commands since OPA_MODE is reset on boost faults. If OTG_EN = 1 and the OTG pin is still ACTIVE (see Table 16), the boost restarts after a 5.2 ms delay, as shown in Figure 41. If the fault condition persists, restart is attempted every 5 ms until the fault clears or an I²C command disables the boost.

Table 18. FAULT BITS DURING BOOST MODE

<table>
<thead>
<tr>
<th>Fault Bit</th>
<th>Fault Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>Normal (no fault)</td>
</tr>
<tr>
<td>0 0 1</td>
<td>VBUS &gt; VBUSOVP</td>
</tr>
<tr>
<td>0 1 0</td>
<td>VBUS fails to achieve the voltage required to advance to the next state during soft-start or sustained (&gt;50 μs) current limit during the BST state.</td>
</tr>
<tr>
<td>0 1 1</td>
<td>VBAT &lt; UVLOBST</td>
</tr>
<tr>
<td>1 0 0</td>
<td>N/A: This code does not appear.</td>
</tr>
<tr>
<td>1 0 1</td>
<td>Thermal shutdown</td>
</tr>
<tr>
<td>1 1 0</td>
<td>Timer fault; all registers reset.</td>
</tr>
<tr>
<td>1 1 1</td>
<td>N/A: This code does not appear.</td>
</tr>
</tbody>
</table>

VREG Pin

The 1.8 V regulated output on this pin can be disabled through I²C by setting the DIS_VREG bit (REG5[6]). VREG can supply up to 2 mA. This circuit, which is powered from PMID, is enabled only when PMID > VBAT and does not drain current from the battery. During boost, VREG is off. It is also off when the HZ_MODE bit (REG1[1]) = 1.

Monitor Register (Reg10H)

Additional status monitoring bits enable the host processor to have more visibility into the status of the IC. The monitor bits are real-time status indicators and are not internally debounced or otherwise time qualified.

The state of the MONITOR register bits listed in High-Impedance Mode is only valid when VBUS is valid.

Table 19. MONITOR REGISTER BIT DEFINITIONS

<table>
<thead>
<tr>
<th>BIT#</th>
<th>NAME</th>
<th>STATE</th>
<th>Active When</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>MONITOR Address 10H</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>ITERM_CMP</td>
<td>VCSIN − VBAT &lt; VITERM</td>
<td>VCSIN − VBAT &gt; VITERM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VCSIN − VBAT &lt; 1 mV</td>
<td>VCSIN − VBAT &gt; 1 mV</td>
</tr>
<tr>
<td>6</td>
<td>VBAT_CMP</td>
<td>VBAT &lt; VSHORT</td>
<td>VBAT &gt; VSHORT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VBAT &lt; VLOWV</td>
<td>VBAT &gt; VLOWV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VBAT &lt; UVLOBST</td>
<td>VBAT &gt; UVLOBST</td>
</tr>
<tr>
<td>5</td>
<td>LINCHG</td>
<td>Linear Charging Not Enabled</td>
<td>Linear Charging Enabled</td>
</tr>
<tr>
<td>4</td>
<td>T_120</td>
<td>T_J &lt; 120°C</td>
<td>T_J &gt; 120°C</td>
</tr>
<tr>
<td>3</td>
<td>ICHG</td>
<td>Charging Current Controlled by ICHARGE Control Loop</td>
<td>Charging Current Not Controlled by ICHARGE Control Loop</td>
</tr>
<tr>
<td>2</td>
<td>IBUS</td>
<td>IBUS Limiting Charging Current</td>
<td>Charge Current Not Limited by IBUS</td>
</tr>
<tr>
<td>1</td>
<td>VBUS_VALID</td>
<td>VBUS Not Valid</td>
<td>VBUS is Valid</td>
</tr>
<tr>
<td>0</td>
<td>CV</td>
<td>Constant Current Charging</td>
<td>Constant Voltage Charging</td>
</tr>
</tbody>
</table>
I²C INTERFACE

The FAN54015’s serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Mode I²C-Bus specifications. The SCL line is an input and the SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 20. I²C SLAVE ADDRESS BYTE

<table>
<thead>
<tr>
<th>Part Type</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN54015</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
<td>R/W</td>
</tr>
</tbody>
</table>

In hex notation, the slave address assumes a 0 LSB. The hex slave address for the FAN54015 is D4H and is D6H for all other parts in the family.

Bus Timing

As shown in Figure 42, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the

![Figure 42. Data Transfer Timing](image)

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 43.

![Figure 43. Start Bit](image)

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 44.

![Figure 44. Stop Bit](image)

During a read from the FAN54015 (Figure 46, Figure 47), the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1–to–0 transition on SDA while SCL is HIGH, as shown in Figure 45.

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master then generates a repeated start condition (Figure 45) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit (Figure 44) is sent by the master. While in HS Mode, packets are separated by repeated start conditions (Figure 45).

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 21. BIT DEFINITIONS FOR FIGURE 46, FIGURE 47, AND FIGURE 48

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>START, see Figure 43</td>
</tr>
<tr>
<td>A</td>
<td>ACK. The slave drives SDA to 0 to acknowledge the preceding packet.</td>
</tr>
<tr>
<td>Å</td>
<td>NACK. The slave sends a 1 to NACK the preceding packet.</td>
</tr>
<tr>
<td>R</td>
<td>Repeated START, see Figure 45</td>
</tr>
<tr>
<td>P</td>
<td>STOP, see Figure 44, Figure 44</td>
</tr>
</tbody>
</table>
REGcER DESCrIPTIONS

The nine FAN54015 user–accessible registers are defined in Table 22.

Table 22. I²C REGISTER ADDRESS

<table>
<thead>
<tr>
<th>Register</th>
<th>Name</th>
<th>REG#</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CONTROL0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CONTROL1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>OREG</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>IC_INFO</td>
<td>03 or 3BH</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>IBAT</td>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SP_CHARGER</td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SAFETY</td>
<td>6</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MONITOR</td>
<td>10h</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 23. REGISTER BIT DEFINITIONS

(This table defines the operation of each register bit for all IC versions. Default values are in bold text.)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Value</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>CONTROL0 Register Address: 00</td>
<td>Default Value = X1XX 0XXX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>TMR_RST OTG</td>
<td>1</td>
<td>W</td>
<td>Writing a 1 resets the f32S timer; writing a 0 has no effect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>R</td>
<td>Returns the OTG pin level (1 = HIGH)</td>
</tr>
<tr>
<td>6</td>
<td>EN_STAT</td>
<td>0</td>
<td>R/W</td>
<td>Prevents STAT pin from going LOW during charging; STAT pin still pulses to enunciate faults</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>Enables STAT pin LOW when IC is charging</td>
<td></td>
</tr>
<tr>
<td>5:4</td>
<td>STAT</td>
<td>00</td>
<td>R</td>
<td>Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td>Charge in progress</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>Charge done</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>Fault</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>BOOST</td>
<td>0</td>
<td>R</td>
<td>IC is not in Boost Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>IC is in Boost Mode</td>
<td></td>
</tr>
<tr>
<td>2:0</td>
<td>FAULT</td>
<td>R</td>
<td>Fault status bits: for Charge Mode, see Table 13; for Boost Mode, see Table 18</td>
<td></td>
</tr>
<tr>
<td>CONTROL1 Register Address: 01</td>
<td>Default Value = 0011 0000 (30h)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:6</td>
<td>IINLIM</td>
<td>R/W</td>
<td>Input current limit, see Table 7</td>
<td></td>
</tr>
<tr>
<td>5:4</td>
<td>VLOWV</td>
<td>R/W</td>
<td>3.4 V</td>
<td>Weak battery voltage threshold</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00</td>
<td>3.4 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01</td>
<td>3.5 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>3.6 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11</td>
<td>3.7 V</td>
</tr>
</tbody>
</table>
Table 23. REGISTER BIT DEFINITIONS
(This table defines the operation of each register bit for all IC versions. Default values are in **bold** text.) (continued)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>CONTROL1</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>TE</td>
<td>0</td>
<td>R/W</td>
<td>Disable charge current termination</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>Enable charge current termination</td>
</tr>
<tr>
<td>2</td>
<td>CE</td>
<td>0</td>
<td>R/W</td>
<td>Charger enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>Charger disabled</td>
</tr>
<tr>
<td>1</td>
<td>HZ_MODE</td>
<td>0</td>
<td>R/W</td>
<td>Not High–Impedance Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>High–Impedance Mode</td>
</tr>
<tr>
<td>0</td>
<td>OPA_MODE</td>
<td>0</td>
<td>R/W</td>
<td>Charge Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>Boost Mode</td>
</tr>
<tr>
<td></td>
<td><strong>OREG</strong></td>
<td></td>
<td>R/W</td>
<td></td>
</tr>
<tr>
<td>7:2</td>
<td>OREG</td>
<td></td>
<td></td>
<td>Charge output “float” voltage; programmable from 3.5 to 4.44V in 20mV increments; defaults to 000010 (3.54 V), see Table 3</td>
</tr>
<tr>
<td>1</td>
<td>OTG_PL</td>
<td>0</td>
<td>R/W</td>
<td>OTG pin active LOW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>OTG pin active HIGH</td>
</tr>
<tr>
<td>0</td>
<td>OTG_EN</td>
<td>0</td>
<td>R/W</td>
<td>Enables OTG pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>Disables OTG pin</td>
</tr>
<tr>
<td></td>
<td><strong>IC_INFO</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:5</td>
<td>Vendor Code</td>
<td>100</td>
<td>R</td>
<td>Identifies ON Semiconductor as the IC supplier</td>
</tr>
<tr>
<td>4:2</td>
<td>PN</td>
<td></td>
<td>R</td>
<td>Part number bits, see the Ordering Info on page 31</td>
</tr>
<tr>
<td>1:0</td>
<td>REV</td>
<td>00</td>
<td>R</td>
<td>IC Revision, revision 1.X, where X is the decimal of these three bits</td>
</tr>
<tr>
<td></td>
<td><strong>IBAT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RESET</td>
<td>1</td>
<td>W</td>
<td>Writing a 1 resets charge parameters, except the Safety register (Reg6), to their defaults: writing a 0 has no effect; read returns 1</td>
</tr>
<tr>
<td>6:4</td>
<td>IOCHARGE</td>
<td>Table 5</td>
<td>R/W</td>
<td>Programs the maximum charge current, see Table 5</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>1</td>
<td>R</td>
<td>Unused</td>
</tr>
<tr>
<td>2:0</td>
<td>ITERM</td>
<td>Table 6</td>
<td>R/W</td>
<td>Sets the current used for charging termination, see Table 6</td>
</tr>
<tr>
<td></td>
<td><strong>SP_CHARGER</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>0</td>
<td>R</td>
<td>Unused</td>
</tr>
<tr>
<td>6</td>
<td>DIS_VREG</td>
<td>0</td>
<td>R/W</td>
<td>1.8 V regulator is ON</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>1.8 V regulator is OFF</td>
</tr>
<tr>
<td>5</td>
<td>IO_LEVEL</td>
<td>0</td>
<td>R/W</td>
<td>Output current is controlled by IOCHARGE bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>Voltage across $R_{SENSE}$ for output current control is set to 34 mV (500 mA for $R_{SENSE} = 68 , \mu\Omega$ and 340 mA for 100 $\mu\Omega$)</td>
</tr>
<tr>
<td>4</td>
<td>SP</td>
<td>0</td>
<td>R</td>
<td>Special charger is not active ($V_{BUS}$ is able to stay above $V_{SP}$)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>Special charger has been detected and $V_{BUS}$ is being regulated to $V_{SP}$</td>
</tr>
<tr>
<td>3</td>
<td>EN_LEVEL</td>
<td>0</td>
<td>R</td>
<td>DISABLE pin is LOW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td>DISABLE pin is HIGH</td>
</tr>
<tr>
<td>2:0</td>
<td>VSP</td>
<td>Table 8</td>
<td>R/W</td>
<td>Special charger input regulation voltage, see Table 8</td>
</tr>
<tr>
<td></td>
<td><strong>SAFETY</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>0</td>
<td>R</td>
<td>Bit disabled and always returns 0 when read back</td>
</tr>
<tr>
<td>6:4</td>
<td>ISAFE</td>
<td>Table 9</td>
<td>R/W</td>
<td>Sets the maximum I_{IOCHARGE} value used by the control circuit, see Table 9</td>
</tr>
<tr>
<td>3:0</td>
<td>VSAFE</td>
<td>Table 10</td>
<td>R/W</td>
<td>Sets the maximum VOREG used by the control circuit, see Table 10</td>
</tr>
</tbody>
</table>

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Table 23. REGISTER BIT DEFINITIONS (This table defines the operation of each register bit for all IC versions. Default values are in **bold** text.) (continued)

<table>
<thead>
<tr>
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<th>Name</th>
<th>Value</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ITERM_CMP</td>
<td>See Table 19</td>
<td>R</td>
<td>ITERM comparator output, 1 when VRSENSE &gt; ITERM reference</td>
</tr>
<tr>
<td>6</td>
<td>VBAT_CMP</td>
<td>See Table 19</td>
<td>R</td>
<td>Output of VBAT comparator</td>
</tr>
<tr>
<td>5</td>
<td>LINCHG</td>
<td>R</td>
<td></td>
<td>30 mA linear charger ON</td>
</tr>
<tr>
<td>4</td>
<td>T_120</td>
<td>R</td>
<td></td>
<td>Thermal regulation comparator; when 1 and T_145 = 0, the charge current is limited to 22.1 mV across RSENSE</td>
</tr>
<tr>
<td>3</td>
<td>ICHG</td>
<td>R</td>
<td></td>
<td>0 indicates the ICHARGE loop is controlling the battery charge current</td>
</tr>
<tr>
<td>2</td>
<td>IBUS</td>
<td>R</td>
<td></td>
<td>0 indicates the IBUS (input current) loop is controlling the battery charge current</td>
</tr>
<tr>
<td>1</td>
<td>VBUS_VALID</td>
<td>R</td>
<td></td>
<td>1 indicates VBUS has passed validation and is capable of charging</td>
</tr>
<tr>
<td>0</td>
<td>CV</td>
<td>R</td>
<td></td>
<td>1 indicates the constant–voltage loop (OREG) is controlling the charger and all current limiting loops have released</td>
</tr>
</tbody>
</table>

**PCB LAYOUT RECOMMENDATIONS**

Bypass capacitors should be placed as close to the IC as possible. In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins. All power and ground pins must be routed to their bypass capacitors, using top copper whenever possible. Copper area connecting to the IC should be maximized to improve thermal performance if possible.
## ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Temperature Range</th>
<th>Package</th>
<th>PN Bits: IC_INFO[4:2]</th>
<th>Shipping¹</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN54015UCX</td>
<td>−40 to 85°C</td>
<td>20–Bump, Wafer–Level Chip–Scale Package (WLCSP), 0.4 mm Pitch, Estimated Size: 1.96 x 1.87 mm (Pb–Free)</td>
<td>101</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>FAN54015BUCX (Note 8)</td>
<td></td>
<td></td>
<td></td>
<td>3000 / Tape &amp; Reel</td>
</tr>
</tbody>
</table>

¹For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
8. FAN54015BUCX includes backside lamination.

ON Semiconductor is licensed by the Philips Corporation to carry the I²C bus protocol.
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

WLCSP20 1.96x1.87x0.586
CASE 567SL
ISSUE O

DATE 30 NOV 2016

NOTES:
A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE
D. DATUM C IS DEFINED BY THE SPHERICAL
CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS
±39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE
PRODUCT DATASHEET.