

# FAN53763

## 1.5 A Synchronous Buck Regulator

### Description

The FAN53763 is a Super Low Iq, step-down switching voltage regulator, that delivers a fixed output from an input voltage supply of 2.3 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53763 is capable of delivering a peak efficiency of 93%, while maintaining efficiency over 90% at load currents as low as 1 mA.

The regulator operates with 0402 and 0603 input and output capacitors, respectively, which reduces the total solution size to 5.5 mm<sup>2</sup>. At moderate and light load, Pulse Frequency Modulation (PFM) is used to operate the device with a low quiescent current. Even with such a low quiescent current, the part exhibits excellent transient response during load swings. In Shutdown Mode, the supply current drops to 100 nA, reducing power consumption. The Mode pin allows the part to be in a Super Low IQ (SLIQ) mode with a typical quiescent current of 2  $\mu$ A.

The FAN53763 is available in 6-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

### Features

- 2  $\mu$ A Typical Quiescent Current
- 5.5 mm<sup>2</sup> Total Solution Size
- 1.5 A Output Current Capability
- 0.6 V to 1.8 V Fixed Output Voltage
- 2.3 V to 5.5 V Input Voltage Range
- Best-in-Class Load Transient Response
- Best-in-Class Efficiency with Sub 1 mA Output Currents
- Internal Soft-Start Limits Battery Current Below 150 mA to Avoid Brown-out Scenarios
- Protection Faults (UVLO, OCP and OTP)
- Thermal Shutdown and Overload Protection
- 6-Bump WLCSP, 0.4 mm Pitch
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Wearables
- Smart Watch
- Health Monitoring
- Sensor Drive
- Energy Harvesting
- Utility and Safety Modules
- RF Modules



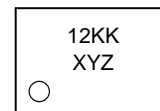
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



WLCSP6  
CASE 567UH

### MARKING DIAGRAM



12	= Alphanumeric Device Code
KK	= Lot Run Code
X	= Alphabetical Year Code
Y	= 2-weeks Date Code
Z	= Assembly Plant Code

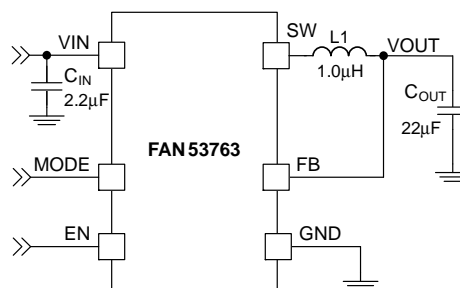


Figure 1. Typical Application

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FAN53763

**Table 1. ORDERING INFORMATION**

Part Number	Output Voltage (Note 1)	Max. Output Current (Note 1)	Temperature Range	Package	Packing Method	Device Marking
FAN53763UC24X	1.8 V	1.5 A	-40 to 85°C	WLCSP	Tape & Reel	GP

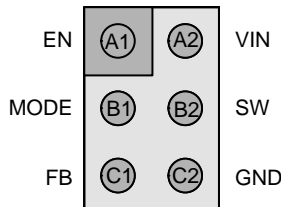
1. Other voltage and output current options are available. Contact an On Semiconductor representative

**Table 2. RECOMMENDED EXTERNAL COMPONENTS**

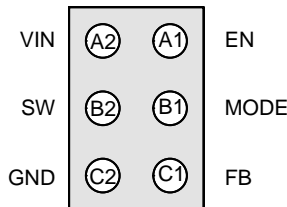
Component	Description	Vendor	Parameter	Typ	Unit
L	1.0 $\mu$ H, 20%, 2.3 A, 107 m $\Omega$ , 1608	DFE160810S-1R0M (Murata)	L	1.0	$\mu$ H
C <sub>IN</sub>	2.2 $\mu$ F, 20%, 6.3 V, X5R, 0402	C1005X5R0J225M050BC (TDK)	C	2.2	$\mu$ F
C <sub>OUT</sub> (Note 2)	22 $\mu$ F, 20%, 6.3 V, X5R, 0603	C1608X5R0J226M080AC (TDK)	C	22	

2. A 10  $\mu$ F, 0402 capacitor can be used to reduce total solution size at the expense of load transient performance.

## Pin Configuration



**Figure 2. Top View**



**Figure 3. Bottom View**

**Table 3. PIN DEFINITIONS**

Pin #	Name	Description
A1	EN	Enable. The device is in Shutdown Mode when voltage to this pin is <0.4 V and enabled when >1.2 V. Do not leave this pin floating. Recommended for GPIO 1.8 V to drive this pin.
A2	VIN	Input Voltage. Connect to input power source across C <sub>IN</sub> .
B1	MODE	MODE. Logic "LOW" allows the IC to be in a Super Low IQ (SLIQ) state. A Logic HIGH allows the part to be in normal Iq state Auto Mode.
B2	SW	Switching Node. Connect to SW pad of inductor.
C1	FB	Feedback. Connect to positive side of output capacitor.
C2	GND	Ground. Power and IC ground. All signals are referenced to this pin.

**Table 4. ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Min	Max	Unit
V <sub>IN</sub>	Input Voltage	-0.3	6.5	V
V <sub>SW</sub>	Voltage on SW Pin	-0.3	V <sub>IN</sub> +0.3 (Note 3)	V
V <sub>CTRL</sub>	EN, FB and Mode Pin Voltage	-0.3	V <sub>IN</sub> +0.3 (Note 3)	V
ESD	Human Body Model per JESD22-A114		2.0	kV
	Charged Device Model per JESD22-C101		1.0	
T <sub>J</sub>	Junction Temperature	-40	+150	°C
T <sub>STG</sub>	Storage Temperature	-40	+150	°C
T <sub>L</sub>	Lead Soldering Temperature, 10 Seconds		+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Lesser of 6 V or V<sub>IN</sub>+0.3 V

**Table 5. RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit
$V_{IN}$	Supply Voltage Range	2.3		5.5	V
$I_{OUT}$	Output Current	0		1.5	A
$C_{IN}$	Input Capacitor		2.2		$\mu$ F
$C_{OUT}$ (Note 4)	Output Capacitor	3		100	$\mu$ F
L	Inductor	0.47	1.0	1.3	$\mu$ H
$T_A$	Operating Ambient Temperature	-40		+85	$^{\circ}$ C
$T_J$	Operating Junction Temperature	-40		+125	$^{\circ}$ C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Effective capacitance after DC bias.

**Table 6. THERMAL PROPERTIES**

Symbol	Parameter	Min	Typ	Max	Unit
$\theta_{JA}$	Junction-to-Ambient Thermal Resistance (Note 5)		125		$^{\circ}$ C/W

5. Junction-to-ambient thermal resistance is a function of application and board layout. This data is simulated with four-layer 2s2p boards with vias in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed the junction temperature.

**Table 7. ELECTRICAL CHARACTERISTICS** Minimum and maximum values are at  $V_{IN} = V_{EN} = 3.6$  V,  $T_A = -40^{\circ}$ C to  $+85^{\circ}$ C, unless otherwise noted. Typical values are at  $T_A = 25^{\circ}$ C,  $V_{IN} = V_{EN} = 3.6$  V,  $V_{OUT} = 1.8$  V.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{Q,SLIQ}$	Quiescent Current	SLIQ Mode, no load, non-switching		2		$\mu$ A
$I_{Q,PFM}$	PFM Quiescent Current	PFM Mode, no load, non-switching		5		$\mu$ A
$I_{SD}$	Shutdown Supply Current	EN=GND, $V_{IN}=3.6$ V, no load		100		nA
$V_{UVLO\_RISE}$	Under-Voltage Lockout Threshold	$V_{IN}$ Rising	2.10	2.15	2.21	V
$V_{UVLO\_FALL}$		$V_{IN}$ Falling	2.00	2.05	2.10	V
$V_{IH}$	HIGH-Level Input Voltage		1.2			V
$V_{IL}$	LOW-Level Input Voltage				0.4	V
$I_{LIM}$	Peak Current Limit	$V_{IN}=4.35$ V, open-loop		2215		mA
$V_{OACC}$	Output Voltage Accuracy	$V_{OUT}=0.6$ V to 1.8V, $I_{OUT(DC)}=0$ , PWM Mode	-25		+25	mV
		$V_{OUT}=0.6$ V to 1.8V, $I_{OUT(DC)}=0$ , PFM Mode	-40		+40	mV
$R_{DS(on)}$	PMOS On Resistance	$V_{IN} = V_{GS} = 3.6$ V		135		$m\Omega$
	NMOS On Resistance	$V_{IN} = V_{GS} = 3.6$ V		95		$m\Omega$
$T_{TSD}$	Thermal Shutdown			150		$^{\circ}$ C
$T_{HYS}$	Thermal Shutdown Hysteresis			15		$^{\circ}$ C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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**Table 8. SYSTEM CHARACTERISTICS** Recommended operating conditions, unless otherwise noted,  $V_{IN} = 2.3\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ ,  $V_{OUT} = 1.8\text{ V}$ . Typical values are given at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 3.6\text{ V}$ . System characteristics are based on circuit per Figure 1.  $L = 1.0\ \mu\text{H}$ ,  $2.3\text{A}$ ,  $107\ \text{m}\Omega$  DCR, DFE160810S-1R0M (Murata),  $C_{IN} = 1 \times 2.2\ \mu\text{F}$ ,  $6.3\text{ V}$ , 0402 (1005 metric), C1005X5R0J225M050BC (TDK) and  $C_{OUT} = 1 \times 22\ \mu\text{F}$ ,  $6.3\text{ V}$ , 0603 (1608 metric), C1608X5R0J226M080AC (TDK).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LOAD <sub>REG</sub>	Load Regulation	$I_{OUT} = 10\ \mu\text{A to }1\ \text{mA}$ , SLIQ Mode		-9.0		mV/mA
		$I_{OUT} = 200\ \text{mA to }1500\ \text{mA}$ , PWM		-2.0		mV/A
LINE <sub>REG</sub>	Line Regulation	$3.0\ \text{V} \leq V_{IN} \leq 4.35\ \text{V}$ , $I_{OUT} = 300\ \text{mA}$ , PWM		-0.5		mV/V
V <sub>OUT_RIPPLE</sub>	Ripple Voltage	$I_{OUT} = 250\ \mu\text{A}$ , SLIQ Mode		40		mV
		$I_{OUT} = 20\ \text{mA}$ , PFM Mode		25		
		$I_{OUT} = 200\ \text{mA}$ , PWM Mode		5		
Eff	Efficiency	$I_{OUT} = 100\ \mu\text{A}$ , SLIQ Mode		88		%
		$I_{OUT} = 500\ \mu\text{A}$ , SLIQ Mode		91		
		$I_{OUT} = 1\ \text{mA}$ , PFM Mode		90		
		$I_{OUT} = 100\ \text{mA}$ , PFM Mode		87		
		$I_{OUT} = 300\ \text{mA}$ , PWM Mode		91		
		$I_{OUT} = 500\ \text{mA}$ , PWM Mode		90		
		$I_{OUT} = 700\ \text{mA}$ , PWM Mode		88		
$\Delta V_{OUT\_LOAD}$	Load Transient	$I_{OUT} = 10\ \text{mA} \leftrightarrow 150\ \text{mA}$ , $T_R = T_F = 1\ \mu\text{s}$ , Auto Mode		-40/+25		mV
		$I_{OUT} = 100\ \mu\text{A} \leftrightarrow 500\ \mu\text{A}$ , $T_R = T_F = 1\ \mu\text{s}$ , SLIQ Mode		$\pm 15$		mV
$\Delta V_{OUT\_LINE}$	Line Transient	$V_{IN} = 3.0\ \text{V} \leftrightarrow 3.6\ \text{V}$ , $T_R = T_F = 10\ \mu\text{s}$ , $I_{OUT} = 300\ \text{mA}$ , PWM Mode		$\pm 20$		mV

NOTE: The above system characteristics are guaranteed by design and are not performed in production testing.

Typical Characteristics

Unless otherwise specified,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode,  $T_A = 25^\circ\text{C}$ ; circuit and components according to Figure 1 and Table 2.

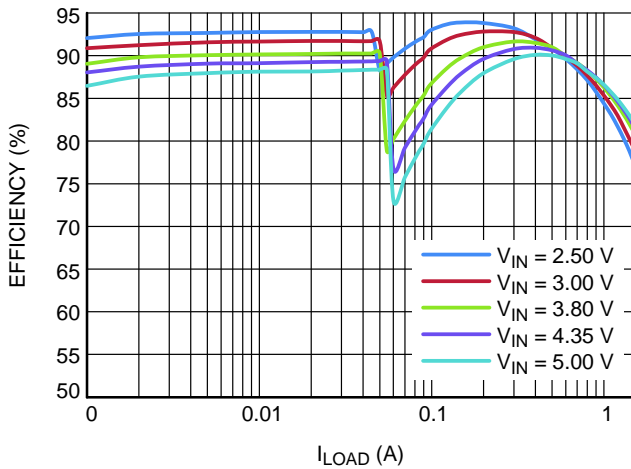


Figure 4. Efficiency vs. Load Current and Input Voltage,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode

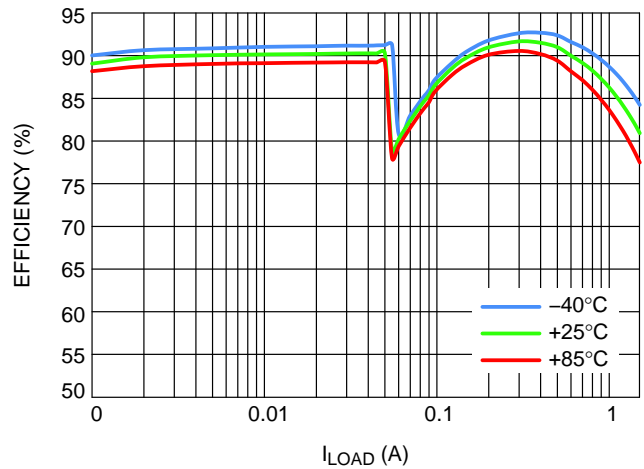


Figure 5. Efficiency vs. Load Current and Temperature,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode

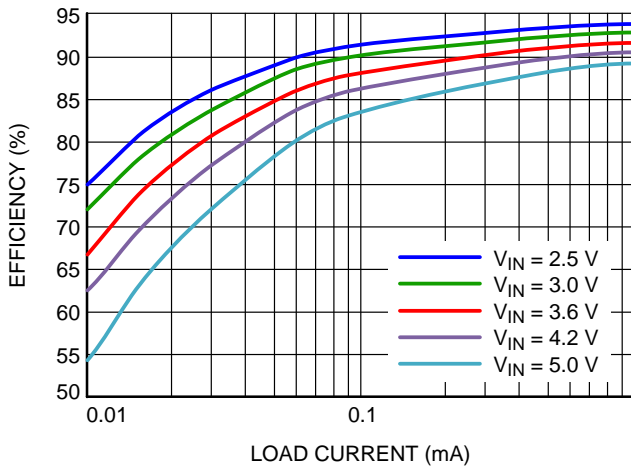


Figure 6. Efficiency vs. Load Current and Input Voltage,  $V_{OUT} = 1.8\text{ V}$ , SLIQ Mode

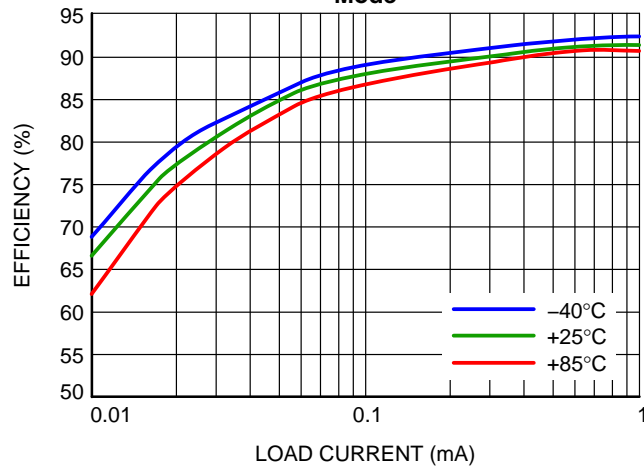


Figure 7. Efficiency vs. Load Current and Temperature,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ , SLIQ Mode

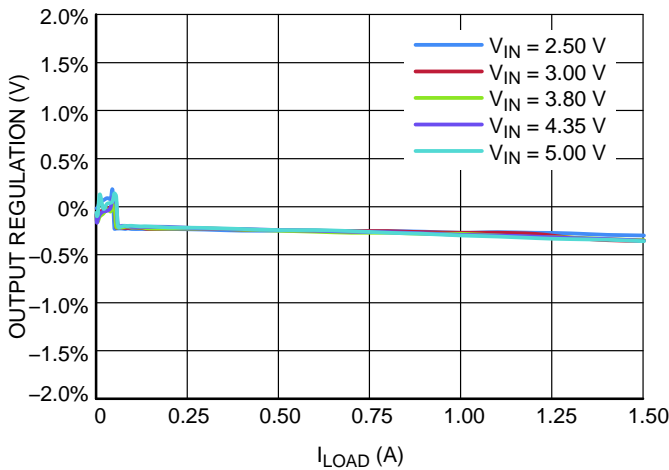


Figure 8. Output Regulation vs. Load Current and Input Voltage,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode

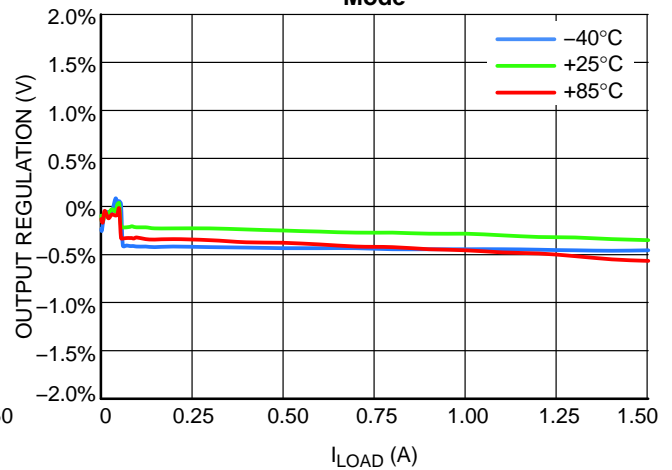


Figure 9. Output Regulation vs. Load Current and Temperature,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode

Typical Characteristics

Unless otherwise specified,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode,  $T_A = 25^\circ\text{C}$ ; circuit and components according to Figure 1 and Table 2.

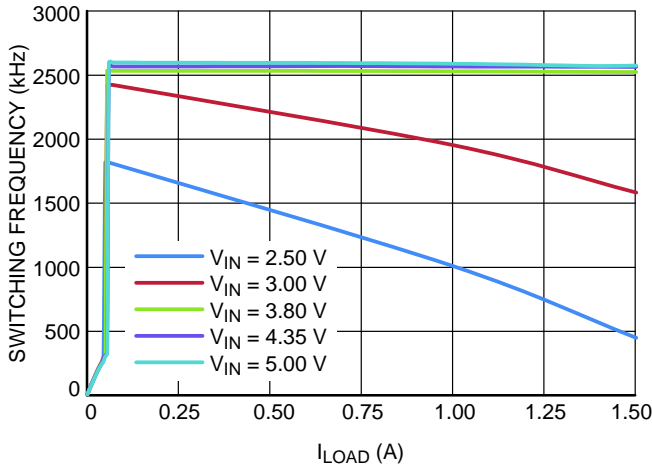


Figure 10. Frequency vs. Load Current and Input Voltage, Auto Mode,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode

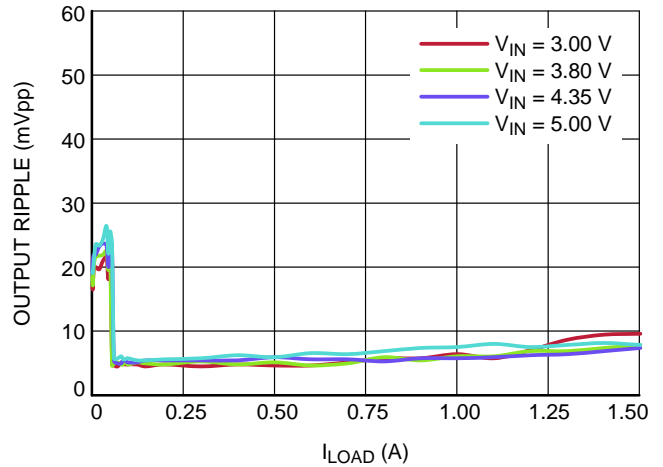


Figure 11. Output Ripple vs. Load Current and Input Voltage,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode

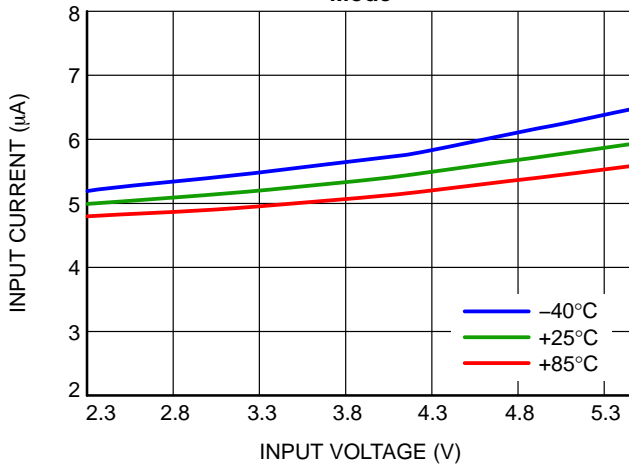


Figure 12. Quiescent Current vs. Input Voltage and Temperature,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode

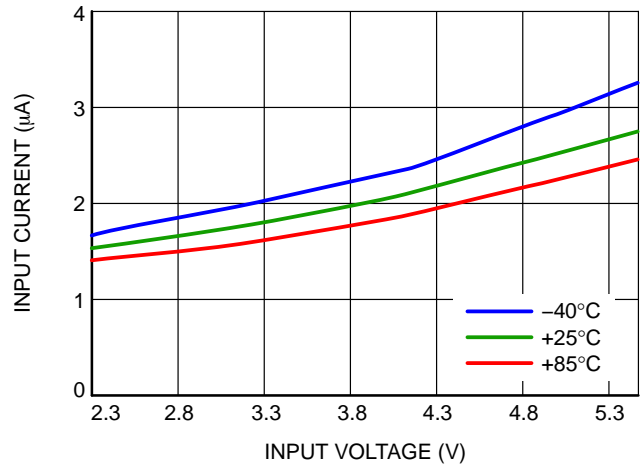


Figure 13. Quiescent Current vs. Input Voltage and Temperature,  $V_{OUT} = 1.8\text{ V}$ , SLIQ Mode

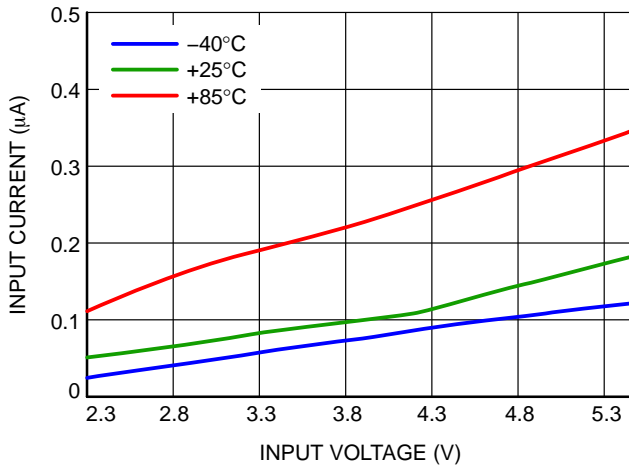


Figure 14. Shutdown Current vs. Input Voltage and Temperature

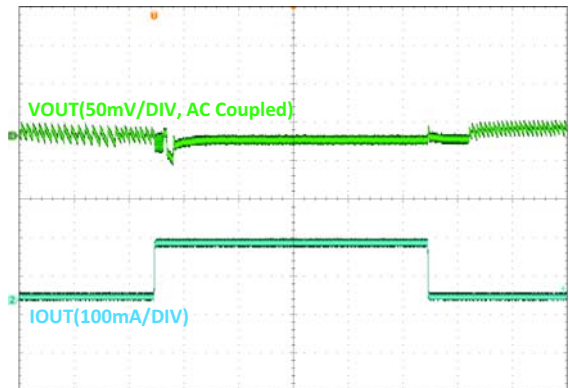


Figure 15. Load Transient,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $10\text{ mA} \Leftrightarrow 150\text{ mA}$ ,  $1\ \mu\text{s}$  Edge, Auto Mode

Typical Characteristics

Unless otherwise specified,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ , Auto Mode,  $T_A = 25^\circ\text{C}$ ; circuit and components according to Figure 1 and Table 2.

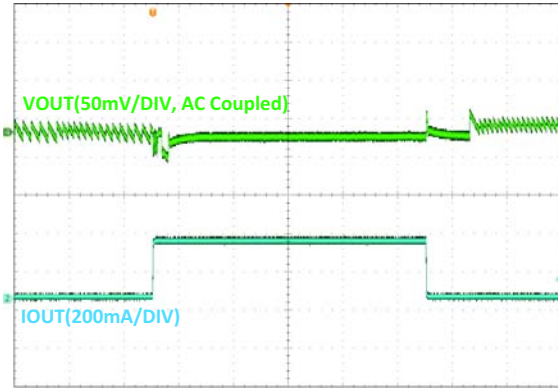


Figure 16. Load Transient,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $5\text{ mA} \leftrightarrow 300\text{ mA}$ ,  $1\ \mu\text{s}$  Edge, Auto Mode

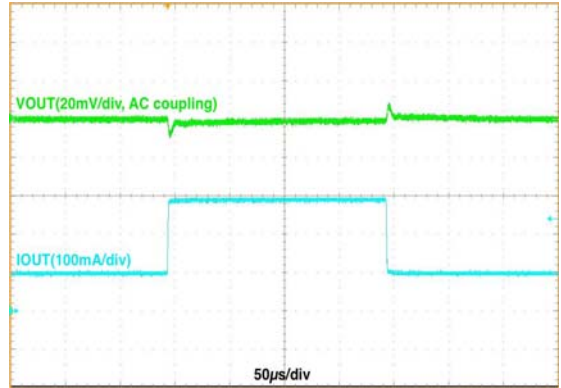


Figure 17. Load Transient,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $100\text{ mA} \leftrightarrow 300\text{ mA}$ ,  $1\ \mu\text{s}$  Edge, Auto Mode

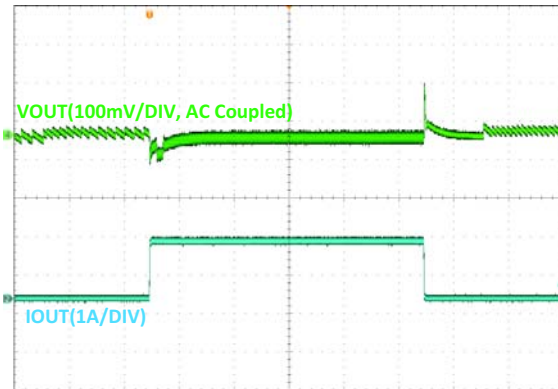


Figure 18. Load Transient,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $10\text{ mA} \leftrightarrow 1500\text{ mA}$ ,  $1\ \mu\text{s}$  Edge, Auto Mode

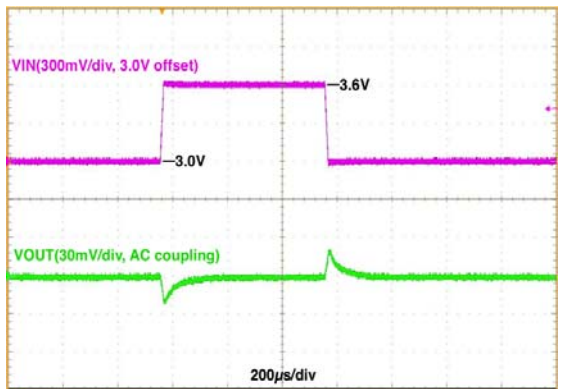


Figure 19. Line Transient,  $V_{IN} = 3.0\text{ V} \leftrightarrow 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $10\ \mu\text{s}$  Edge,  $300\text{ mA}$  Load, Auto Mode

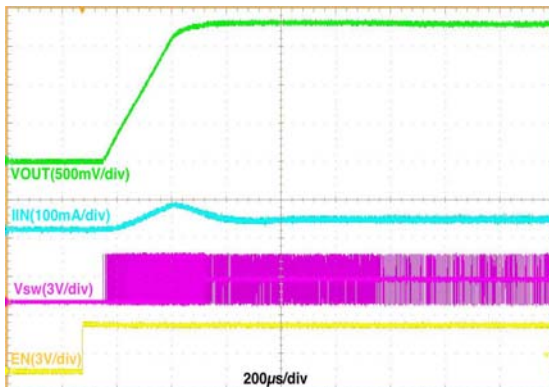


Figure 20. Start-up,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $50\text{ mA}$  Resistive Load, Auto Mode

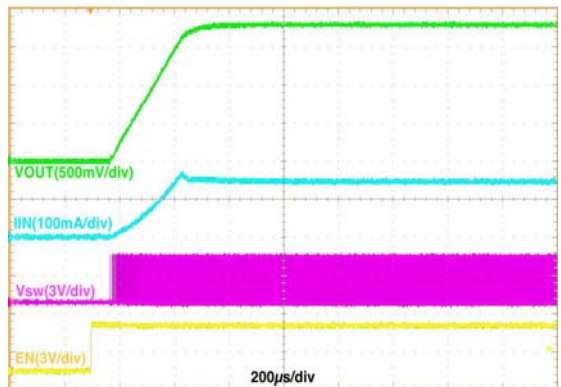


Figure 21. Start-up,  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V}$ ,  $300\text{ mA}$  Resistive Load, Auto Mode

## Operation Description

The FAN53763 is a Super Low Iq (SLIQ), step-down switching voltage regulator, typically operating at 2.5 Mhz in Continuous Conduction Mode(CCM). Using a proprietary architecture with synchronous rectification, the FAN53763 is capable of delivering a peak efficiency of 93%, while maintaining efficiency over 90% at load currents sub 1 mA.

In SLIQ mode the device is very efficient with load currents in the  $\mu\text{A}$  range. In SLIQ mode the device draws less than 2  $\mu\text{A}$  typical from the battery with no load. The load transients in SLIQ mode are best in class.

The FAN53763 provides a fixed output voltage of 0.6 V to 1.8 V and load capability of 1.5 A, which can support wearable or mobile phone applications which Li-Ion batteries. Specialized soft-start limits the battery current to 150 mA to limit any brown out occurrences.

## Control Scheme

### Enable and Disable

When EN pin is Low, all circuits are off and the IC draws 100 nA current. When EN is High and  $V_{\text{IN}}$  is above its UVLO threshold, the regulator begins a soft-start cycle. The FAN53763 has internal soft-start which limits the battery current draw to 150 mA. Once the part reaches 95% of  $V_{\text{OUT}}$  target, the part will transition to the correct mode of operation depending on load current. The part starts up within 400  $\mu\text{s}$  typical with the recommended external components listed in Table 1.

### MODE Pin

Setting Mode Pin Low sets the device in SLIQ mode; setting Mode Pin High sets the device in normal Iq Auto Mode.

## Protection Features

### VOUT Fault

If the  $V_{\text{OUT}}$  fails to reach 95% of  $V_{\text{OUT}}$  target within 1.8 ms during startup, a VOUT fault is declared. During the fault condition the part restarts every 20 ms to achieve the 95% target voltage. Once the output voltage reaches the 95%  $V_{\text{OUT}}$  target voltage within 1.8 ms, the VOUT fault clears.

### Over-Current Protection (OCP)

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching this point, the high-side switch turns off, preventing high

currents from causing damage. The regulator continues to limit the current cycle-by-cycle. After 500  $\mu\text{s}$  of current limit, the regulator triggers an over-current fault, causing the regulator to shut down for about 20ms before attempting a restart.

### Under-Voltage Lockout (UVLO)

When EN is HIGH, the under-voltage lockout keeps the part from operating until the input supply voltage rises high enough to properly operate. This ensures no misbehavior of the regulator during startup or shutdown.

### Over-Temperature Protection (OTP)

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 15°C hysteresis. Once the junction temperature falls below the hysteresis threshold, the regulator performs a soft-start.

## Modes of Operations

### SLIQ (Super Low Iq)

In SLIQ Mode the device acts in a modified PFM mode with a super low Iq state. The part draws 2  $\mu\text{A}$  with no load.

The part enters SLIQ Mode when the Mode pin is set to logic "LOW". Before pulling the Mode Pin Low, the load current should drop below 1 mA to maintain output voltage regulation in SLIQ mode. The maximum load current in SLIQ Mode that the device can support is 1 mA. If load current exceeds 1 mA, it is recommended to place part in Auto Mode by pulling Mode pin High so that the device can support more current.

The part can support more than 1mA in SLIQ Mode if the output capacitor is increased.

### PFM

At light load operation in Auto Mode, the device enters PFM mode when load current is below 20 mA typically. PFM mode reduces switching frequency as well as battery current draw, which yields high efficiency.

When Mode pin goes High, the part will transition from SLIQ Mode into normal PFM mode within 10  $\mu\text{s}$  typically.

### PWM

When load is high, the part transitions smoothly from PFM mode to PWM mode. The part enters PWM mode when load current exceeds 50 mA typically.



**Applications Information**

**Selecting the Inductor**

The output inductor must meet both the required inductance and the energy-handling capability of the application. The inductor value affects average current limit, output voltage ripple, and efficiency.

The ripple current ( $\Delta I$ ) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left( \frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \right) \quad (\text{eq. 1})$$

The maximum average load current,  $I_{MAX(Load)}$ , is related to the peak current limit,  $I_{LIM(PK)}$ , by the ripple current, given by:

$$I_{MAX(Load)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad (\text{eq. 2})$$

The transition between PFM and PWM operation is determined by the point at which the inductor valley current crosses zero. The regulator DC current when the inductor current crosses zero,  $I_{DCM}$ , is:

$$I_{DCM} = \frac{\Delta I}{2} \quad (\text{eq. 3})$$

The FAN53763 is optimized for operation with  $L = 1.0 \mu H$ , but is stable with inductances up to 1.3 H (nominal). The inductor should be rated to maintain at least 80% of its value at  $I_{LIM(PK)}$ .

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but because  $\Delta I$  increases, the RMS current increases, as do the core and skin effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^2 + \frac{\Delta I^2}{12}} \quad (\text{eq. 4})$$

The increased RMS current produces higher losses through the  $R_{DS(ON)}$  of the IC MOSFETs, as well as the inductor DCR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given

physical inductor size, increased inductance usually results in an inductor with lower saturation current and higher DCR.

Table 9 shows the effects of inductance higher or lower than the recommended 1.0  $\mu H$  on regulator performance.

**Output Capacitor**

Increasing  $C_{OUT}$  has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Vice versa, lower  $C_{OUT}$  can be used but with a compromise of load transient response. Output voltage ripple,  $\Delta V_{OUT}$ , is:

$$\Delta V_{OUT} = \Delta I_L \left[ \frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}} \right] \quad (\text{eq. 5})$$

**Input Capacitor**

The 2.2  $\mu F$  ceramic input capacitor should be placed as close as possible between the VIN pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed between  $C_{IN}$  and the power source lead to reduce the ringing that can occur between the inductance of the power source leads and  $C_{IN}$ .

The effective capacitance value decreases as  $V_{IN}$  increases due to DC bias effects.

**PCB Layout Guidelines**

1. The input capacitor ( $C_{IN}$ ) should be connected as close as possible to the VIN and GND pins. Connect to VIN and GND using only top metal. Do not route through vias (*see Figure 27.*)
2. Place the inductor (L) as close as possible to the IC. Use short wide traces for the main current paths.
3. An output capacitor ( $C_{OUT}$ ) should be placed as close as possible to the IC. Connection to GND should only be on top metal. Feedback signal connection to VOUT should be routed away from noisy components and traces (e.g. SW line).

**Table 9. EFFECTS OF CHANGES in Inductor Value (from 1.0  $\mu H$  Recommended Value) on Regulator Performance**

Inductor Value	$I_{MAX(Load)}$	$\Delta V_{OUT}$	Transient Response
Increase	Increase	Decrease	Degraded
Decrease	Decrease	Increase	Improved

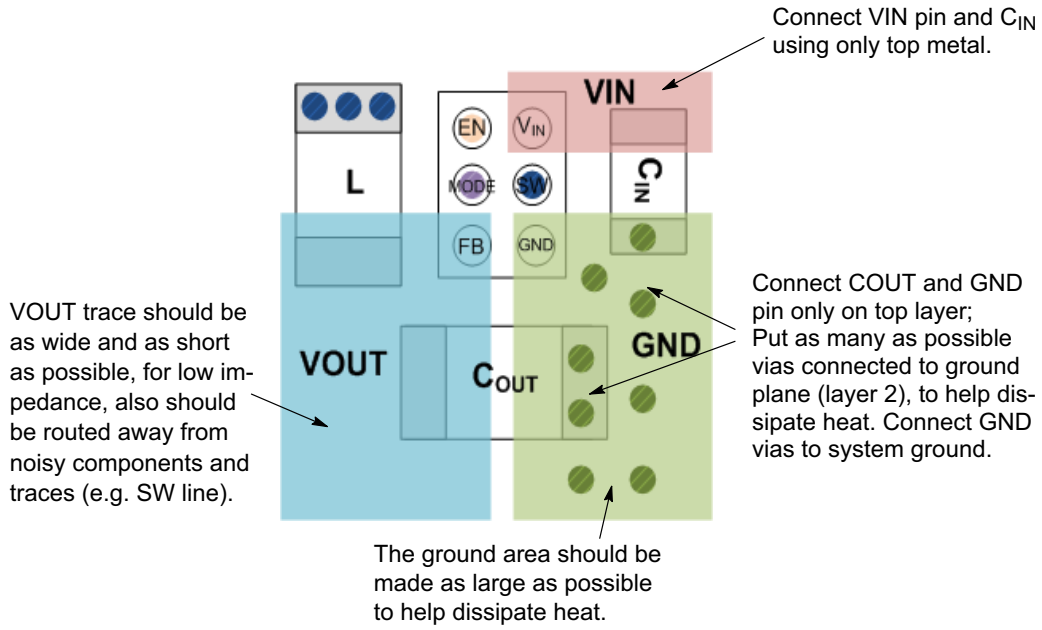
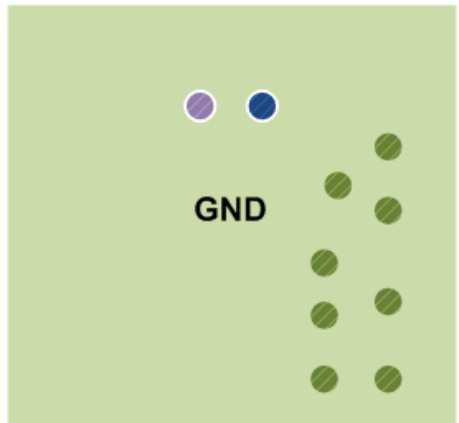
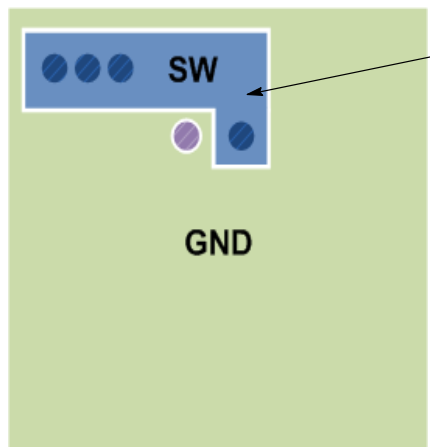


Figure 22. Top Layer



Layer 2 should be a solid ground layer, to shield VOUT from capacitive coupling of the fast edges of SW node. Logic signals can be routed on this layer.

Figure 23. Layer 1

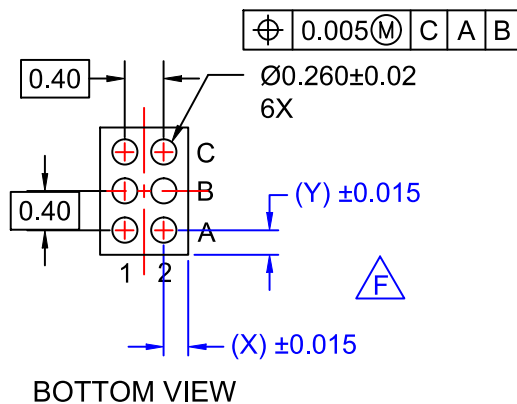
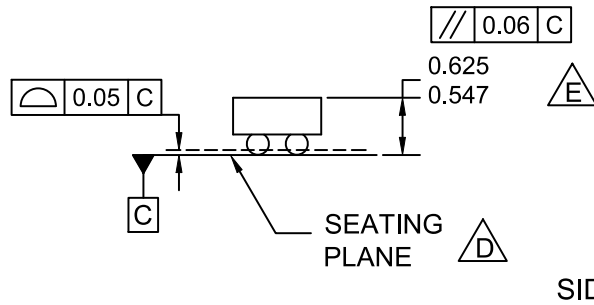
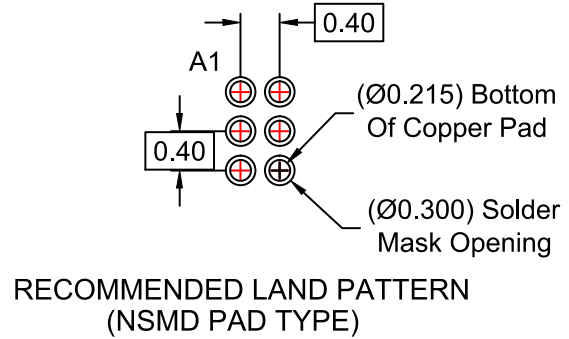
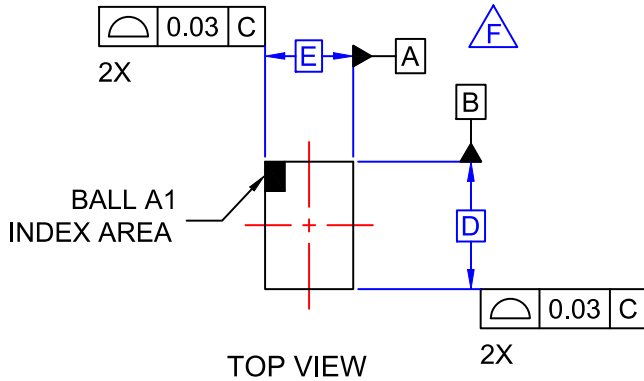


SW trace should be as wide and as short as possible, and be isolated with GND area from any other sensitive traces.

Figure 24. Layer 3

**WLCSP6 1.38x0.94x0.625**  
CASE 567UH  
ISSUE O

DATE 31 APR 2017



**NOTES**

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 586 ± 39 MICRONS (547-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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