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October 2013

FAN2012

1.5 A Low-Voltage, Current-Mode Synchronous PWM Buck Regulator

Features

- 95% Efficiency, Synchronous Operation
- Adjustable Output Voltage from 0.8 V to 3.5 V
- 4.5 V to 5.5 V Input Voltage Range
- Up to 1.5 A Output Current
- Fixed-Frequency 1.3 MHz PWM Operation
- Soft Start
- Excellent Load Transient Response
- 3 x 3 mm, 6-Lead, MLP

Applications

- Hard Disk F
- Set-T n E
- Point-o oad on d
 - Note ok amputer
- Comr unications Equipment

Description

The FAN2C12 is a refficiency, low-noise, synchror us also V the violulated (PWM) current-mode DC onvioler designs a for low-voltage applicants. It places up to 1.5 A continuous-load are true. 4.5 V to 5.5 V input. The output voltage is adjulable over a wide range in 0.8 V to 3.5 V by me is an external voltage divitor.

The FAN2012 has an "Finalle Input" and the device can be put in shutdown mode, in which the ground current falls below 1 µA.

A current-mode control loop with a fast transient response ensurer excellent line and load regulation. The fixed 1.3 MHz switching frequency enables designers to choose a small, inexpensive external inductor and capacitor. Filtering is easily accomplished with vory small components.

Protection features include input under-voltage lockout, short-circuit protection, and thermal shutdown. Soft-start limits inrush current during start-up conditions.

The device is available in a 3x3 mm 6-lead molded leadless package (MLP), making it possible to build a 1.5 A complete DC-DC converter in limited space on the printed circuit board (PCB).

Ordering Information

Part Number	Output Voltage	Operating Temperature Range	Package
FAN2012MPX	Adjustable	0°C to 85°C	3x3 mm 6-Lead MLP
FAN2012EMPX	Adjustable	-40°C to 85°C	3x3 mm 6-Lead MLP

Typical Application

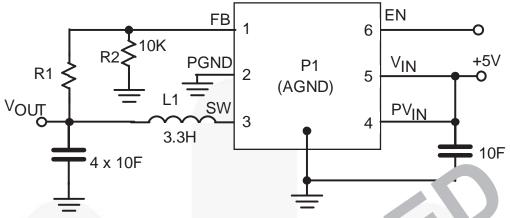


Figure 1. Typical Application

Pin Configuration

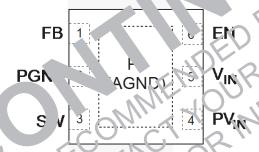


Figure 2. Pin Assignments

r in D∈ 'ni ons

Pi. 4	Name	Description			
P1	ACIND	Analog Ground. P1 must be soldered to the PCB ground.			
1	FB	Feedback Input. Adjustable voltage option; connect this pin to the resistor divider.			
5	PGND	ov er Cround. This pin is connected to the internal MOSFET switches. This pin must be charmally connected to AGND.			
3	SW	Switching Node. This pin is connected to the internal MOSFET switches.			
4	PVIN	Supply Voltage Input. This pin is connected to the internal MOSFET switches.			
5	VIN	Supply Voltage Input.			
6	EN	Enable Input. Logic HIGH enables the chip and logic LOW disables the chip, reducing the supply current to less than 1 μA. Do not float this pin.			

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Input Voltage		-0.3	6.5	V
V _{IN}	Input Voltage on PVIN and Any Other Pin		-0.3	V _{IN}	V
θ_{JC}	Thermal Resistance-Junction to Tab ⁽¹⁾			8	°C/W
TL	Lead Soldering Temperature (10 Seconds)			260	°C
T _{STG}	Storage Temperature		-65	, v.	°C
TJ	Junction Temperature		-40	150	°C
ESD	Electrostatic Discharge Protection Level ⁽²⁾	HBM			KV
E9D	Electrostatic discharge Protection Level 7	CDM	2		

Notes:

- Junction-to-ambient thermal resistance, θ_{JA}, is a strong function c PCL naterial board thickness, thickness and number of copper planes, number of via used, diameter of via used. Tval the pper surface, and attached heat sink characteristics.
- 2. Using Mil Std. 883E, method 3015.7 (Human Body Model and FlAct D22C10: -A (Charged Device Model)

Recommended Operating Con

The Recommended Operating C dition tal defines the conditions for actual derice operation. Recommended operating conditions are specifie to ensure operating conditions are specified to ensure operations. Fairchild does not recommend exceeding the defining talk defines the conditions for actual derice operation. Recommended operations for actual derice operation. Recommended operations are specified to the conditions of actual derice operation. Recommended operation operations are specified to the conditions are specified to the conditio

Symbols	aramet	er	Mir).	Тур.	Max.	Unit
V _{IN}	E pply ''altay ige		4.5		5.5	V
V _{OUT}	Output Voluge Range, Adjus	stable Version	0.8		3.5	V
·OU1	ıtpu. Jurrent				1.5	Α
L	Invuctor ⁽³⁾			3.3		μH
11	Input Capacitor ⁽³⁾			10		μF
C _{OUT}	Output Capacitor (3)			4 x 10		μF
FIL	Operating Ambient	FAN2012MPX	0		+85	°C
C TA	Temperature Range	FAN2012EMPX	-40		+85	°C

Notes:

3. Refer to the Applications section for details.

Electrical Characteristics

 $V_{IN}=4.5$ V to 5.5 V, $V_{OUT}=1.2$ V, $I_{OUT}=200$ mA, $C_{IN}=10~\mu F,~C_{OUT}=4~x~10~\mu F,~L=3.3~\mu H,~T_A=0^{\circ}C$ to +85°C, unless otherwise noted. Typical values are at $T_A=25^{\circ}C.$

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
V _{IN}	Input Voltage		4.5		5.5	V
ΙQ	Quiescent Current	I _{OUT} = 0 mA		7	10	mA
\/	UVLO Threshold	V _{IN} Rising	3.4	3.7	4.0	V
V_{UVLO}	OVLO Tilleshold	Hysteresis		150		mV
$R_{\text{ON_PMOS}}$	PMOS On Resistance	$V_{IN} = V_{GS} = 5 \text{ V}$		150	290	M□
R _{ON_NMOS}	NMOS On Resistance	$V_{IN} = V_{GS} = 5 \text{ V}$		150	290	m□
I _{LIMIT}	P-Channel Current Limit	4.5 V < V _{IN} < 5.5 V	2.2	2.6	3.5	Α
T _{OVP}	Over-Temperature	Rising Temperature		J0		(C)
I OAb	Protection	Hysteresis		26		°C
f_{SW}	Switching Frequency		1 70	ارور	1600	kHz
R _{LINE}	Line Regulation	V _{IN} = 4.5 to 5.5 V, I _{OUT} = 100 r A		0.13	1	%/V
R _{LOAD}	Load Regulation	0 mA ≤ I _{OUT} ≤ 1500 mA		0.2	0.5	%
V_{OUT}	Output Voltage During	I _{OUT} from 700 mA tc 70 . 1	OL		5	%
V 001	Load Transition ⁽⁴⁾	I _{OUT} from 100 1 to 7 L mA	-5	0/1		%
I _{LEAK}	Reverse Leakage Current into Pin SW	$V_{IN} = Op$, $EN = ND$, $V_{SW} = 5.5 V$	ON	0.1	1.0	μA
V_{REF}	Reference Voltage	SHIP	0	0.8		V
		= 5 to 5.5 V, (F,3.N2012MiPX	-2		2	%
V _{OUT}	Output Voltage Accu cy	0 A ≤ UT ≤ 15) mA FAN20\2EMPX	-3		3	%
I _{SD}	Shutdown I ode Supply Current	V _{EN} = 0 V		0.1	1.0	μA
I _{BIAS}	E Bias Curre	K ON C. P			0.1	μA
V _{ENH}	FN miGH \ ltage	, CO. 11	1.3			V
ENL	L 'Lc √oltage		7		0.4	V

A es:

4. Plear refer to the load transition response tost waveform shown in Figure 3.

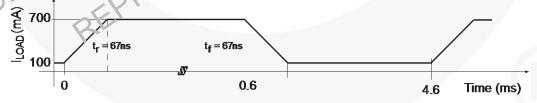


Figure 3. Load Transient Response Test Waveform

Typical Performance Characteristics

 $T_A = 25$ °C, $C_{IN} = 10 \ \mu F$, $C_{OUT} = 40 \ \mu F$, $L = 3.3 \ \mu H$, $V_{IN} = 5 \ V$; unless otherwise noted.

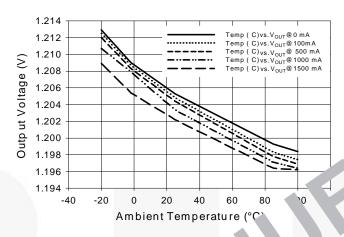


Figure 4. Output Voltage vs Amb nt in the little

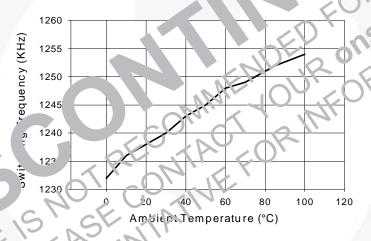


Figure 5. Switching Frequency vs. Ambient Temperature

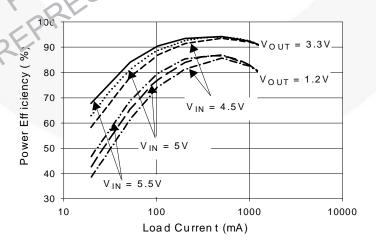
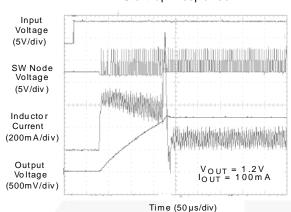


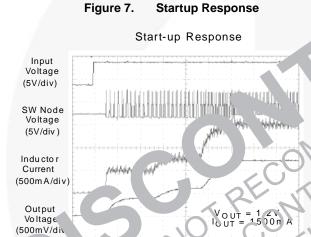
Figure 6. Efficiency vs. Load Current

Typical Performance Characteristics (Continued) $T_A = 25$ °C, $C_{IN} = 10 \mu F$, $C_{OUT} = 40 \mu F$, $L = 3.3 \mu H$, $V_{IN} = 5 V$; unless otherwise noted. Start-up Response



Start-up Response Input Voltage (5V/div) SW Node Voltage (5V/div) Inductor Current (200mA/div) Output Voltage (1V/div) (100 µs/di /)

Startup Response



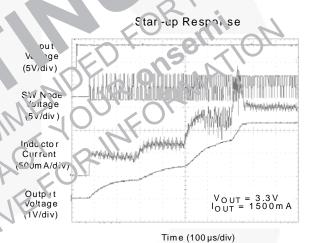


Figura 9. Startuo Response

Tin.e (100 ;: s, 'iv)

ransient Response

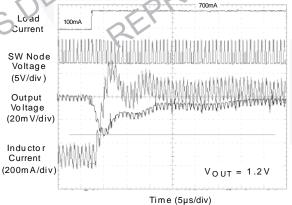
Figure 10. **Startup Response** Transient Response

Load

Output

Curr ent

re 8



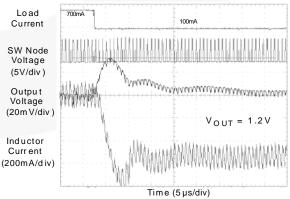
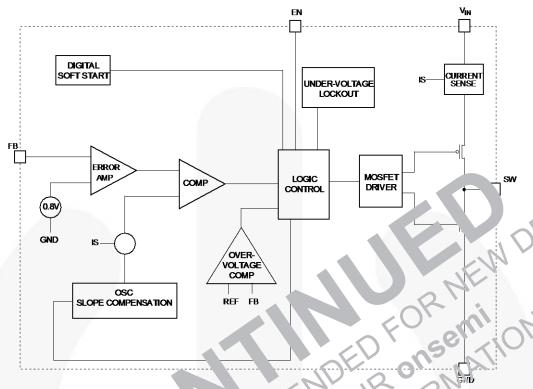


Figure 11. Transient Response

Figure 12. Transient Response

Block Diagram



Figu. 3. Block Diagram

Detailed C veration. To cription

The FAN2 '2 is a stoodown pulse width modulated (PV) urre in converter with a typical switching quency of 3 MHz. A the beginning of each clock c) a, the P-channel transistor is furned on. The ind, 'or arrent ramps up and is monitored via an intern circuit. The P-channel switch is ruined off when the sensed current causes the PWW comparator to trip when the output voltage is in regulation or when the inductor current reaches the current limit (set internally, typically 2600 mA). After a minimum dead time, the Nchannel transistor is terrica on and the inductor current ramps down. As the clock cycle is completed, the Nchannel switch is turned off and the next clock cycle starts. The duty cycle is solely given by the ratio of output voltage and input voltage. Therefore, the converter runs with a minimum duty cycle when output voltage is at minimum and input voltage is at maximum.

UVLO and Soft Start

The reference and the circuit remain reset until the V_{IN} crosses its UVLO threshold.

The FAN2012 has an internal soft-start circuit that limits the in-rush current during start-up. This prevents

possible voltage drops of the input voltage and eliminates the output voltage overshoot. The soft-start is implemented as a digital circuit, increasing the switch current in four steps to the P-channel current limit (2600 mA). Typical start-up time for a 40 μ F output capacitor and a load current of 1500 mA is 800 μ s.

Short-Circuit Protection

The switch peak current is limited cycle by cycle to a typical value of 2600 mA. In the event of an output voltage short circuit, the device operates with a frequency of 400 kHz and minimum-duty cycle, therefore the average input current is typically 350 mA.

Thermal Shutdown

When the die temperature exceeds 150°C, a reset occurs and remains in effect until the die cools to 130°C, at which point, the circuit restarts.

Applications Information

Setting the Output Voltage

The internal voltage reference is 0.8 V. The output is divided down by a voltage divider, R1 and R2 to the FB pin. The output voltage is:

$$V_{OUT} = V_{REF} \left(1 + \frac{R_1}{R_2} \right)$$
 EQ. 2

According to this equation, and assuming desired output voltage of 1.5096 V, and given R2 = 10 k Ω , the calculated value of R1 is 8.87 k Ω .

Inductor Selection

The inductor parameters directly related to device performance are saturation current and DC resistance. The FAN2012 operates with a typical inductor value of 3.3 µH. The lower the DC resistance, the higher the efficiency. For saturation current, the inductor should be rated higher than the maximum load current, plus half of the inductor ripple current calculated as follows:

$$\Delta I_{L} = V_{OUT} \times \frac{1 - (V_{OUT} / V_{IN})}{L \times f}$$
 EQ. 3

where:

 ΔI_L = Inductor Ripple Current

f = Switching Frequency

L = Inductor Value

Some recommended inductors ar nes d in eatable below:

Table 1. Recommender' ..u..cto.

Inductor Value	endor	Part Number
3.3 µH	Pa. Por	ELICPM3P3N
3.3 L	/lurata	LQS66C3R3M04
-tH	Coiltronics	SD 3R3-R

C nacit is selection

For performances, a low-ESR input capacitor is required. A ceramic capacitor of at least 10 µF, placed as close to the VIN and AGND pins of the device is recommended. The output capacitor determines the output ripple and the transien' response.

Vable 2. Recommended Capacitors

Capacitor Value	Vendor	Part Number
	Taivo Vudon	JMK212BJ106MG
	Taiyo Yuden	JMK316BJ106KL
10 μF	TDK	C2012X5ROJ106K
	IDK	C3216X5ROJ106M
	Murata	GRM32ER61C106K

PCB Layout Recommendations

The inherently high peak currents and switching frequency of power supplies require a careful PCB layout design. For best results, use wide traces for high-current paths and place the input capacitor, the inductor, and the output capacitor as close as possible to the integrated circuit terminals. To minimize voltage stress to the device resulting from ever-present switching spikes, use an input bypass capacitor with low ESR. Use of an external Schottky diode, with its anode connected to SW node and cathode connected to PVIN, further reduces switching spike. Note that the peak amplitude of the switching spike. The higher he and current, the higher he and current, the higher he are switching spikes.

The resistor divide that is the output voltage should be routed away from the fluor to avoid RF coupling. The ground plane at a bound side of the PCB acts as an election and etic hield to reduce EMI. The recommend 1 Proposition of the produce is shown below in Figure 14.

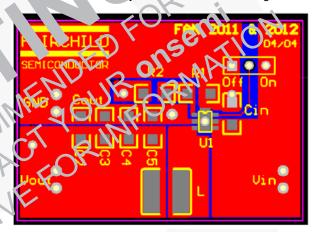
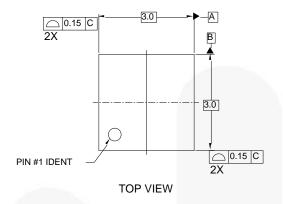
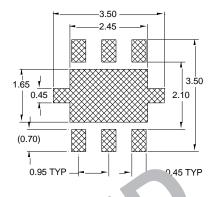
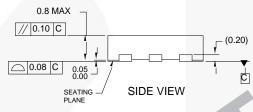


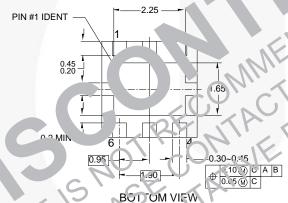
Figure 14. Recommended PCB Layout

Physical Dimensions









OTES:

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIC'NS AND TOLERANCES PER ASME Y14.5M, 1994

MLP06FrevA

Figure 15. 3x3 mm, 6-Lead, Molded Leadless Package (MLP)

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Definition of Terms		
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