Boost Converter Stage in APM16 Series for Multiphase and Semi-Bridgeless PFC

FAM65CR51XZ1, FAM65CR51XZ2

Features
• Integrated SIP or DIP Boost Converter Stage Power Module for On-board Charger (OBC) in EV or PHEV
• 5 kV/1 sec Electrically Isolated Substrate for Easy Assembly
• Creepage and Clearance per IEC60664–1, IEC 60950–1
• Compact Design for Low Total Module Resistance
• Module Serialization for Full Traceability
• Low Thermal Resistance Due to the Used ALN Substrate
• AEC–Q101 & AQG324 Qualified and PPAP Capable
• UL94V–0 Compliant
• These Devices are Pb–Free and are RoHS Compliant

Applications
• PFC Stage of an On-board Charger in PHEV or EV

Benefits
• Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO₂ Emission
• Simplified Assembly, Optimized Layout, High Level of Integration, and Improved Thermal Performance

MARKING DIAGRAM

ORDERING INFORMATION
See detailed ordering and shipping information on page 2 of this data sheet.
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Lead Forming</th>
<th>DBC Material</th>
<th>Pb-Free and RoHS Compliant</th>
<th>Operating Temperature (Ta)</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAM65CR51XZ1</td>
<td>APMCD–A16</td>
<td>Y–Shape</td>
<td>AlN</td>
<td>Yes</td>
<td>−40°C–125°C</td>
<td>72 Units / Tube</td>
</tr>
<tr>
<td>FAM65CR51XZ2</td>
<td>APMCD–B16</td>
<td>L–Shape</td>
<td>AlN</td>
<td>Yes</td>
<td>−40°C–125°C</td>
<td>72 Units / Tube</td>
</tr>
</tbody>
</table>

Pin Configuration and Block Description

Table 1. PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2</td>
<td>AC1</td>
<td>Phase 1 Leg of the PFC Bridge</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>Not Connected</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>Not Connected</td>
</tr>
<tr>
<td>5, 6</td>
<td>B+</td>
<td>Positive Battery Terminal</td>
</tr>
<tr>
<td>7, 8</td>
<td>Q1 Source</td>
<td>Source Terminal of Q1</td>
</tr>
<tr>
<td>9</td>
<td>Q1 Gate</td>
<td>Gate Terminal of Q1</td>
</tr>
<tr>
<td>10</td>
<td>Q2 Gate</td>
<td>Gate Terminal of Q2</td>
</tr>
<tr>
<td>11, 12</td>
<td>Q2 Source</td>
<td>Source Terminal of Q2</td>
</tr>
<tr>
<td>13</td>
<td>NC</td>
<td>Not Connected</td>
</tr>
<tr>
<td>14</td>
<td>NC</td>
<td>Not Connected</td>
</tr>
<tr>
<td>15, 16</td>
<td>AC2</td>
<td>Phase 2 Leg of the PFC Bridge</td>
</tr>
</tbody>
</table>

Figure 1. Pin Configuration
INTERNAL EQUIVALENT CIRCUIT

Figure 2. Internal Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS OF MOSFET (T_J = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DS (Q1–Q2)</td>
<td>Drain-to-Source Voltage</td>
<td>650</td>
<td>V</td>
</tr>
<tr>
<td>V_GS (Q1–Q2)</td>
<td>Gate-to-Source Voltage</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>I_D (Q1–Q2)</td>
<td>Drain Current Continuous (T_C = 25°C, V_GS = 10 V) (Note 1)</td>
<td>64</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Drain Current Continuous (T_C = 100°C, V_GS = 10 V) (Note 1)</td>
<td>40</td>
<td>A</td>
</tr>
<tr>
<td>E_AS (Q1–Q2)</td>
<td>Single Pulse Avalanche Energy (Note 2)</td>
<td>623</td>
<td>mJ</td>
</tr>
<tr>
<td>P_D</td>
<td>Power Dissipation (T_C = 25°C, V_GS = 10 V) (Note 1)</td>
<td>463</td>
<td>W</td>
</tr>
<tr>
<td>T_J</td>
<td>Maximum Junction Temperature</td>
<td>−55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>T_C</td>
<td>Maximum Case Temperature</td>
<td>−40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>T_STG</td>
<td>Storage Temperature</td>
<td>−40 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum continuous current and power, without switching losses, to reach T_J = 150°C respectively at T_C = 25°C and T_C = 100°C; defined by design based on MOSFET R_DS(ON) and max. R_θJC and not subject to production test

DBC Substrate
0.63 mm AlN with 0.3 mm copper on both sides. DBC substrate is NOT nickel plated.

Lead Frame
OFC copper alloy, 0.50 mm thick. Plated with 8 µm to 25.4 µm thick Matte Tin.

Flammability Information
All materials present in the power module meet UL flammability rating class 94V-0.

Compliance to RoHS Directives
The power module is 100% lead free and RoHS compliant 2000/53/C directive.

Solder
Solder used is a lead free SnAgCu alloy. Solder presents high risk to melt at temperature beyond 210°C. Base of the leads, at the interface with the package body, should not be exposed to more than 200°C during mounting on the PCB or during welding to prevent the re-melting of the solder joints.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Defined by design, not subject to production test
Table 4. ABSOLUTE MAXIMUM RATINGS OF THE BOOST DIODE \( (T_J = 25^\circ C \text{ unless otherwise noted}) \) (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{RRM} )</td>
<td>Peak Repetitive Reverse Voltage ( (Note 5) )</td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>( V_{RWM} )</td>
<td>Working Peak Reverse Voltage ( (Note 5) )</td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>( V_R )</td>
<td>DC Blocking Voltage</td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>( I_{F(AV)} )</td>
<td>Average Rectified Forward Current ( T_C = 25^\circ C )</td>
<td>15</td>
<td>A</td>
</tr>
<tr>
<td>( I_{FSM} )</td>
<td>Non-Repetitive Peak Surge Current (Half Wave 1 Phase 60 Hz)</td>
<td>45</td>
<td>A</td>
</tr>
<tr>
<td>( T_J )</td>
<td>Maximum Junction Temperature</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
<tr>
<td>( T_C )</td>
<td>Maximum Case Temperature</td>
<td>-40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{STG} )</td>
<td>Storage Temperature</td>
<td>-40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>( E_{AVL} )</td>
<td>Avalanche Energy ( (2.85 \text{ A, } 1 \text{ mH}) )</td>
<td>4</td>
<td>mJ</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Defined by design, not subject to production test
5. \( V_{RRM} \) and \( I_{F(AV)} \) value referenced to TO220−2L Auto Qualified Package Device ISL9R1560P_F085

Table 5. ELECTRICAL SPECIFICATIONS OF THE BOOST DIODE \( (T_J = 25^\circ C \text{ unless otherwise noted}) \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_R )</td>
<td>Instantaneous Reverse Current</td>
<td>( V_R = 600 \text{ V} ) ( T_C = 25^\circ C )</td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>( \mu \text{A} )</td>
</tr>
<tr>
<td>( V_{FM} )</td>
<td>Instantaneous Forward Voltage ( (Note 7) )</td>
<td>( I_R = 15 \text{ A} ) ( \frac{dI_R}{dt} = 200 \text{ A/\mu s} ) ( V_R = 390 \text{ V} ) ( T_C = 25^\circ C )</td>
<td>–</td>
<td>1.65</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>( T_{tr} )</td>
<td>Reverse Recovery Time</td>
<td>( I_R = 15 \text{ A} ) ( \frac{dI_R}{dt} = 200 \text{ A/\mu s} ) ( V_R = 390 \text{ V} ) ( T_C = 25^\circ C )</td>
<td>–</td>
<td>1.24</td>
<td>1.7</td>
<td>V</td>
</tr>
<tr>
<td>( t_a )</td>
<td>Time to reach peak reverse current</td>
<td>( I_R = 15 \text{ A} ) ( \frac{dI_R}{dt} = 200 \text{ A/\mu s} ) ( V_R = 390 \text{ V} ) ( T_C = 25^\circ C )</td>
<td>–</td>
<td>16</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>( t_b )</td>
<td>Time from peak ( I_{RRM} ) to projected zero crossing of ( I_{RRM} ) based on a straight line from peak ( I_{RRM} ) through 25% of ( I_{RRM} ) ( T_C = 25^\circ C )</td>
<td>–</td>
<td>13</td>
<td>–</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( Q_{rr} )</td>
<td>Reverse Recovered Charge</td>
<td>( T_C = 25^\circ C )</td>
<td>–</td>
<td>43</td>
<td>–</td>
<td>nC</td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Defined by design, not subject to production test
7. Test pulse width = 300 \( \mu \text{s} \), Duty Cycle = 2%

Table 6. THERMAL RESISTANCE

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JC} ) (per MOSFET chip) ( Q1, Q2 ) Thermal Resistance Junction→to–Case ( (Note 8) )</td>
<td>–</td>
<td>0.19</td>
<td>0.27</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JS} ) (per MOSFET chip) ( Q1, Q2 ) Thermal Resistance Junction→to–Sink ( (Note 9) )</td>
<td>–</td>
<td>0.62</td>
<td>–</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JC} ) (per DIODE chip) ( D1, D2 ) Thermal Resistance Junction→to–Case ( (Note 8) )</td>
<td>–</td>
<td>0.74</td>
<td>1.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JS} ) (per DIODE chip) ( D1, D2 ) Thermal Resistance Junction→to–Sink ( (Note 9) )</td>
<td>–</td>
<td>1.65</td>
<td>–</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

8. \( R_{JC} \) (junction to case) Test method compliant with MIL STD 883−1012.1, from case temperature under the chip to case temperature measured below the package at the chip center. Cosmetic oxidation and discoloration on the DBC surface allowed
9. \( R_{JS} \) (junction to heat sink) Defined by thermal simulation assuming the module is mounted on a 5 mm Al−360 die casting material with 30 \( \mu \text{m} \) of 1.8 W/mK thermal interface material

Table 7. ISOLATION \( (\text{Isolation resistance at tested voltage between the base plate and to control pins or power terminals.}) \)

<table>
<thead>
<tr>
<th>Test</th>
<th>Test Conditions</th>
<th>Isolation Resistance</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage @ Isolation Voltage (Hi−Pot)</td>
<td>( V_{AC} = 5 \text{ kV, } 50 \text{ Hz} )</td>
<td>100 M &lt;</td>
<td>( \Omega )</td>
</tr>
</tbody>
</table>
Table 8. REFERENCE TO TABLE 3: PARAMETER OF MOSFET ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BVDSS</strong></td>
<td>Q1, Q2 MOSFET Drain–to–Source Breakdown Voltage &lt;br&gt;The maximum drain–to–source voltage the MOSFET can endure without the avalanche breakdown of the body–drain P–N junction in off state. &lt;br&gt;The measurement conditions are to be found in table 3. &lt;br&gt;The typ. Temperature behavior is described in Figure 14</td>
</tr>
<tr>
<td><strong>VGS(th)</strong></td>
<td>Q1, Q2 MOSFET Gate to Source Threshold Voltage &lt;br&gt;The gate–to–source voltage measurement is triggered by a threshold ID current given in conditions at table 4 &lt;br&gt;The typ. Temperature behavior can be found in Figure 11</td>
</tr>
<tr>
<td><strong>RDS(ON)</strong></td>
<td>Q1, Q2 MOSFET On Resistance &lt;br&gt;RDS(on) is the total resistance between the source and the drain during the on state. &lt;br&gt;The measurement conditions are to be found in table 3. &lt;br&gt;The typ behavior can be found in Figure 12 and Figure 13 as well as Figure 18</td>
</tr>
<tr>
<td><strong>gFS</strong></td>
<td>Q1, Q2 MOSFET Forward Transconductance &lt;br&gt;Transconductance is the gain in the MOSFET, expressed in the Equation below. &lt;br&gt;It describes the change in drain current by the change in the gate–source bias voltage: &lt;br&gt;$$g_{fs} = \frac{\Delta I_{DS}}{\Delta V_{GS}}v_{DS}$$</td>
</tr>
<tr>
<td><strong>IGSS</strong></td>
<td>Q1, Q2 MOSFET Gate–to–Source Leakage Current &lt;br&gt;The current flowing from Gate to Source at the maximum allowed VGS &lt;br&gt;The measurement conditions are described in the table 3.</td>
</tr>
<tr>
<td><strong>IDSS</strong></td>
<td>Q1, Q2 MOSFET Drain–to–Source Leakage Current &lt;br&gt;Drain – Source current is measured in off state while providing the maximum allowed drain–to–source voltage and the gate is shorted to the source. &lt;br&gt;IDSS has a positive temperature coefficient.</td>
</tr>
</tbody>
</table>
Figure 3. Timing Measurement Variable Definition

### Table 9. PARAMETER OF SWITCHING CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turn–On Delay (td(on))</td>
<td>This is the time needed to charge the input capacitance, Ciss, before the load current ID starts flowing. The measurement conditions are described in the table 3. For signal definition please check Figure 3 above.</td>
</tr>
<tr>
<td>Rise Time (tr)</td>
<td>The rise time is the time to discharge output capacitance, Coss. After that time the MOSFET conducts the given load current ID. The measurement conditions are described in the table 3. For signal definition please check Figure 3 above.</td>
</tr>
<tr>
<td>Turn–On Time (ton)</td>
<td>Is the sum of turn–on–delay and rise time</td>
</tr>
<tr>
<td>Turn–Off Delay (td(off))</td>
<td>td(off) is the time to discharge Ciss after the MOSFET is turned off. During this time the load current ID is still flowing. The measurement conditions are described in the table 3. For signal definition please check Figure 3 above.</td>
</tr>
<tr>
<td>Fall Time (tf)</td>
<td>The fall time, tf, is the time to charge the output capacitance, Coss. During this time the load current drops down and the voltage VDS rises accordingly. The measurement conditions are described in the table 3. For signal definition please check Figure 3 above.</td>
</tr>
<tr>
<td>Turn–Off Time (toff)</td>
<td>Is the sum of turn–off–delay and fall time</td>
</tr>
</tbody>
</table>
Table 10. REFERENCE TO TABLE 5: PARAMETER OF DIODE ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantaneous Reverse Current (I_R)</td>
<td>Current flowing in reverse after the reverse recovery time t_rr. I_R is shown in Figure 4 above. The behavior over voltage can be seen in Figure 23</td>
</tr>
<tr>
<td>Instantaneous Forward Voltage VFM</td>
<td>Voltage drop over the diode in a dynamic condition given in Note 7. The voltage is measured after the given test pulse width. To avoid self heating effects a small duty cycle is used. The behavior over voltage can be seen in Figure 22</td>
</tr>
<tr>
<td>Reverse Recovery Time t_rr</td>
<td>During this transition time, from conduction to blocking, the current is flowing in reverse direction and diode generates switching losses. The time is characterized on the scope by using the ta and tb approximation method. ta + tb = t_tr parameter result in table 3. The parameter is dependent on temperature and initial dI/dt. Figure 25 shows the dependency on dI/dt</td>
</tr>
<tr>
<td>Time to reach peak reverse current t_a</td>
<td>ta is the transition time from the moment the current starts to flow in reverse direction until the diode voltage drops (also the reverse current peak)</td>
</tr>
<tr>
<td>Time from peak IRM to zero crossing t_b</td>
<td>tb is defined by using a linear approximation from the peak IRM to a projected zero crossing of IR by crossing IR at 25% of IRM</td>
</tr>
<tr>
<td>Reverse Recovered Charge Q_rr</td>
<td>The reverse recovery charge is defined as Q_rr = \int_{t_a}^{t_b} I_R(t) dt. This parameter is highly depend on temperature and dI/dt. See Figure 27</td>
</tr>
</tbody>
</table>
FAM65CR51XZ1, FAM65CR51XZ2

TYPICAL CHARACTERISTICS - MOSFETS

Figure 5. Normalized Power Dissipation vs. Case Temperature

Figure 6. Maximum Continuous \( I_D \) vs. Case Temperature

Figure 7. Transfer Characteristics

Figure 8. Forward Diode

Figure 9. On Region Characteristics (25°C)

Figure 10. On Region Characteristics (150°C)
FAM65CR51XZ1, FAM65CR51XZ2

TYPICAL CHARACTERISTICS - MOSFETS (continued)

Figure 11. On-Resistance vs. Gate-to-Source Voltage

Figure 12. \( R_{DS(\text{norm})} \) vs. Junction Temperature

Figure 13. Normalized Gate Threshold Voltage vs. Temperature

Figure 14. Normalized Breakdown Voltage vs. Temperature

Figure 15. Eoss vs. Drain-to-Source Voltage

Figure 16. Capacitance Variation
FAM65CR51XZ1, FAM65CR51XZ2

TYPICAL CHARACTERISTICS - MOSFETS (continued)

Figure 17. Gate Charge Characteristics

Figure 18. ON-Resistance Variation with Drain Current and Gate Voltage

Figure 19. Safe Operating Area

Figure 20. Peak Current Capability

Figure 21. Peak Transient Power Capability

NOTE:

R_{JC} = 0.27°C/W

Duty Cycle: D = t_1/t_2

Peak T_J = PDM x Z_{JUC}(t) + T_C

Derate peak current as follows:

I_{DM} = I_{25} \times \sqrt{\frac{150 - T_C}{125}}
TYPICAL CHARACTERISTICS - DIODES

Figure 22. Typical Forward Voltage Drop vs. Forward Current

Figure 23. Typical Reverse Current vs. Reverse Voltage

Figure 24. Capacitance

Figure 25. Reverse Recovery Time vs. di/dt

Figure 26. Reverse Recovery Current vs. di/dt

Figure 27. Reverse Recovery Charge vs. di/dt
Figure 28. Transient Thermal Impedance
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

APMCD–A16 / 12LD, AUTOMOTIVE MODULE
CASE MODGG
ISSUE C

DATE 03 NOV 2021

NOTES:
1. DIMENSIONING AND TOLERANCING PER:
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH AND TIE BAR EXTRUSIONS.

<table>
<thead>
<tr>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIM</td>
</tr>
<tr>
<td>A2</td>
</tr>
<tr>
<td>b</td>
</tr>
<tr>
<td>b2</td>
</tr>
<tr>
<td>c</td>
</tr>
<tr>
<td>D</td>
</tr>
<tr>
<td>E</td>
</tr>
<tr>
<td>E1</td>
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<td>E2</td>
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<td>L1</td>
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<td>L2</td>
</tr>
<tr>
<td>q</td>
</tr>
<tr>
<td>S</td>
</tr>
<tr>
<td>ΦA</td>
</tr>
</tbody>
</table>

*This information is generic. Please refer to device data sheet for actual part marking.

Pb–Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.

GENERAL MARKING DIAGRAM*

| XXXXX = Specific Device Code |
| ZZZ = Lot ID |
| AT = Assembly & Test Location |
| Y = Year |
| WW = Work Week |
| NNN = Serial Number |

*This information is generic. Please refer to device data sheet for actual part marking.

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

APMCD-B16 / 12LD, AUTOMOTIVE MODULE
CASE MODGK
ISSUE D

DATE 04 NOV 2021

NOTES:
1. DIMENSIONING AND TOLERANCING PER.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH AND TIE BAR EXTRUSIONS.

<table>
<thead>
<tr>
<th>MILLIMETERS</th>
<th>MIN.</th>
<th>NOM.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>4.30</td>
<td>4.50</td>
<td>4.70</td>
</tr>
<tr>
<td>b</td>
<td>0.45</td>
<td>0.50</td>
<td>0.60</td>
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**GENERIC MARKING DIAGRAM**

<table>
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<th>XXXX = Specific Device Code</th>
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<tr>
<td>ZZZ = Lot ID</td>
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<td>AT = Assembly &amp; Test Location</td>
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<td>Y = Year</td>
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<td>W = Work Week</td>
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<td>NNN = Serial Number</td>
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*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot ",", may or may not be present. Some products may not follow the Generic Marking.

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