Half-Bridge Gate Driver
1200 V 2.5 A Source/3.4 A Sink

FAD8253MX-1

Description
The FAD8253 is a monolithic half-bridge gate driver IC designed for driving high voltage, high speed and high power IGBTs up to +1200 V. The FAD8253 employs ON’s high-voltage process and common-mode noise canceling technique to provide stable operation of high-side driver under high dv/dt noise circumstances. The gate driver includes UVLO circuits tailored to IGBT threshold for both high side and low side outputs to prevent malfunction when VDD and VBS are lower than the specified threshold voltage.

The FAD8253 offers a built-in low-side current detection circuitry with an additional provision for soft shutdown (for low side) during overcurrent or short-circuit conditions. The driver can provide adequate protection during short-circuits by turning off its outputs while simultaneously generating a fault output for fault reporting purposes. The driver also provides additional flexibility by providing a shutdown pin to disable driver outputs externally.

Features
- Floating Channel for Bootstrap Operation to +1200 V
- Peak Output Current Capability of 2.5 A Source/3.4 A Sink
- Allowable Negative VSTransient Swing of up to −15 V at VBS = 15 V
- Built-in Common Mode dv/dt Noise Canceling Circuit
- Separate Power and Signal Ground for Enhanced dl/dt Immunity
- Matched Propagation Delay < 50 ns
- 3.3 V and 5 V Input Logic Compatible
- Built in Shoot-through Prevention Logic with 120 ns (Typ) Dead Time
- Built-in UVLO Functions for both High and Low Side with Thresholds Optimized for IGBTs
- Built-in Low Side Short-circuit Protection with Soft Shutdown
- In SOIC14NB with Non Connected Pins for High Voltage Creepage and Clearance Requirements
- Fault Reporting during Overcurrent or Short-circuit Condition
- External Shutdown Pin to Enable or Disable Driver Outputs
- AEC-Q100 Qualified and PPAP Capable
- Pb-Free Devices

Typical Applications
- High Voltage Auxiliary Motor Drive
- Generic Half-Bridge and Full-Bridge Driver
- On-Board Chargers & DC/DC Converters
- Traction Inverters
Figure 1. 3-Phase Motor Drive Application

Figure 2. DC Motor Drive Application
FAD8253MX-1

BLOCK DIAGRAM

Figure 3. Block Diagram

PIN DESCRIPTION

PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VSS</td>
<td>Logic Ground</td>
</tr>
<tr>
<td>2</td>
<td>LIN</td>
<td>Logic Input for Low-Side Gate Driver Output</td>
</tr>
<tr>
<td>3</td>
<td>SD</td>
<td>Shutdown Control Input with Active Low</td>
</tr>
<tr>
<td>4</td>
<td>HIN</td>
<td>Logic Input for High-Side Gate Driver Output</td>
</tr>
<tr>
<td>5</td>
<td>FO</td>
<td>Fault Output with Open Drain (Low True)</td>
</tr>
<tr>
<td>6</td>
<td>CSC</td>
<td>Short-Circuit Current Detection Input</td>
</tr>
<tr>
<td>7</td>
<td>VDD</td>
<td>Low-Side and Logic Power Supply Voltage</td>
</tr>
<tr>
<td>8</td>
<td>COM</td>
<td>Low-Side Driver Return</td>
</tr>
<tr>
<td>9</td>
<td>LO</td>
<td>Low-Side Driver Output</td>
</tr>
<tr>
<td>12</td>
<td>VS</td>
<td>High-Side Floating Supply Return</td>
</tr>
<tr>
<td>13</td>
<td>HO</td>
<td>High-Side Driver Output</td>
</tr>
<tr>
<td>14</td>
<td>VB</td>
<td>High-Side Floating Supply</td>
</tr>
<tr>
<td>10, 11</td>
<td>NC</td>
<td>No Connect</td>
</tr>
</tbody>
</table>
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS</td>
<td>High–side Offset Voltage VS</td>
<td>(V_B – 25) to (V_B + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>VB</td>
<td>High–side Floating Supply Voltage VB</td>
<td>–0.3 to 1225</td>
<td>V</td>
</tr>
<tr>
<td>VW</td>
<td>High–side Floating Output Voltage</td>
<td>(VS – 0.3) to (VB + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>Low–side and Logic–fixed Supply Voltage</td>
<td>–0.3 to 25</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Logic Input Voltage (HIN, LIN, SD)</td>
<td>–0.3 to (VDD + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>VCS</td>
<td>Current Sense Input Voltage</td>
<td>–0.3 to (VDD + 0.3)</td>
<td>V</td>
</tr>
<tr>
<td>dVg/dt</td>
<td>Allowable Offset Voltage Slew Rate</td>
<td>50</td>
<td>V/ns</td>
</tr>
<tr>
<td>P_D</td>
<td>Power Dissipation (SO14NB) (Note 1)</td>
<td>0.8</td>
<td>W</td>
</tr>
<tr>
<td>θJA</td>
<td>Thermal Resistance, Junction–to–Ambient (SO14NB)</td>
<td>156</td>
<td>°C/W</td>
</tr>
<tr>
<td>TJ(max)</td>
<td>Junction Temperature</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature</td>
<td>–55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>ESDHBM</td>
<td>ESD, Human Body Model (Note 3)</td>
<td>2500</td>
<td>V</td>
</tr>
<tr>
<td>ESDCDM</td>
<td>ESD, Charged Device Model (Note 3)</td>
<td>750</td>
<td>V</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Do not exceed PD under any circumstances.
2. Mounted on 76.2 × 114.3 × 1.6 mm PCB (FR–4 glass epoxy material). Refer to the following standards:
   - JESD51–2: Integral circuits thermal test method environmental conditions – natural convection
   - JESD51–3: Low effective thermal conductivity test board for leaded surface mount packages
3. This device series incorporates ESD protection and is tested by the following methods:
   - ESD Human Body Model tested per ANSI/ESDA/JEDEC JS–001–2012
   - ESD Charged Device Model tested per JESD22–C101

RECOMMENDED OPERATING RANGES (Parameters are referenced to VSS)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage Range</td>
<td>4.5</td>
<td>18.0</td>
<td>V</td>
</tr>
<tr>
<td>VS</td>
<td>High–Side VS Floating Supply Offset Voltage (Note 4)</td>
<td>5 – VBS</td>
<td>1200</td>
<td>V</td>
</tr>
<tr>
<td>VBS</td>
<td>High–side BS Bootstrap Voltage</td>
<td>VBSUV+</td>
<td>22</td>
<td>V</td>
</tr>
<tr>
<td>VH</td>
<td>High–Side Output Voltage</td>
<td>VS</td>
<td>VB</td>
<td>V</td>
</tr>
<tr>
<td>VDD</td>
<td>Low–Side and Logic Supply Voltage</td>
<td>VDDUV+</td>
<td>22</td>
<td>V</td>
</tr>
<tr>
<td>VLO</td>
<td>Low–Side Output Voltage</td>
<td>COM</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>Logic Input Voltage (IN, SD)</td>
<td>V_S</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td>COM</td>
<td>Power Ground</td>
<td>VDD – 22</td>
<td>VDD</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Ambient Temperature (Note 5)</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Recommended based on min 5 V on VB, for proper operation of the level shifter circuit and ensure proper propagation of the signal from the input to the output.
5. Power and thermal impedance should be determined with care so that T_j does not exceed 150°C.
ELECTRICAL CHARACTERISTICS

(V_{BIAS} (V_{DD}, V_{BS}) = 15 V, T_A = -40°C to 125°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS}. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>LOW SIDE POWER SUPPLY SECTION</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{QDD}</td>
<td>Quiescent V_{DD} Supply Current</td>
<td>V_{LIN} = 0 V or 5 V</td>
<td>50</td>
<td>280</td>
<td>400</td>
<td>μA</td>
</tr>
<tr>
<td>I_{PD}</td>
<td>Operating V_{DD} Supply Current</td>
<td>C_L = 1 nF, f_{LIN} = 20 kHz, rms value</td>
<td>400</td>
<td>660</td>
<td>800</td>
<td>μA</td>
</tr>
<tr>
<td>V_{DDUV+}</td>
<td>V_{DD} Supply Under−Voltage Positive−going Threshold</td>
<td>V_{DD} = Rising</td>
<td>11</td>
<td>12</td>
<td>12.9</td>
<td>V</td>
</tr>
<tr>
<td>V_{DDUV−}</td>
<td>V_{DD} Supply Under−Voltage Negative going Threshold</td>
<td>V_{DD} = Falling</td>
<td>10.5</td>
<td>11.4</td>
<td>12.4</td>
<td>V</td>
</tr>
<tr>
<td>V_{DDHYS}</td>
<td>V_{DD} Supply Under−Voltage Lockout Hysteresis</td>
<td>–</td>
<td>0.6</td>
<td>–</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

BOOSTERAPPED POWER SUPPLY SECTION |
| I_{QBS} | Quiescent V_{BS} Supply Current | V_{HIN} = 0 V or 5 V | – | 25 | 45 | μA |
| I_{PBS} | Operating V_{BS} Supply Current | C_L = 1 nF, f_{HIN} = 20 kHz, rms value | – | 430 | 550 | μA |
| I_LK | Offset Supply Leakage Current | V_B = V_S = 1200 V | – | – | 120 | μA |
| V_{BSUV+} | V_{BS} Supply Under−Voltage Positive−going Threshold | V_{BS} = Rising | 10.6 | 11.7 | 12.5 | V |
| V_{BSUV−} | V_{BS} Supply Under−Voltage Negative Going Threshold | V_{BS} = Falling | 10.1 | 11.1 | 11.9 | V |
| V_{BSHYS} | V_{BS} Supply Under−Voltage Lockout Hysteresis | – | 0.6 | – | V |

GATE DRIVER OUTPUT SECTION |
| V_OH | High−level Output Voltage, V_{BIAS}−V_O | I_O = 0 mA (No Load) | – | – | 50 | mV |
| V_OL | Low−level Output Voltage, V_O | I_O = 0 mA (No Load) | – | – | 50 | mV |
| I_O+ | Output HIGH Short−circuit Pulsed Current | V_O = 0 V, V_{IN} = 5 V with PW < 10 μs | 1200 | 2700 | – | mA |
| I_O− | Output LOW Short−circuit Pulsed Current | V_O = 15 V, V_{IN} = 0 V with PW < 10 μs | 1200 | 4200 | – | mA |
| V_S | Allowable Negative V_S Pin Voltage, with Signal Propagation Capability from HIN to HO | V_{BS} = 15 V | –10.0 | – | – | V |
| V_S (Note 6) | Allowable Transient Negative V_S Pin Voltage, No Signal Propagation Capability from HIN to HO | V_{BS} = 15 V | –15.0 | – | – | V |
| COM−V_SS | Allowable COM−V_SS Power/Signal Grounds Offset | V_{DD} = 15 V, V_{SS} = 0 V | –7.0 | – | – | V |

LOGIC INPUT SECTION (HIN, LIN, SD) |
| V_{IH} | Logic "1" Input Voltage Threshold | – | – | 2.5 | V |
| V_{IL} | Logic "0" Input Voltage Threshold | 1.2 | – | – | V |
| V_{INHYS} | Logic Input Hysteresis Voltage | – | 0.5 | – | V |
| I_{IN+} | Logic "1" Input Bias Current (HIN, LIN) | V_{IN} = 5 V | – | 23 | – | μA |
| I_{IN−} | Logic "0" Input Bias Current (HIN, LIN) | V_{IN} = 0 V | – | – | 2.0 | μA |
| I_{SD+} | Logic "1" Input Bias Current (SD) | V_{SD} = 5 V | – | 15.7 | – | μA |
| I_{SD−} | Logic "0" Input Bias Current (SD) | V_{SD} = 0 V | – | – | 2.0 | μA |

SHORT−CIRCUIT PROTECTION |
| V_{CSCREF} | Short−circuit detector reference voltage | 0.45 | 0.50 | 0.6 | V |
| R_{CSCIN} | Input Pull Down Short Circuit Resistance | – | 210 | – | kΩ |
| I_{CSCIN} | Short−Circuit Input Current | V_{CSCIN} = 5 V | 15 | 23.5 | 37.5 | μA |
| I_{SOFT} | Soft Turn−off Source Current | V_{DD} = 15 V, LO = 7.5 V | 70 | 110 | 140 | mA |
ELECTRICAL CHARACTERISTICS (continued)

(V\text{BIAS} (V\text{DD}, V\text{BS}) = 15 \text{ V}, T\text{A} = -40°C to 125°C unless otherwise specified. The V\text{IN} and I\text{IN} parameters are referenced to V\text{SS}. The V\text{O} and I\text{O} parameters are referenced to V\text{S} and COM and are applicable to the respective outputs HO and LO.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{FOH}</td>
<td>Fault Output High Level Voltage</td>
<td>V\text{CSC} = 0 \text{ V}, R\text{PULL-UP} = 4.7 k\Omega</td>
<td>4.7</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>V\text{FOL}</td>
<td>Fault Output Low Level Voltage</td>
<td>V\text{CSC} = 1 \text{ V}, I\text{FO} = 2 \text{ mA}</td>
<td>-</td>
<td>-</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

DYNAMIC OUTPUT SECTION

(V\text{BIAS} (V\text{DD}, V\text{BS}) = 15.0 \text{ V}, T\text{A} = -40°C to 125°C, V\text{S} = V\text{SS}, C\text{LOAD} = 1000 \text{ pF unless otherwise specified.})

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\text{on}</td>
<td>Turn–on Propagation Delay (Note 7)</td>
<td>V\text{S} = 0 \text{ V}</td>
<td>65</td>
<td>100</td>
<td>145</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{off}</td>
<td>Turn–off Propagation Delay</td>
<td>V\text{S} = 0 \text{ V or 1200 V}</td>
<td>65</td>
<td>90</td>
<td>145</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{SDOFF_LO}</td>
<td>\text{SD} to Low–side Propagation Delay</td>
<td>-</td>
<td>25</td>
<td>45</td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{SDOFF_HO}</td>
<td>\text{SD} to How–side Propagation Delay</td>
<td>-</td>
<td>65</td>
<td>95</td>
<td>145</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{r}</td>
<td>Turn–on Rise Time</td>
<td>-</td>
<td>-</td>
<td>13</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{f}</td>
<td>Turn–off Fall Time</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>26</td>
<td>ns</td>
</tr>
<tr>
<td>M\text{TON}</td>
<td>Delay Matching HO and LO Turn–On</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>M\text{TOFF}</td>
<td>Delay Matching HO and LO Turn–Off</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DT</td>
<td>Dead–time (Note 8)</td>
<td>-</td>
<td>70</td>
<td>120</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>t\text{UVFLT}</td>
<td>Under–voltage Filtering Time (Note 6)</td>
<td>-</td>
<td>10</td>
<td>-</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>t\text{CSCFLT}</td>
<td>CSC Pin Filtering Time (Note 6)</td>
<td>-</td>
<td>300</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\text{CSCFO}</td>
<td>Time from CSC Triggering to FO</td>
<td>-</td>
<td>530</td>
<td>1250</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t\text{FO}</td>
<td>Fault Output Pulse Width</td>
<td>-</td>
<td>24</td>
<td>65</td>
<td>140</td>
<td>μs</td>
</tr>
<tr>
<td>t\text{CSCLO}</td>
<td>Time from CSC Triggering to Low–side and High–side Gate Output</td>
<td>-</td>
<td>600</td>
<td>1350</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Parameter guaranteed by design.
7. The turn–on propagation delay does not includes the dead time.
8. The dead time includes the turn on propagation time.
TYPICAL CHARACTERISTICS

Figure 4. $V_{DD}$ UVLO (+) vs. Temperature

Figure 5. $V_{DD}$ UVLO (−) vs. Temperature

Figure 6. $V_{BS}$ UVLO (+) vs. Temperature

Figure 7. $V_{BS}$ UVLO (−) vs. Temperature

Figure 8. $V_{DD}$ Quiescent Current vs. Temperature

Figure 9. $V_{BS}$ Quiescent Current vs. Temperature
Figure 10. $V_{DD}$ Operating Current vs. Temperature

Figure 11. $V_{BS}$ Operating Current vs. Temperature

Figure 12. Logic High Input Bias Current vs. Temperature

Figure 13. $I_{CSCIN}$ vs. Temperature

Figure 14. $I_{SOFT}$ vs. Temperature

Figure 15. Turn–on Rising Time vs. Temperature
TYPICAL CHARACTERISTICS (Continued)

Figure 16. Turn-off Falling Time vs. Temperature

Figure 17. Turn-on Delay Time vs. Temperature

Figure 18. Turn-off Delay time vs. Temperature

Figure 19. Logic High Input Voltage Threshold vs. Temperature

Figure 20. Logic Low Input Voltage Threshold vs. Temperature

Figure 21. $V_{\text{CSCREF}}$ vs. Temperature
Figure 22. SD Logic High Input Bias Current vs. Temperature

Figure 23. Input Pull Down Short Circuit Resistance vs. Temperature

Figure 24. Fault Output High Level Voltage vs. Temperature

Figure 25. Fault Output Low Level Voltage vs. Temperature

Figure 26. Allowable Negative $V_S$ Voltage vs. Temperature

Figure 27. High-level Output Voltage vs. Temperature
Figure 28. Low-level Output Voltage vs. Temperature

Figure 29. Dead Time vs. Temperature

Figure 30. Delay Matching HO and LO Turn–on vs. Temperature

Figure 31. Delay Matching HO and LO Turn–off vs. Temperature

Figure 32. SD to Low–side Propagation Delay vs. Temperature

Figure 33. SD to High–side Propagation Delay vs. Temperature
TYPICAL CHARACTERISTICS (Continued)

Figure 34. Fault Output Minimum Pulse Width vs. Temperature

Figure 35. Time from CSC Triggering to Low-side Gate Output vs. Temperature

Figure 36. Time from CSC Triggering to High-side Gate Output vs. Temperature

Figure 37. Time from CSC Triggering to FO vs. Temperature

Figure 38. Output High Short-circuit Pulsed Current vs. Temperature

Figure 39. Output Low Short-circuit Pulsed Current vs. Temperature
Figure 40. Switching Timing Waveforms Definition (Propagation Delay, Rise and Fall Time)

Figure 41. Switching Timing Waveforms Definition (Matching Delay)
Figure 42. Switching Timing Waveforms Definition – Low Side

Figure 43. Switching Timing Waveforms Definition – High Side
Protection Function

Shutdown (SD) Function

The shutdown (SD) pin of FAD8253 is active low, meaning that the driver outputs are enabled when SD pin is pulled up and vice versa. If SD pin is pulled low for a time equivalent to propagation delay, the outputs of both high and low side driver stages are turned off. The outputs are reactivated on the next rising edge of the input signal, once the SD pin is pulled up.

Under–Voltage Lockout (UVLO)

The FAD8253 has an internal under–voltage lockout (UVLO) protection circuitry for both high–side and low–side driver stages, with a threshold optimized for IGBTs. The UVLO independently monitors the supply voltage (VDD) and bootstrap capacitor voltage (VBS) to prevent malfunction if VDD and VBS drop lower than the specified threshold voltage in the manner explained below:

- If VBS drops below its negative–going threshold voltage, the output of the high side driver stage is pulled down (or turned off).
- If VDD voltage drops below its negative–going threshold voltage, the outputs of both the low side and high side driver stages are pulled down (or turned off).

In either of the above cases, the outputs will resume their normal operation once the VBS/VDD voltages have risen back to the necessary positive going threshold, as shown in Figure 44. Moreover, the UVLO hysteresis and the UV filtering time prevent chattering during power supply transitions. If the supply voltage (VDD or VBS) maintains an under–voltage condition for a duration longer than the under–voltage filtering time, the high and low side driver outputs are turned off. Note that an UVLO event has no impact to the Fault Output flag.

Shoot–Through Prevention Function

The FAD8253 has a shoot–through prevention circuitry that monitors both the high–side and low–side inputs. It is designed to prevent the outputs of the high–side and low–side stages from turning on at the same time.

As shown in Figure 45, if the low–side input (LIN) signal is provided to the driver while the high–side input (HIN) signal is already present, the high side output (HO) is turned off immediately while the low–side output (LO) is kept turned off. In addition, both driver outputs are kept turned off for as long as both HIN and LIN are present. This prevents the shoot–through of the high–side and low–side devices in an application. Similarly, as shown in Figure 46, if HIN signal is provided to the driver while LIN signal is already present, LO is turned off immediately while HO is kept turned off.

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Figure 44. Waveforms for Under–Voltage Lockout

Figure 45. Example Waveforms for Shoot–through Prevention

Figure 46. Example waveforms for Shoot–through Prevention
Please note that the driver resumes normal operation with a built-in dead time of 120 ns (typ.) between HO and LO, only when LIN and HIN signals are not provided at the same time.

Over-Current/Short-Circuit Protection Function

The FAD8253 has a low side over-current detection circuitry that monitors the voltage across the low side current sensing resistor (\(R_{CSR}\)) through the short-circuit current detection input (CSC) pin.

The input stage of the over current circuitry is depicted in Figure 47. The principle of overcurrent/short-circuit detection feature is to monitor the voltage at point A (which appears due to the phase current flowing into \(R_{CSR}\)). If the sensed voltage exceeds the short-circuit detector reference voltage \(V_{CSCREF}\) (typ. 0.5 V), this indicates an over-current condition and the driver outputs are turned off.

For example, if \(R_{CSC} = 1 \text{ m} \Omega\), the driver will activate the short circuit protection for a phase current exceeding 500 A (\(1 \text{ m} \Omega \times 500 \text{ A} = 0.5 \text{ V} \geq V_{CSCREF}\)).

![Figure 47. Input Circuit of the Overcurrent/Short–circuit Protection Block](image)

A voltage divider that could lower the voltage at the CSC pin (at point B in Figure 47). To minimize the voltage difference, a value of 1 k\(\Omega\) is recommended for \(R_{CSCEXT}\). As a result, the voltage at point B (or CSC pin) will be \(R_{CSCEXT} / (R_{CSCEXT} + R_{CSCIN}) \approx 0.005 \text{ k} \Omega / (200 \text{ k} \Omega + 1 \text{ k} \Omega)\), which is only 0.5% lower than at point A.

An over-current condition must last for a minimum duration of \(t_{CSCFLT}\) (typ. 300 ns) to trigger the short-circuit protection. This duration has been defined to provide adequate noise filtering against high frequency noises during IGBT switching. If this time is not sufficient, an additional capacitor can be placed at the input of the CSC pin to further extend the filtering time.

Upon detection of a short circuit through the CSC pin:
- the high side output turns off immediately;
- the low side driver output initiates a soft shutdown to turn off the low side IGBT slowly to prevent it from entering the avalanche mode;
- the Fault Output (FO) pin generates a fault signal for a duration of \(t_{FO}\) (typ. 60 \(\mu\)s).

Please note that once the FO is triggered, the driver outputs can be reactivated on the next rising edge of input signal only after the duration of \(t_{FO}\) has passed.

Layout Considerations

For optimum performance, considerations must be taken during printed circuit board (PCB) layout.

Power Supply Bypass Capacitors

The implementation of bypass capacitors is essential to optimal operation of gate drivers like FAD8253 and so, special attention is required.

The local bypass capacitor between \(V_{DD}\) and \(V_{SS}\) needs to provide pulsed currents for the low side driver output. At the same time, if a high-side bootstrap circuit is employed, it has to rapidly charge the bootstrap capacitor as well.

A typical criterion for choosing the value of bypass capacitor is to keep the ripple voltage on the supply pin to \(\leq 5\%\). Typically, two capacitors in parallel are recommended. Often, a capacitor of smaller value is placed very close to the \(V_{DD}\) pin in parallel with another capacitor of higher value to reduce impedance. For sizing of the bootstrap capacitor please refer to application note AN–6076.

Gate–Drive Loop

Current loops behave like antennae, able to receive and transmit noise. To reduce the noise coupling/emission and improve the power switch turn–on and off performance, gate–drive loops must be reduced as much as possible.

Ground Plane

To minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.
NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

SOLDERING FOOTPRINT*

**For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “*”, may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**
### STYLE 1:
- **PIN 1**: COMMON CATHODE
- **PIN 2**: ANODE/CATHODE
- **PIN 3**: ANODE/CATHODE
- **PIN 4**: NO CONNECTION
- **PIN 5**: ANODE/CATHODE
- **PIN 6**: NO CONNECTION
- **PIN 7**: ANODE/CATHODE
- **PIN 8**: ANODE/CATHODE
- **PIN 9**: ANODE/CATHODE
- **PIN 10**: NO CONNECTION
- **PIN 11**: ANODE/CATHODE
- **PIN 12**: ANODE/CATHODE
- **PIN 13**: NO CONNECTION
- **PIN 14**: COMMON ANODE

### STYLE 2:
- **PIN 1**: NO CONNECTION
- **CANCELLED**

### STYLE 3:
- **PIN 1**: NO CONNECTION
- **PIN 2**: ANODE/CATHODE
- **PIN 3**: ANODE/CATHODE
- **PIN 4**: NO CONNECTION
- **PIN 5**: ANODE/CATHODE
- **PIN 6**: NO CONNECTION
- **PIN 7**: ANODE/CATHODE
- **PIN 8**: ANODE/CATHODE
- **PIN 9**: ANODE/CATHODE
- **PIN 10**: NO CONNECTION
- **PIN 11**: ANODE/CATHODE
- **PIN 12**: ANODE/CATHODE
- **PIN 13**: NO CONNECTION
- **PIN 14**: COMMON ANODE

### STYLE 4:
- **PIN 1**: NO CONNECTION
- **PIN 2**: CATHODE
- **PIN 3**: CATHODE
- **PIN 4**: NO CONNECTION
- **PIN 5**: CATHODE
- **PIN 6**: NO CONNECTION
- **PIN 7**: CATHODE
- **PIN 8**: CATHODE
- **PIN 9**: CATHODE
- **PIN 10**: CATHODE
- **PIN 11**: CATHODE
- **PIN 12**: CATHODE
- **PIN 13**: NO CONNECTION
- **PIN 14**: COMMON CATHODE

### STYLE 5:
- **PIN 1**: COMMON CATHODE
- **PIN 2**: ANODE/CATHODE
- **PIN 3**: ANODE/CATHODE
- **PIN 4**: NO CONNECTION
- **PIN 5**: ANODE/CATHODE
- **PIN 6**: NO CONNECTION
- **PIN 7**: ANODE/CATHODE
- **PIN 8**: ANODE/CATHODE
- **PIN 9**: ANODE/CATHODE
- **PIN 10**: NO CONNECTION
- **PIN 11**: ANODE/CATHODE
- **PIN 12**: ANODE/CATHODE
- **PIN 13**: NO CONNECTION
- **PIN 14**: COMMON CATHODE

### STYLE 6:
- **PIN 1**: CATHODE
- **PIN 2**: CATHODE
- **PIN 3**: CATHODE
- **PIN 4**: NO CONNECTION
- **PIN 5**: CATHODE
- **PIN 6**: NO CONNECTION
- **PIN 7**: CATHODE
- **PIN 8**: CATHODE
- **PIN 9**: CATHODE
- **PIN 10**: CATHODE
- **PIN 11**: CATHODE
- **PIN 12**: CATHODE
- **PIN 13**: NO CONNECTION
- **PIN 14**: COMMON ANODE

### STYLE 7:
- **PIN 1**: ANODE/CATHODE
- **PIN 2**: COMMON ANODE
- **PIN 3**: COMMON CATHODE
- **PIN 4**: NO CONNECTION
- **PIN 5**: ANODE/CATHODE
- **PIN 6**: NO CONNECTION
- **PIN 7**: ANODE/CATHODE
- **PIN 8**: ANODE/CATHODE
- **PIN 9**: ANODE/CATHODE
- **PIN 10**: ANODE/CATHODE
- **PIN 11**: NO CONNECTION
- **PIN 12**: ANODE/CATHODE
- **PIN 13**: ANODE/CATHODE
- **PIN 14**: COMMON CATHODE

### STYLE 8:
- **PIN 1**: COMMON CATHODE
- **PIN 2**: ANODE/CATHODE
- **PIN 3**: ANODE/CATHODE
- **PIN 4**: NO CONNECTION
- **PIN 5**: ANODE/CATHODE
- **PIN 6**: ANODE/CATHODE
- **PIN 7**: COMMON ANODE
- **PIN 8**: COMMON CATHODE
- **PIN 9**: ANODE/CATHODE
- **PIN 10**: ANODE/CATHODE
- **PIN 11**: NO CONNECTION
- **PIN 12**: ANODE/CATHODE
- **PIN 13**: ANODE/CATHODE
- **PIN 14**: COMMON CATHODE