FAD6263

Product Preview
Half-Bridge Gate Driver, 600 V, 3 A

Description
The FAD6263 is a high voltage half bridge gate driver IC providing 2 complementary outputs for driving power MOSFETs or IGBTs in a half-bridge configuration.

It uses the bootstrap technique to ensure a proper drive of the high-side power switch. The driver works with a single input.

Features
- Complementary High and Low Drive Outputs
- Shoot-Through Protection with adjustable Dead-Time
- High Voltage Range: Up to 600 V
- DV/dt Immunity ±50 V/ns
- Matched Propagation Delay 100 ns
- Gate Drive Supply Range from 10 V to 22 V
- Output Source / Sink Current Capability 3 A / 3 A
- 3.3 V and 5 V Input Logic Pins
- Extended Allowable Negative Bridge Pin Voltage Swing to –10 V for Signal Propagation
- Under Voltage LockOut (UVLO) for Both Channels
- Shutdown Pin with Latched Fault State
- AEC–Q100 Qualified and PPAP Capable
- This Device is Pb–Free, Halogen Free and is RoHS Compliant

Applications
- Automotive
- Motor Control (fans, pumps, compressors)
- MOSFET and IGBT driver applications

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.
Figure 1. Application Schematic – SOIC16

Figure 2. Simplified Block Diagram
Table 1. PIN FUNCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN</td>
<td>Logic Input for Complementary Outputs</td>
</tr>
<tr>
<td>2</td>
<td>SD</td>
<td>Logic Input Shutdown (Active Low)</td>
</tr>
<tr>
<td>3</td>
<td>SR</td>
<td>Shutdown Reset</td>
</tr>
<tr>
<td>4</td>
<td>DT</td>
<td>Dead-Time Control with External Resistor (referenced to VSS)</td>
</tr>
<tr>
<td>5</td>
<td>VSS</td>
<td>Logic Ground</td>
</tr>
<tr>
<td>6</td>
<td>COM</td>
<td>Power Ground, Low–Side Driver Return</td>
</tr>
<tr>
<td>7</td>
<td>VDD</td>
<td>Low–Side and Logic Power Supply Voltage</td>
</tr>
<tr>
<td>8</td>
<td>LOP</td>
<td>Low–Side Driver Output (Pull Up)</td>
</tr>
<tr>
<td>9</td>
<td>LON</td>
<td>Low–Side Driver Output (Pull Down)</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td>No Electrical Connection (Note 1)</td>
</tr>
<tr>
<td>11</td>
<td>NC</td>
<td>No Electrical Connection (Note 1)</td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
<td>No Electrical Connection (Note 1)</td>
</tr>
<tr>
<td>13</td>
<td>VS</td>
<td>High–Side Floating Supply Return</td>
</tr>
<tr>
<td>14</td>
<td>HON</td>
<td>High–Side Driver Output (Pull Down)</td>
</tr>
<tr>
<td>15</td>
<td>HOP</td>
<td>High–Side Driver Output (Pull Up)</td>
</tr>
<tr>
<td>16</td>
<td>VB</td>
<td>High–Side Floating Supply</td>
</tr>
</tbody>
</table>

1. The lead and the silicon die are not electrically connected. Printed circuit board traces are allowable.
### Table 2. MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>High–Side Floating Supply Voltage</td>
<td>$V_B$</td>
<td>−0.3 to 625 V</td>
<td>V</td>
</tr>
<tr>
<td>High–Side Floating Offset Voltage</td>
<td>$V_S$</td>
<td>$(V_B - 25)$ to $(V_B + 0.3)$ V</td>
<td></td>
</tr>
<tr>
<td>High–Side Floating Output Voltage</td>
<td>$V_{HO}$</td>
<td>$(V_S - 0.3)$ to $(V_B + 0.3)$ V</td>
<td></td>
</tr>
<tr>
<td>Low–Side and Logic–Fixed Supply Voltage</td>
<td>$V_{DD}$</td>
<td>−0.3 to 25 V</td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Voltage (IN, SD, SR)</td>
<td>$V_{IN}$</td>
<td>−0.3 to $(V_{DD} + 0.3)$ V</td>
<td></td>
</tr>
<tr>
<td>Programmable Dead–Time Pin Voltage</td>
<td>$DT$</td>
<td>−0.3 to $(V_{DD} + 0.3)$ V</td>
<td></td>
</tr>
<tr>
<td>Low–Side Output Voltage</td>
<td>$V_{LO}$</td>
<td>$(COM - 0.3)$ to $(V_{DD} + 0.3)$ V</td>
<td></td>
</tr>
<tr>
<td>Power Ground</td>
<td>$COM$</td>
<td>$(V_{DD} - 25)$ to $(V_{DD} + 0.3)$ V</td>
<td></td>
</tr>
<tr>
<td>Allowable Offset Voltage Slew Rate</td>
<td>$dV_S/dt$</td>
<td>50 V/ns</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation (Note 2)</td>
<td>$P_D$</td>
<td>0.86 W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, Junction–to–Ambient (Do not exceed PD under any circumstances Note 3)</td>
<td>$\theta_{JA}$</td>
<td>145 °C/W</td>
<td></td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_{J(max)}$</td>
<td>150 °C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$TSTG$</td>
<td>−55 to 150 °C</td>
<td></td>
</tr>
<tr>
<td>ESD Capability, Human Body Model (Note 4)</td>
<td>$ESDHBM$</td>
<td>2 kV</td>
<td></td>
</tr>
<tr>
<td>ESD Capability, Charged Device Model (Note 4)</td>
<td>$ESDCDM$</td>
<td>2 kV</td>
<td></td>
</tr>
<tr>
<td>Moisture Sensitivity Level</td>
<td>$MSL$</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Lead Temperature Soldering Reflow (SMD Styles Only), Pb–Free Versions (Note 5)</td>
<td>$T_{SLD}$</td>
<td>260 °C</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Do not exceed $P_D$ under any circumstances.
3. Refer to the following standards:
   - JESD51–2: Integral circuits thermal test method environmental conditions – natural convection
   - JESD51–3: Low effective thermal conductivity test board for leaded surface mount packages
4. This device series incorporates ESD protection and is tested by the following methods:
   - ESD Human Body Model tested per ANSI/ESDA/JEDEC JS–001–2012
   - ESD Charged Device Model tested per JESD22–C101
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### Table 3. RECOMMENDED OPERATING RANGES

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>High–Side $V_S$ Floating Offset Voltage (Note 6)</td>
<td>$V_S$</td>
<td>5 – $V_{BS}$</td>
<td>600 V</td>
<td>V</td>
</tr>
<tr>
<td>High–side $V_{BS}$ Bootstrap Voltage</td>
<td>$V_{BS}$</td>
<td>$V_{BSUV}+$</td>
<td>22 V</td>
<td>V</td>
</tr>
<tr>
<td>High–Side Output Voltage</td>
<td>$V_{HO}$</td>
<td>$V_S$</td>
<td>$V_B$</td>
<td>V</td>
</tr>
<tr>
<td>Low–Side and Logic Supply Voltage</td>
<td>$V_{DD}$</td>
<td>$V_{DDUV}+$</td>
<td>22 V</td>
<td>V</td>
</tr>
<tr>
<td>Low–Side Output Voltage</td>
<td>$V_{LO}$</td>
<td>COM</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Voltage (IN, SD, SR)</td>
<td>$V_{IN}$</td>
<td>$V_{SS}$</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>Programmable Dead–Time Pin Voltage</td>
<td>$DT$</td>
<td>$V_{SS}$</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>Power Ground</td>
<td>$COM$</td>
<td>$V_{DD}$ – 22</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>Ambient Temperature (Note 7)</td>
<td>$T_A$</td>
<td>−40 °C</td>
<td>125 °C</td>
<td>°C</td>
</tr>
<tr>
<td>External Shutdown Input Pull–Up Resistance (Note 8)</td>
<td>$R_{SDext}$</td>
<td>3.1</td>
<td>12.4 kΩ</td>
<td></td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Recommended based on min 5 V on $V_B$, for proper operation of the level shifter circuit and ensure proper propagation of the signal from the input to the output.
7. $T_J$ does not exceed 150°C.
8. Pulled up to 5 V.
Table 4. ELECTRICAL CHARACTERISTICS

\( V_{BIAS} (V_{DD}, V_{BS}) = 15 \, V, \, V_{SS} = COM = 0 \, V, \, DT = V_{SS} \) and \( T_a = -40^\circ C \) to \( 125^\circ C \) unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER SUPPLY SECTION (V_{DD} and V_{BS})</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DD} ) and ( V_{BS} ) Supply Under Voltage Positive-going Threshold</td>
<td>( V_{DDUV}^+ ) ( V_{BSUV}^+ )</td>
<td>7.3</td>
<td>8.3</td>
<td>9.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{DD} ) and ( V_{BS} ) Supply Under Voltage Negative-going Threshold</td>
<td>( V_{DDUV}^- ) ( V_{BSUV}^- )</td>
<td>6.7</td>
<td>7.8</td>
<td>8.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{DD} ) and ( V_{BS} ) Supply Under Voltage Lockout Hysteresis Voltage</td>
<td>( V_{DDUVH} ) ( V_{BSUVH} )</td>
<td>0.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Supply Leakage Current</td>
<td>( V_B = V_S = 600 , V )</td>
<td>( I_{LK} )</td>
<td>50</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Quiescent ( V_{DD} ) Supply Current</td>
<td>( V_{IN} = 0 , V ) or ( 5 , V )</td>
<td>( I_{QDD} )</td>
<td>355</td>
<td>550</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent ( V_{BS} ) Supply Current</td>
<td>( V_{IN} = 0 , V ) or ( 5 , V )</td>
<td>( I_{QBS} )</td>
<td>45</td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating ( V_{DD} ) Supply Current</td>
<td>( V_{IN} = 0 , V ) or ( 5 , V; ) ( f_{SW} = 20 , kHz; ) ( C_L = 1 , nF )</td>
<td>( I_{PDD} )</td>
<td>1000</td>
<td>2000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating ( V_{BS} ) Supply Current</td>
<td>( V_{IN} = 0 , V ) or ( 5 , V; ) ( f_{SW} = 20 , kHz; ) ( C_L = 1 , nF )</td>
<td>( I_{PBS} )</td>
<td>700</td>
<td>1400</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>LOGIC INPUT SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic “1” Input Voltage for ( IN, SD, SR ) Threshold (Note 9)</td>
<td>( V_{IH} )</td>
<td>2.1</td>
<td>2.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic “0” Input Voltage for ( IN, SD, SR ) Threshold (Note 9)</td>
<td>( V_{IL} )</td>
<td>0.8</td>
<td>1.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Input High Bias Current</td>
<td>( V_{IN} = 5 , V )</td>
<td>( I_{IN+} )</td>
<td>20</td>
<td>40</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Logic Input Low Bias Current</td>
<td>( V_{IN} = 0 , V )</td>
<td>( I_{IN-} )</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( SD ) High Bias Current</td>
<td>( SD = 5 , V )</td>
<td>( I_{SD+} )</td>
<td>−11</td>
<td>−6</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( SD ) Low Output Voltage (Note 10)</td>
<td>10 k( \Omega ) external pull up to 5 ( V )</td>
<td>( V_{SD-} )</td>
<td>0.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic Input Pull-Down/Up Resistance</td>
<td>( R_{IN} )</td>
<td>125</td>
<td>250</td>
<td></td>
<td>k( \Omega )</td>
<td></td>
</tr>
<tr>
<td>Shutdown Input Pull-Up Resistance</td>
<td>( R_{SD} )</td>
<td>125</td>
<td>250</td>
<td></td>
<td>k( \Omega )</td>
<td></td>
</tr>
<tr>
<td>Shutdown Reset Pull-Down Resistance</td>
<td>( R_{GRES} )</td>
<td>125</td>
<td>250</td>
<td></td>
<td>k( \Omega )</td>
<td></td>
</tr>
<tr>
<td><strong>GATE DRIVER OUTPUT SECTION</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-Level Output Voltage (( V_O - V_{OH} )) for High Side and (( V_{DD} - V_{OL} )) for Low Side</td>
<td>( V_{IN} = 5 , V ) for High Side, ( V_{IN} = 0 , V ) for Low Side, No Load (( I_O = 0 , A )</td>
<td>( V_{OH} )</td>
<td>10</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Low-Level Output Voltage (( V_{OH} - V_S )) for High Side and (( V_{OL} - COM )) for Low Side</td>
<td>( V_{IN} = 0 , V ) for High Side, ( V_{IN} = 5 , V ) for Low Side, No Load (( I_O = 0 , A )</td>
<td>( V_{OL} )</td>
<td>10</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Source Peak Pulsed Current</td>
<td>( V_{OH} = 0 , V, ) Pulse Width ( \leq 10 , \mu s )</td>
<td>( I_{O+} )</td>
<td>2</td>
<td>3.3</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Sink Peak Pulsed Current</td>
<td>( V_{OH} = 15 , V, ) Pulse Width ( \leq 10 , \mu s )</td>
<td>( I_{O-} )</td>
<td>2</td>
<td>3.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Allowable Negative ( V_S ) Pin Voltage, with signal Propagation capability from ( IN ) to ( HO )</td>
<td>( V_{BS} = 15 , V )</td>
<td>( V_S )</td>
<td>−10</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Allowable Transient Negative ( V_S ) Pin Voltage, no signal propagation capability from ( IN ) to ( HO ) (Note 12)</td>
<td>( V_{BS} = 15 , V )</td>
<td>( V_S )</td>
<td>−15</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Allowable ( COM-V_{SS} ) Power/Signal Grounds Offset</td>
<td>( V_{DD} = 15 , V, V_{SS} = 0 , V )</td>
<td>COM−( V_{SS} )</td>
<td>−8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
Table 4. ELECTRICAL CHARACTERISTICS
V_{B\text{IAS}} (V_{\text{DD}, V_{\text{BS}}}) = 15 \text{ V}, V_{\text{SS}} = \text{COM} = 0 \text{ V}, DT = V_{SS} \text{ and } T_a = -40^\circ C \text{ to } 125^\circ C \text{ unless otherwise noted.}

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Condition</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DYNAMIC SECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn–On Propagation Delay (Note 10)</td>
<td>V_S = 0 V, R_{DT} = 0 \Omega, C_L = 1000 pF</td>
<td>t_{ON}</td>
<td>155</td>
<td>230</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn–Off Propagation Delay (Note 11)</td>
<td>V_S = 0 V, C_L = 1000 pF</td>
<td>t_{OFF}</td>
<td>55</td>
<td>90</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Delay Matching HO and LO Turn–On</td>
<td></td>
<td>M_{ON}</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay Matching HO and LO Turn–Off</td>
<td></td>
<td>M_{OFF}</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn–On Rise Time</td>
<td>V_S = 0 V, C_L = 1000 pF</td>
<td>t_{R}</td>
<td>10</td>
<td>23</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Dead–Time: LO Turn–Off to HO Turn–On, HO Turn–Off to LO Turn–On</td>
<td>R_{DT} = 0 \Omega</td>
<td>DT</td>
<td>85</td>
<td>120</td>
<td>160</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>R_{DT} = 200 k\Omega</td>
<td></td>
<td>0.7</td>
<td>1</td>
<td>1.5</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Dead–Time Matching:</td>
<td></td>
<td>MDT</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>75</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown Minimum Pulse Width</td>
<td></td>
<td>t_{SDMIN}</td>
<td>270</td>
<td>310</td>
<td>450</td>
<td>ns</td>
</tr>
<tr>
<td>Shutdown Reset Minimum Pulse Width</td>
<td></td>
<td>t_{SRMIN}</td>
<td>1</td>
<td>1.6</td>
<td>2.4</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>UVLO Response Time (Note 12)</td>
<td></td>
<td></td>
<td>15</td>
<td>$\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POR Settling Time after Vdd Ramp Up</td>
<td></td>
<td>t_{POR}</td>
<td>50</td>
<td>$\mu$s</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. SR Logic Input Voltage guaranteed by design.
10. The turn–on propagation delay includes the dead time.
11. Turn–off propagation applies to SD pin. See Figure 37 for timing definitions.
12. Guaranteed by design.
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. Turn–On Propagation Delay vs. Temperature

Figure 5. Turn–Off Propagation Delay vs. Temperature

Figure 6. Turn–On Rise Time vs. Temperature

Figure 7. Turn–Off Fall Time vs. Temperature

Figure 8. Dead Time ($R_{DT} = 0 \, \Omega$) vs. Temperature

Figure 9. Dead Time Matching ($R_{DT} = 0 \, \Omega$) vs. Temperature
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Figure 10. Dead Time ($R_{DT} = 200\,k\Omega$) vs. Temperature

Figure 11. Dead Time Matching ($R_{DT} = 200\,k\Omega$) vs. Temperature

Figure 12. Turn–On Delay Matching vs. Temperature

Figure 13. Turn–Off Delay Matching vs. Temperature

Figure 14. Dead Time vs. $R_{DT}$

Figure 15. Quiescent $V_{DD}$ Supply Current vs. Temperature
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Figure 16. Operating $V_{DD}$ Supply Current vs. Temperature

Figure 17. Quiescent $V_{BS}$ Supply Current vs. Temperature

Figure 18. Operating $V_{BS}$ Supply Current vs. Temperature

Figure 19. $V_{DD}$ UVLO+ vs. Temperature

Figure 20. $V_{DD}$ UVLO− vs. Temperature

Figure 21. $V_{BS}$ UVLO+ vs. Temperature
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Figure 22. $V_{BS\, UVLO-}$ vs. Temperature

Figure 23. High-Level Output Voltage vs. Temperature

Figure 24. Low-Level Output Voltage vs. Temperature

Figure 25. Logic HIGH Input Voltage vs. Temperature

Figure 26. Logic LOW Input Voltage vs. Temperature

Figure 27. Logic Input HIGH Bias Current vs. Temperature
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Figure 28. Allowable Negative $V_S$ Voltage vs. Temperature

Figure 29. Turn–on Propagation Delay vs. Supply Voltage

Figure 30. Turn–off Propagation Delay vs. Supply Voltage

Figure 31. Turn–on Rise Time vs. Supply Voltage

Figure 32. Turn–off Rise Time vs. Supply Voltage
SWITCHING TIME DEFINITIONS

Figure 33. Switching Time and Dead-Time Waveform Definition

Figure 34. Delay Matching Waveform Definition
APPLICATIONS DESCRIPTION

Power On Reset (POR) Sequence
The purpose of the POR sequence is to ensure that the logic circuitry has reached a stable state after Vdd has ramped up before the gate driver can be operated:
1. Ramp up VDD to the target operating voltage.
2. Wait during tPOR for the internal logic to settle.
3. Apply a SR pulse to ensure the LO output is activated.
4. Wait sufficient time for the bootstrap capacitor to charge.
5. Operate the device as intended.

It is recommended to keep IN low until the bootstrap capacitor is properly charged.
The POR sequence is illustrated in Figure 35.

Shut Down and Reset Signal
This section describes how to use the SD and the SR pins to shutdown the driver outputs, ie pull down all outputs independently from the input signal, and to reactivate them.
When the SR pin is pulled down, the SD pin is used to trigger a shutdown of the driver outputs and the SR pin is then used to reactivate the outputs.
The sequence with the SR pin pulled down:
• To shutdown the outputs, pull down the SD pin for a minimum duration of tSDMIN.
• After being pulled down externally, the SD pin is kept low/latched by the internal pull down transistor.
The equivalent Rdson resistance of the internal pull down transistor in latch mode is around 300 Ω
• The output of the driver remains shutdown as long as the SD pin is kept pulled down.
• The SD pin is released and the outputs are reactivated by pulling up the SR pin for a duration of tSRMIN.

Refer to Figure 36.

Operating and Reset Signal
Important note: once pulled down, the pin should not be pulled up externally otherwise:
• The HO and LO will be reactivated for the duration that SD is forced high.
• Additional current drawn by the SD pin through its internal pull down circuit will add needlessly to the total power dissipation of the IC. With equivalent Rdson resistance of 300 Ω, the internal pull down transistor in latch mode can dissipate additional 83 mW if the SD pin is forced externally to 5 V.

To prevent this situation after SD is latch to low, it is recommended to not force externally any state to SD to avoid any conflict with the internal logic of the driver. The SD must have the possibility to be pulled up by the external pull up resistor Rsdx after a pulse is given on the SR pin.
To do so, the SD could be driven by a pull up open drain circuit.

Alternate Operating Mode with SR Pin Pulled Up and SD Pin Used as Enable
When the SR pin is kept pulled up, the pin operates similar to an Enable. With the SR pin pulled up:
• When the pin is pulled down, all outputs are pulled down independently from the input pin.
• When the pin is pulled up, the outputs are activated and respond to the input pin.
Note: as long as the SR pin is pulled up, the pin does not draw any current through its internal pull down transistor. The internal pull down transistor remains open with SR pin being pulled up.

Refer to Figure 37.
Adjustable Dead time

The dead time between turn off and turn on of the opposite outputs can be adjusted with an external resistor. The relation between the resistor value and the dead time is defined in the Figure 14.

A floating DT pin would not allow any output to turn on. This pin must be connected to ground with a proper resistor.

UVLO

Two independent Under Voltage Lock Out circuitries monitor the Vbs voltage and the Vdd to Vss voltage.

- If the Vbs voltage drops below the negative going threshold voltage, then the output of the high side is pulled down.
- If the Vdd voltage drops below the negative going threshold voltage, then the output of the low side as well as the output of the high side is pulled down.

In both cases, the outputs will be reactivated at the next positive edge at the input after the Vbs/Vdd voltages reach again the positive going threshold voltage.

Note that an under voltage lockout event has no impact to the Shutdown functionality and it does not need a signal on the SR pin to reactivate the output.

Pull Up and Pull Down Outputs

The turn on and turn off speed can be defined separately without the need for a diode in the gate resistance path.

HOP and LOP are the pull up output stages that command the turn on of the power switch to drive. The value of R1 and R3 consequently impacts the turn on speed.

HON and LON are the pull down output stages that command the turn off of the power switch to drive. The value of R2 and R4 consequently impacts the turn off speed.
SOIC-16 9.90x3.90x1.50 1.27P
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ISSUE L

DATE 29 MAY 2024

NOTES:
2. DIMENSION IN MILLIMETERS, ANGLE IN DEGREES
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS

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TOLERANCE OF FORM AND POSITION

| aaa | 0.10 |
| bbb | 0.20 |
| ccc | 0.10 |
| ddd | 0.25 |
| eee | 0.10 |

RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR IR FREE STRATEGY AND SOUDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D
**MECHANICAL CASE OUTLINE**

**PACKAGE DIMENSIONS**

SOIC-16 9.90x3.90x1.50 1.27P

CASE 751B

ISSUE L

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**GENERIC MARKING DIAGRAM**

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, “G” or microdot “/C0071”, may or may not be present. Some products may not follow the Generic Marking.

**STYLE 1:**

1. COLLECTOR
2. BASE
3. COLLECTOR
4. BASE
5. EMITTER
6. BASE
7. COLLECTOR
8. BASE
9. EMITTER
10. BASE

**STYLE 2:**

1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

**STYLE 3:**

1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. BASE, #1

**STYLE 4:**

1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

**STYLE 5:**

1. DRAIN, DYE #1
2. CATHODE
3. DRAIN, #1
4. CATHODE
5. DRAIN, #2
6. CATHODE
7. DRAIN, #3
8. CATHODE
9. DRAIN, #4
10. CATHODE
11. DRAIN, #5
12. CATHODE
13. DRAIN, #6
14. CATHODE
15. DRAIN, #7
16. CATHODE

**STYLE 6:**

1. SOURCE N–CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. COMMON DRAIN (OUTPUT)
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. COMMON DRAIN (OUTPUT)
9. COMMON DRAIN (OUTPUT)
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. COMMON DRAIN (OUTPUT)
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. COMMON DRAIN (OUTPUT)

**STYLE 7:**

1. SOURCE N–CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. COMMON DRAIN (OUTPUT)
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. COMMON DRAIN (OUTPUT)
9. COMMON DRAIN (OUTPUT)
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11. COMMON DRAIN (OUTPUT)
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16. COMMON DRAIN (OUTPUT)