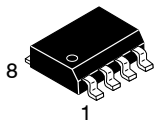
Gate Drivers, High-Speed, Low-Side, Dual 4-A

FAD3224



SOIC8
CASE 751EB

Description

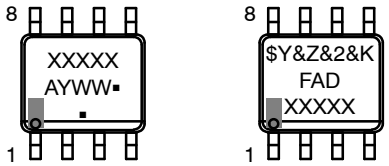
The FAD3224 4-A gate driver is designed to drive N-channel enhancement-mode MOSFETs in low-side switching applications by providing high peak current pulses during the short switching intervals. Internal circuitry provides an und-voltage lockout function by holding the output LOW until the supply voltage is within the operating range. In addition, the drivers feature matched internal propagation delays between A and B channels for applications requiring dual gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two drivers in parallel to effectively double the current capability driving a single MOSFET.

The FAD3224 has dual independent enable pins that default to ON if not connected. If one or both inputs are left unconnected, internal resistors bias the inputs such that the output is pulled LOW to hold the power MOSFET OFF.

Features

- Industry-Standard Pinouts
- 4.5 V to 30 V Operating Range
- 5 A Peak Sink / Source at V_{DD} = 12 V
- 4.3 A Sink / 2.8 A Source at V_{OUT} = 6 V
- TTL Input Thresholds
- Internal Resistors Turn Driver Off If No Inputs
- 12 ns / 9 ns Typical Rise/Fall Times (2.2 nF Load)
- Under 20 ns Typical Propagation Delay Matched within 2 ns to the Other Channel
- Double Current Capability by Paralleling Channels
- Rated from –40 °C to +125 °C Ambient
- Automotive Qualified to AEC-Q100
- FAD3224TMX with 4.5 V UVLO
- FAD3224TUMX with 9 V UVLO
- These are Pb-Free Devices

MARKING DIAGRAMS



XXX = Specific Device Code
A = Assembly Lot Code
Y = Year
WW = Work Week
▪ = Pb-Free Package

$Y = **onsemi** Logo Graphic
&Z = Assembly Plant Code
&2 = 2-Digit Date Code (Year and Week)
&K = 2-Digit Lot Run Traceability Code
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

Applications

- Switch-Mode Power Supplies
- High-Efficiency MOSFET Switching
- Synchronous Rectifier Circuits
- DC-to-DC Converters
- Motor Control
- Automotive-Qualified Systems

Related Resources

- AN-6069 - Application Review and Comparative Evaluation of Low-Side Gate Drivers

PACKAGE OUTLINES

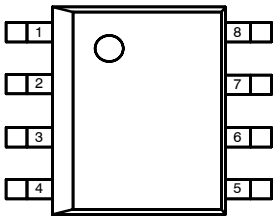


Figure 1. SOIC-8
(Top View)

THERMAL CHARACTERISTICS (Note 1)

Package	Θ_L (Note 2)	Θ_{JT} (Note 3)	Θ_{JA} (Note 4)	Ψ_{JB} (Note 5)	Ψ_{JT} (Note 6)	Unit
8-Pin Small Outline Integrated Circuit (SOIC)	38	29	150	41	2.3	°C/W

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the SOIC-8-EP package, the board reference is defined as the PCB copper connected to the thermal pad and protruding from either end of the package. For the SOIC-8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

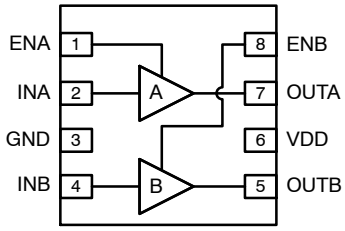


Figure 2. Pin Assignment

PIN DEFINITIONS

Name	Pin Description
ENA	Enable Input for Channel A. Pull pin LOW to inhibit driver A. ENA has TTL thresholds for INx threshold
ENB	Enable Input for Channel B. Pull pin LOW to inhibit driver B. ENB has TTL thresholds INx threshold
GND	Ground. Common ground reference for input and output circuits
INA	Input to Channel A
INB	Input to Channel B
OUTA	Gate Drive Output A: Held LOW unless required input(s) are present and V_{DD} is above UVLO threshold
OUTB	Gate Drive Output B: Held LOW unless required input(s) are present and V_{DD} is above UVLO threshold
VDD	Supply Voltage. Provides power to the IC

OUTPUT LOGIC

ENx	INx	OUTx
0	0 (Note 7)	0
0	1	0
1 (Note 7)	0 (Note 7)	0
1 (Note 7)	1	1

7. Default input signal if no external connection is made.

BLOCK DIAGRAMS

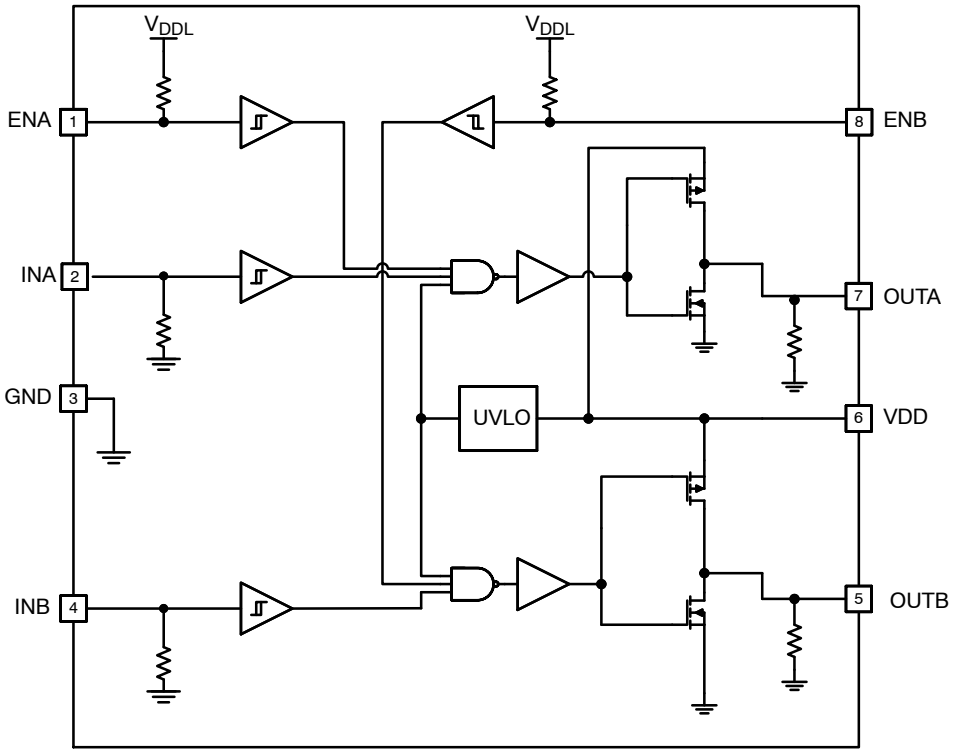


Figure 3. FAD3224 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{DD}	VDD to PGND		−0.3	33.0	V
V_{EN}	ENA and ENB to GND		GND − 10	30.0	V
V_{IN}	INA and INB to GND		GND − 10	30.0	V
V_{OUT}	OUTA and OUTB to GND	Repetitive Pulse < 200 ns (Note 8)	−2.0	V_{DD} + 0.3	V
		DC	GND − 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)		−	+260	°C
T_J	Junction Temperature		−55	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage Range	4.5	30.0	V
V_{DD}	Supply Voltage Range (FAD3224TU only)	9.5	30.0	V
V_{EN}	Enable Voltage ENA and ENB	0	28	V
V_{IN}	Input Voltage INA and INB	0	28	V
V_{OUT}	OUTA and OUTB to GND	0	V_{DD}	V
T_A	Operating Ambient Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

8. Not tested in production.

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{DD} = 12 V, T_J = −40 °C to +125 °C. Currents are defined as positive into the device and negative out of the device.)

Symbol	Parameter	Characteristic	Min	Typ	Max	Unit
SUPPLY [FAD3224T(MX)-F085]						
V_{DD}	Operating Range		4.5	–	30.0	V
I_{DD}	Supply Current, Inputs / EN Not Connected			0.70	1.20	mA
V_{ON}	Turn-On Voltage	INA = ENA = V_{DD}, INB = ENB = 0 V	3.5	3.9	4.3	V
V_{OFF}	Turn-Off Voltage	INA = ENA = V_{DD}, INB = ENB = 0 V	3.3	3.7	4.1	V
SUPPLY [FAD3224TU(MX)-F085 (Modified UVLO Version)]						
V_{DD}	Operating Range		9.5		30.0	V
I_{DD}	Supply Current, Inputs / EN Not Connected			0.70	1.20	mA
V_{ON}	Turn-On Voltage	INA = ENA = V_{DD}, INB = ENB = 0 V	8.0	9.1	10.2	V
V_{OFF}	Turn-Off Voltage	INA = ENA = V_{DD}, INB = ENB = 0 V	7.0	8.2	9.3	V
INPUTS [FAD3224(T/TU)(MX)-F085]						
V_{INL_T}	INx Logic LOW Threshold		0.8	1.2	–	V
V_{INH_T}	INx Logic HIGH Threshold		–	1.6	2.0	V
V_{HYS_T}	TTL Logic Hysteresis Voltage		–	0.4	0.9	V
I_{IN_T}	Non-inverting Input Current	IN from 0 to V_{DD}	–	–	50	μA
ENABLE [FAD3224(T/TU)(MX)-F085]						
V_{ENL}	Enable Logic Low Threshold	EN from 5 V to 0 V	0.8	1.2	–	V
V_{ENH}	Enable Logic High Threshold	EN from 0 V to 5 V	–	1.6	2.0	V
V_{HYS_T}	TTL Logic Hysteresis Voltage (Note 9)		–	0.4	–	V
R_{PU}	Enable Pull-Up Resistance (Note 10)		–	400	–	kΩ
t_{D3}	EN to Output Propagation Delay (Note 11)	0 V to 5 V EN, 1 V/ns Slew Rate	9	17	29	ns
t_{D4}		5 V to 0 V EN, 1 V/ns Slew Rate	9	17	29	ns

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{DD} = 12 V, T_J = −40 °C to +125 °C. Currents are defined as positive into the device and negative out of the device.)

Symbol	Parameter	Characteristic	Min	Typ	Max	Unit
OUTPUTS [FAD3224(T/TU)(MX)-F085]						
I_{SINK}	Out Current, Mid-Voltage, Sinking (Note 10)	OUT at V_{DD}/2, C_{LOAD} = 0.22 μF, f = 1 kHz	–	4.3	–	A
I_{SOURCE}	Out Current, Mid-Voltage, Sourcing (Note 10)	OUT at V_{DD}/2, C_{LOAD} = 0.22 μF, f = 1 kHz	–	−2.8	–	A
I_{PK_SINK}	OUT Current, Peak, Sinking (Note 10)	C_{LOAD} = 0.22 μF, f = 1 kHz	–	5	–	A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing (Note 10)	C_{LOAD} = 0.22 μF, f = 1 kHz	–	−5	–	A
t_{RISE}	Output Rise Time (Note 11)	C_{LOAD} = 2200 pF	–	12	20	ns
t_{FALL}	Output Fall Time (Note 11)	C_{LOAD} = 2200 pF	–	9	17	ns
$t_{DEL.MATCH}$	Propagation Matching Between Channels	INA = INB, OUTA and OUTB at 50% Point	–	2	4	ns
t_{D1}, t_{D2}	Output Propagation Delay, TTL Inputs (Note 11)	0 – 5 V_{IN}, 1 V/ns Slew Rate	9	17	29	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. EN inputs have TTL thresholds; refer to the ENABLE section.
10. Not tested in production.
11. See Timing Diagrams of Figures 4 and 5. The propagation tests are Guaranteed by Design.

TIMING DIAGRAMS

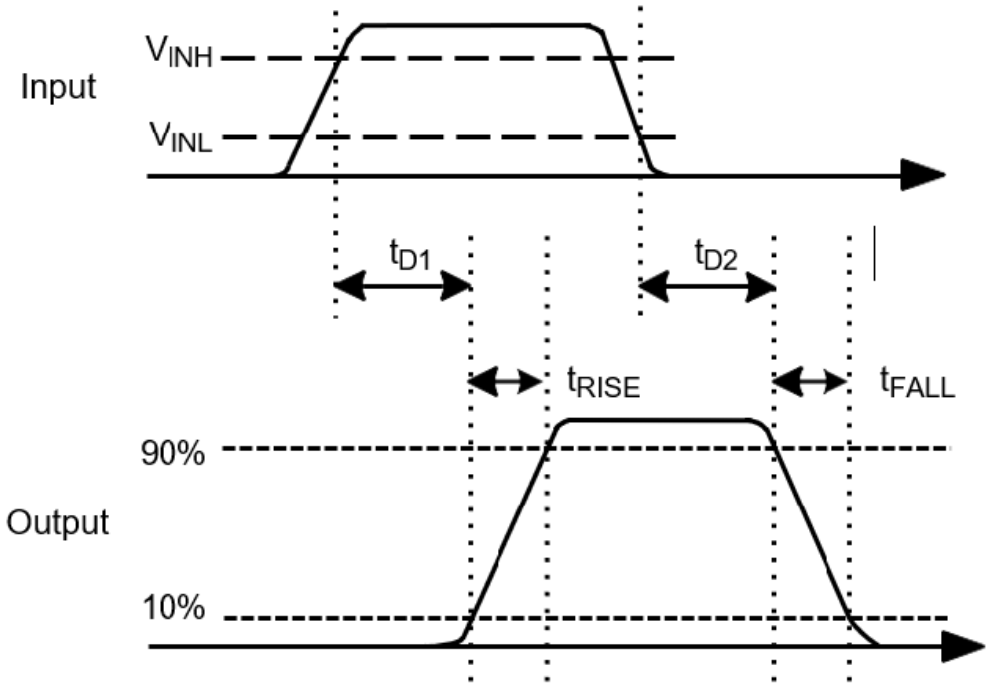


Figure 4. (EN HIGH or Floating)

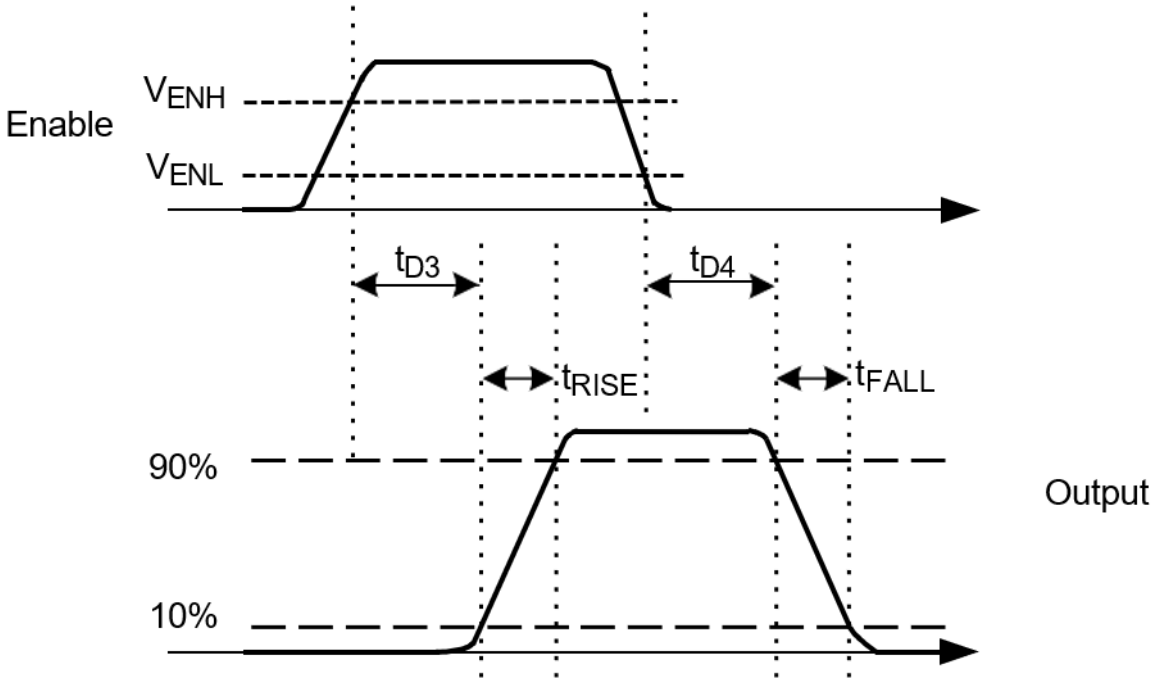


Figure 5. (IN HIGH)

TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL CHARACTERISTICS ARE PROVIDED AT 25 °C AND V_{DD} = 12 V UNLESS OTHERWISE NOTED.

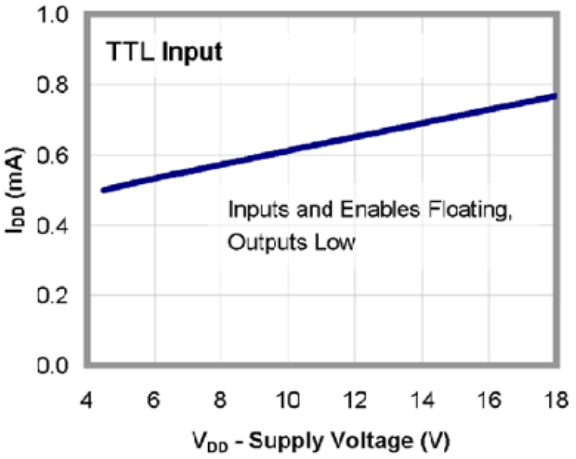


Figure 6. I_{DD} (Static) vs. Supply Voltage (Note 14)

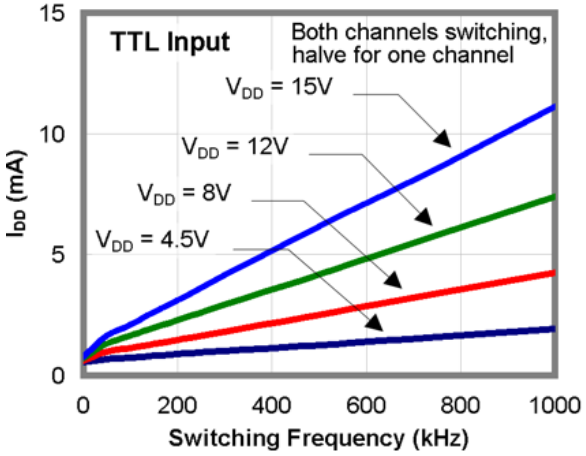


Figure 7. I_{DD} (No-Load) vs. Frequency

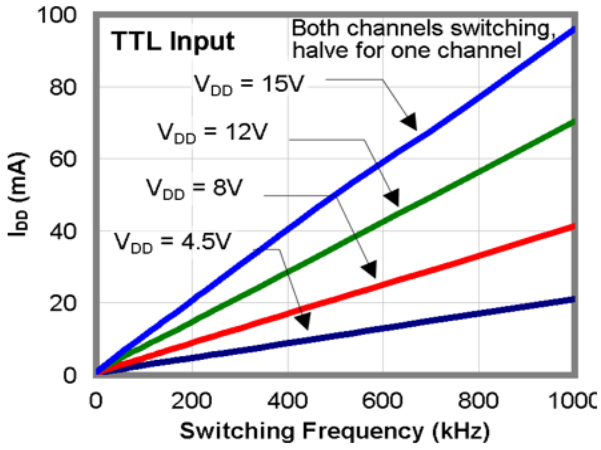


Figure 8. I_{DD} (2.2 nF Load) vs. Frequency

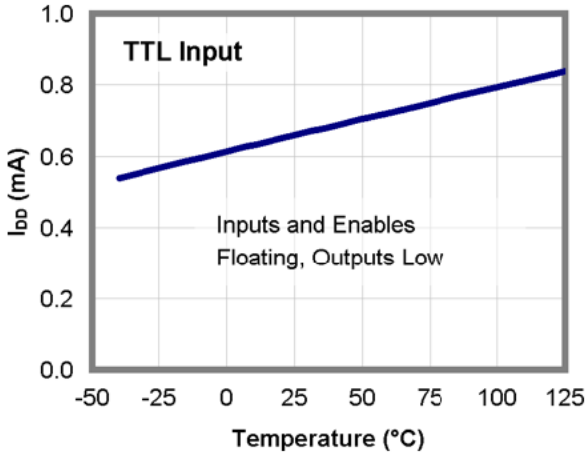


Figure 9. I_{DD} (Static) vs. Temperature (Note 14)

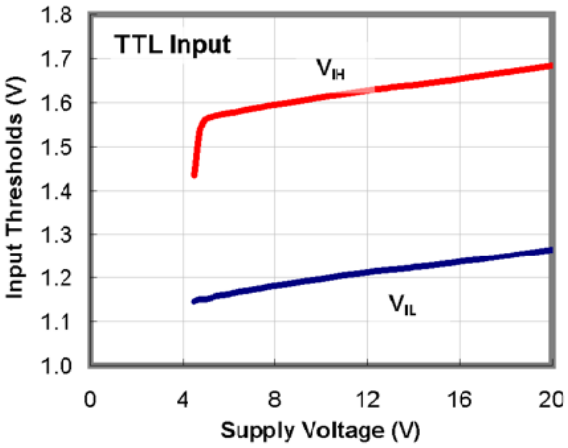


Figure 10. Input Thresholds vs. Supply Voltage

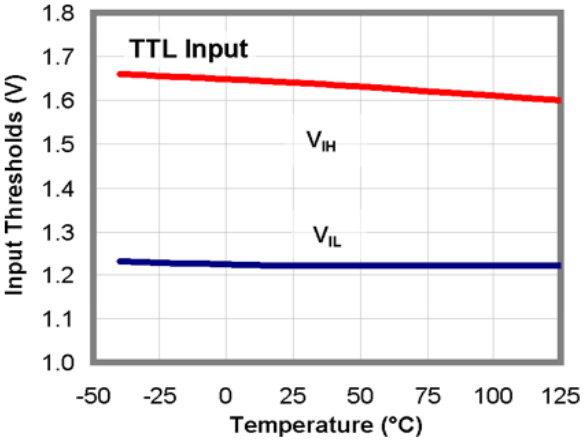


Figure 11. Input Thresholds vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL CHARACTERISTICS ARE PROVIDED AT 25 °C AND V_{DD} = 12 V UNLESS OTHERWISE NOTED. (CONTINUED)

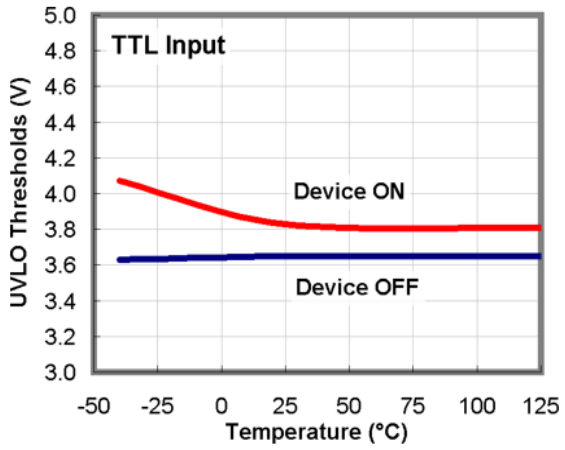


Figure 12. UVLO Threshold vs. Temperature

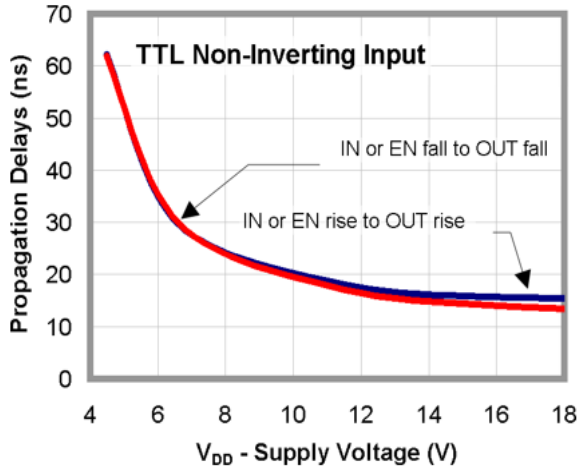


Figure 13. Propagation Delay vs. Supply Voltage

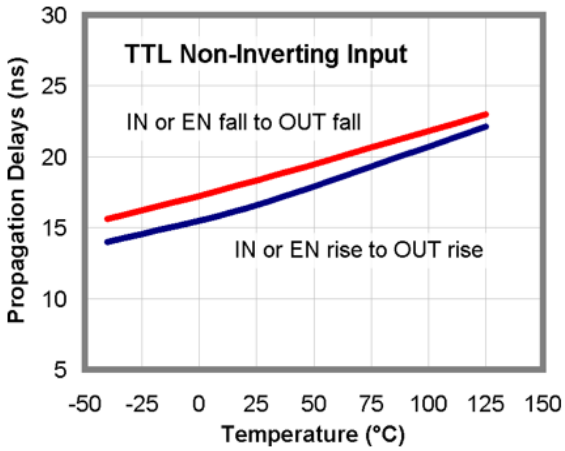


Figure 14. Propagation Delays vs. Temperature

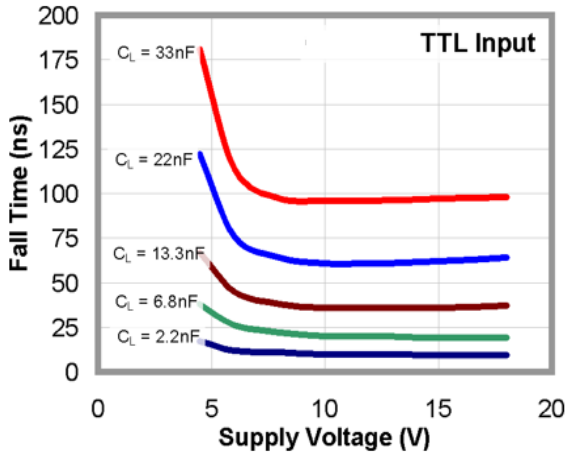


Figure 15. Fall Time vs. Supply Voltage

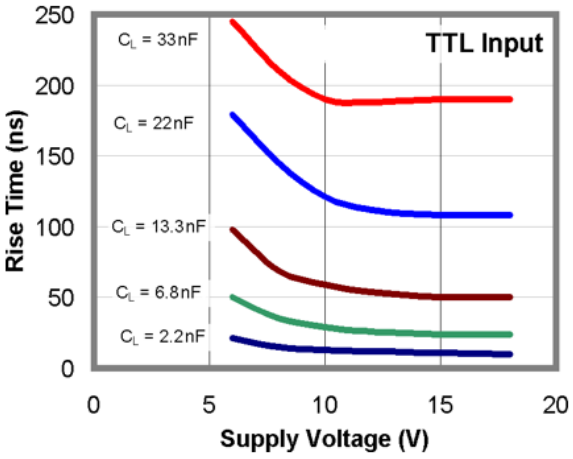


Figure 16. Rise Time vs. Supply Voltage

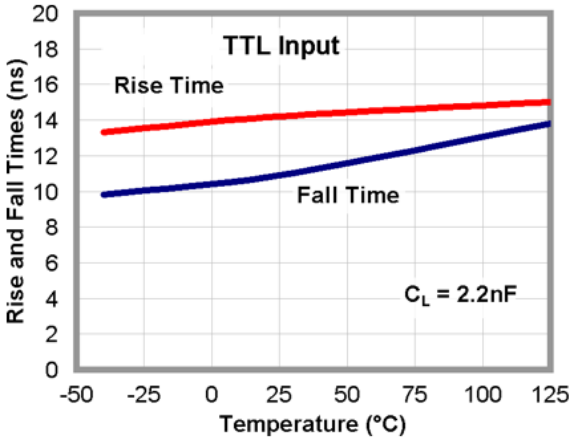


Figure 17. Rise a Fall Times vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL CHARACTERISTICS ARE PROVIDED AT 25 °C AND V_{DD} = 12 V UNLESS OTHERWISE NOTED. (CONTINUED)

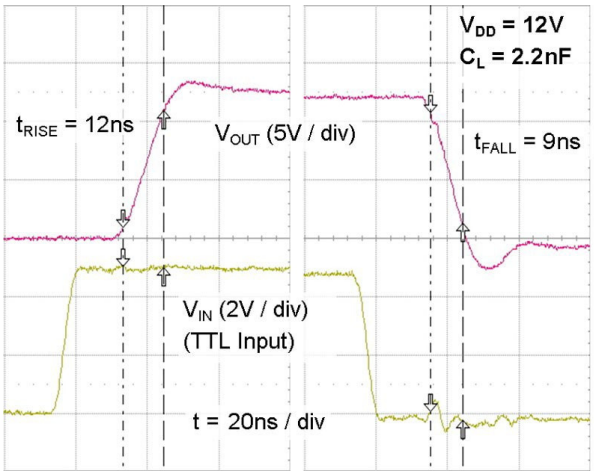


Figure 18. Rise/Fall Waveforms with 2.2 nF Load

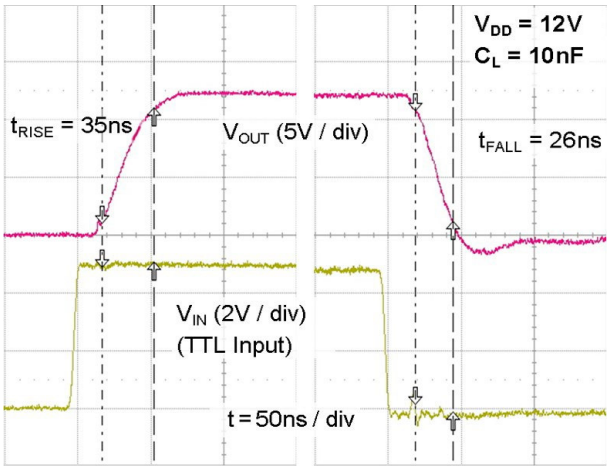


Figure 19. Rise/Fall Waveforms with 10 nF Load

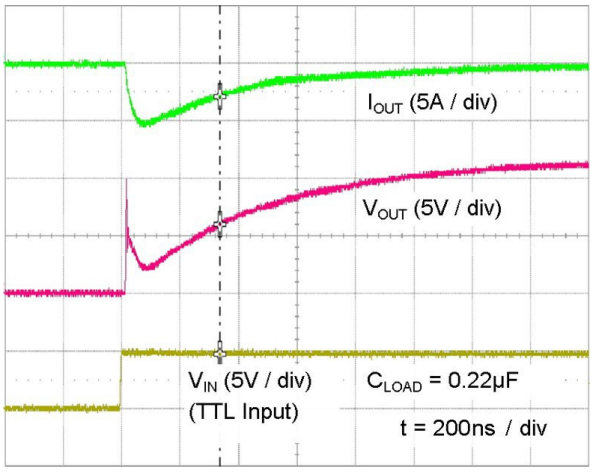


Figure 20. Quasi-Static Source Current with V_{DD} = 12 V (Note 12)

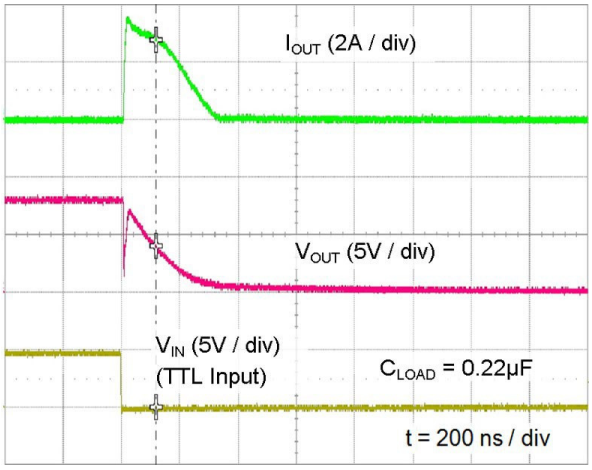


Figure 21. Quasi-Static Sink Current with V_{DD} = 12 V (Note 12)

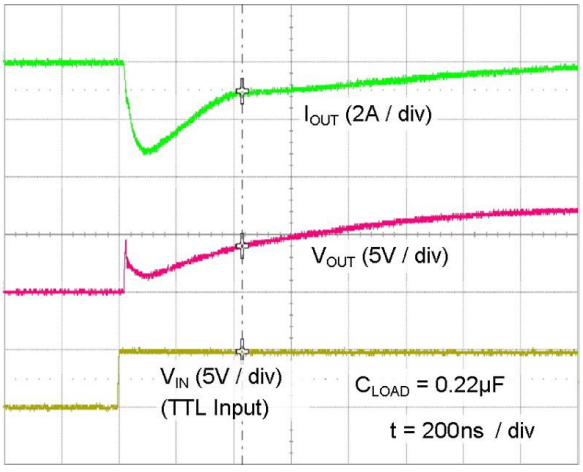


Figure 22. Quasi-Static Source Current with V_{DD} = 8 V (Note 12)

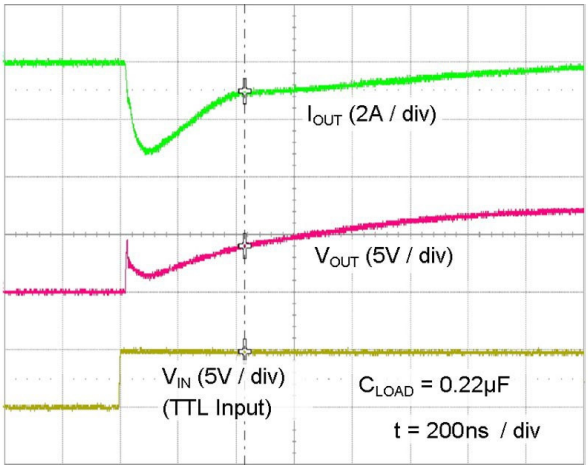


Figure 23. Quasi-Static Sink Current with V_{DD} = 8 V (Note 12)

12. The initial spike in each current waveform is a measurement artifact caused by the stray inductance of the current-measurement loop.

TEST CIRCUIT

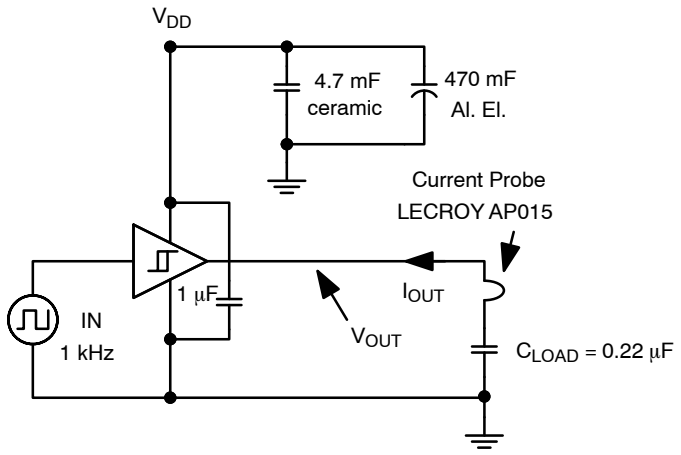


Figure 24. Quasi-Static I_{OUT} / V_{OUT} Test Circuit

APPLICATIONS INFORMATION

Input Thresholds

Each member of the FAD322x driver family consists of two identical channels that may be used independently at rated current or connected in parallel to double the individual current capacity. In the FAD3224, channels A and B can be enabled or disabled independently using ENA or ENB, respectively. The EN pin has TTL thresholds for parts with TTL input thresholds. If ENA and ENB are not connected, an internal pull-up resistor enables the driver channels by default. ENA and ENB have TTL thresholds in parts with TTL INx threshold.

If the channel A and channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB should be connected and driven together. In addition, it is recommended to include an individual gate resistance for each channel output to limit the shoot through current possibly happening between the two channels due to variations in propagation delay or in input threshold between the two channels.

The FAD3224 family offers TTL input thresholds. In the FAD3224, the input thresholds meet industry-standard TTL-logic thresholds independent of the VDD voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/µs or faster, so a rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

Static Supply Current

In the I_{DD} (static) typical performance characteristics (Figure 6 and Figure 9), the curve is produced with all inputs/enables floating (OUT is low) and indicates the lowest static I_{DD} current for the tested configuration. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs shown in the block diagram (see Figure 3). In these cases, the actual static I_{DD} current is the value obtained from the curves plus this additional current.

Under-Voltage Lockout

The FAD3224 startup logic is optimized to drive ground-referenced N-channel MOSFETs with an under-voltage lockout (UVLO) function to ensure that the IC starts up in an orderly fashion. When V_{DD} is rising, yet below the UVLO level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.2 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high-side P-channel MOSFETs because the low output voltage of the driver would turn the P-channel MOSFET ON with V_{DD} below the UVLO level.

V_{DD} Bypass Capacitor Guidelines

To enable this IC to turn a device ON quickly, a local high-frequency bypass capacitor, C_{BYP}, with low ESR and ESL should be connected between the V_{DD} and GND pins with minimal trace length. This capacitor is in addition to the bulk electrolytic capacitance of 10 μF to 47 μF commonly found on the driver and controller bias circuits. A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the VDD supply to ≤5%. This is often achieved with a value ≥20 times the equivalent load capacitance CEQV, defined here as Q_{GATE}/V_{DD}. Ceramic capacitors of 0.1 μF to 1 μF or larger are common choices, as are dielectrics, such as X5R and X7R with good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of CBYP may be increased to 50-100 times the C_{EQV}, or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10 nF mounted closest to the V_{DD} and GND pins to carry the higher frequency components of the current pulses. The bypass capacitor must provide the pulsed current from both of the driver channels and, if the drivers are switching simultaneously, the combined peak current sourced from the CB_{YP} would be twice as large as when a single channel is switching.

Layout and Connection Guidelines

The FAD3224 family of gate drivers incorporates fast-reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 4 A to facilitate voltage transition times from under 10 ns to over 150 ns. The following layout and connection guidelines are strongly recommended:

- Keep high-current output and power ground paths separate logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.
- Keep the driver as close to the load as possible to minimize the length of high-current traces. This reduces the series inductance to improve high-speed switching, while reducing the loop area that can radiate EMI to the driver inputs and surrounding circuitry.
- If the inputs to a channel are not externally connected, the internal 400 kΩ resistors indicated on block diagrams command a low output. In noisy environments, it may be necessary to tie inputs of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboard or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The FAD3224 is compatible with many other industry-standard drivers. In single input parts with enable pins, there is an internal 400 kΩ resistor tied to VDD to enable the driver by default; this should be considered in the PCB layout.
- The turn-on and turn-off current paths should be minimized, as discussed in the following section

Figure 25 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET ON. The current is supplied from the local bypass capacitor, C_{BYP}, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized CBYP acts to contain the high peak current pulses within this driver-MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

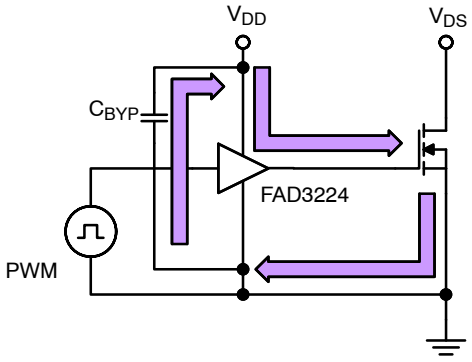


Figure 25. Current Path for MOSFET Turn-On

Figure 26 shows the current path when the gate driver turns the MOSFET OFF. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn-off times, the resistance and inductance in this path should be minimized.

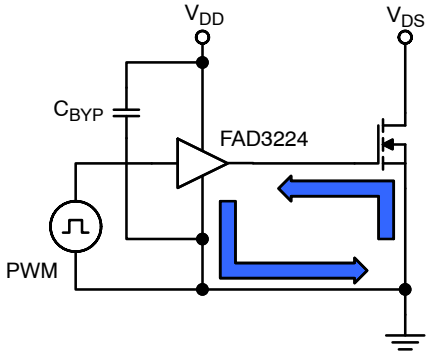


Figure 26. Current Path for MOSFET Turn-Off

Operational Waveforms

At power-up, the driver output remains LOW until the V_{DD} voltage reaches the turn-on threshold. The magnitude of the OUT pulses rises with V_{DD} until steady-state V_{DD} is reached. The non-inverting operation illustrated in Figure 27 shows that the output remains LOW until the UVLO threshold is reached, then the output is in-phase with the input.

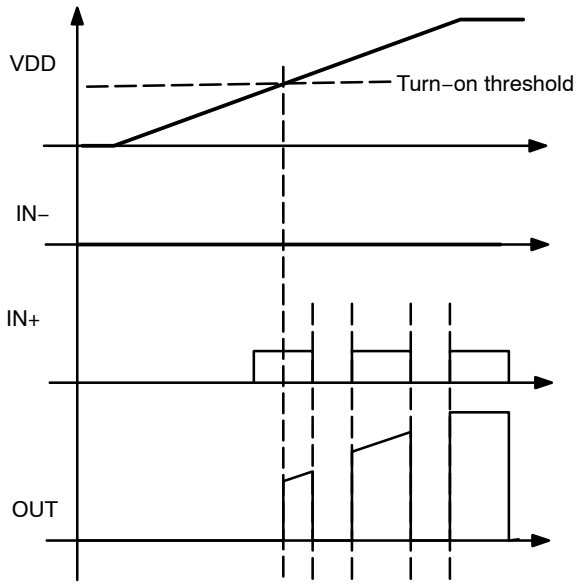


Figure 27. Startup Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad \text{(eq. 1)}$$

P_{GATE} (Gate Driving Loss): The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \times V_{GS} \times f_{SW} \times n \quad \text{(eq. 2)}$$

where n is the number of driver channels in use (1 or 2).

$P_{DYNAMIC}$ (Dynamic Pre-Drive / Shoot-through Current): A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors. The internal current consumption ($I_{DYNAMIC}$) can be estimated using the graphs in Figure 7 and Figure 8 of the Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \times V_{DD} \times n \quad \text{(eq. 3)}$$

where n is the number of driver ICs in use. Note that n is usually be one IC even if the IC has two channels, unless two or more.driver ICs are in parallel to drive a large load.

Once the power dissipated in the driver is determined, the driver junction temperature rise with respect to circuit board can be evaluated using the following thermal equation, assuming

Ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \times \psi_{JB} + T_B \quad \text{(eq. 4)}$$

where:

T_J = driver junction temperature;
Ψ_{JB} = (psi) thermal characterization parameter relating temperature rise to total power dissipation; and
T_B = board temperature in location as defined in the Thermal Characteristics table.

To give a numerical example, assume for a 12 V V_{DD} (V_{BIAS}) system, the synchronous rectifier switches of Figure 30 have a total gate charge of 60 nC at V_{GS} = 7 V. Therefore, two devices in parallel would have 120 nC gate charge. At a switching frequency of 300 kHz, the total power dissipation is:

$$P_{GATE} = 120\ nC \times 7\ V \times 300\ kHz \times 2 = 0.504\ W \quad \text{(eq. 5)}$$

$$P_{DYNAMIC} = 3.0\ mA \times 12\ V \times 1 = 0.036\ W \quad \text{(eq. 6)}$$

$$P_{TOTAL} = 0.540\ W \quad \text{(eq. 7)}$$

The SOIC-8 has a junction-to-board thermal characterization parameter of Ψ_{JB} = 42 °C/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150 °C; with 80% derating, T_J would be limited to 120 °C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120 °C:

$$T_{B,\,MAX} = T_J - P_{TOTAL} \times \psi_{JB} \quad \text{(eq. 8)}$$

$$T_{B,\,MAX} = 120°C - 0.54\ W \times 42°C/W = 97°C \quad \text{(eq. 9)}$$

TYPICAL APPLICATION DIAGRAMS

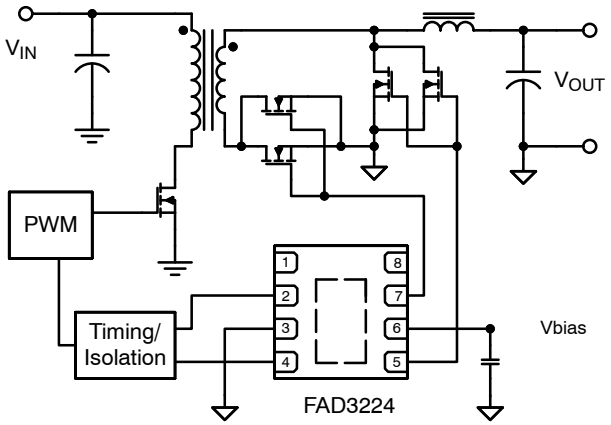


Figure 28. High Current Forward Converter with Synchronous Rectification

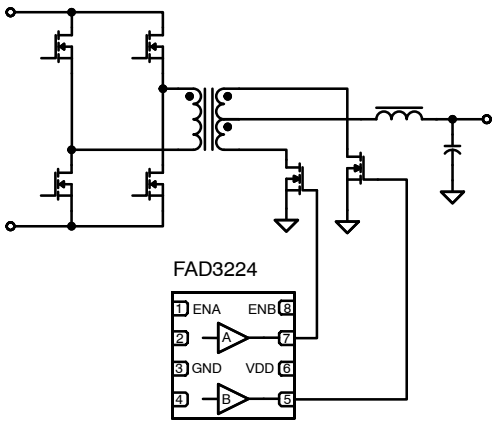


Figure 29. Center-Tapped Bridge Output with Synchronous Rectifiers

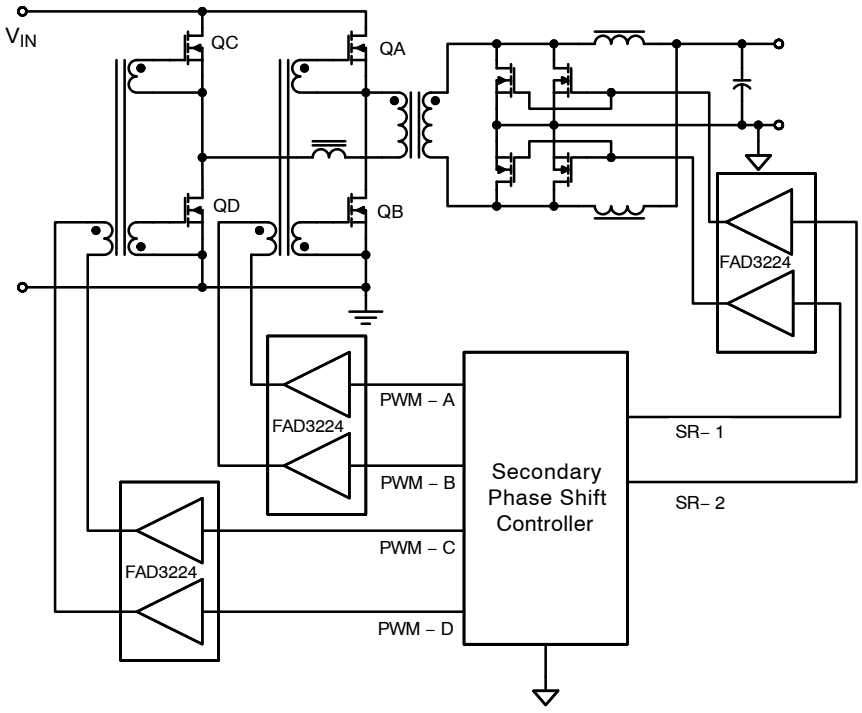


Figure 30. Secondary Controlled Full Bridge with Current Doubler Output, Synchronous Rectifiers (Simplified)

ORDERING INFORMATION

Part Number	Logic	Input Threshold	Package	Packing Method	Quantity per Reel
FAD3224TMX-F085	Dual Non-Inverting Channels + Dual Enable	TTL	SOIC-8	Tape & Reel	2,500
FAD3224TUMX-F085 (Note 13)			SOIC-8	Tape & Reel	2,500

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

13. Modified UVLO thresholds.

RELATED PRODUCTS

Type	Part Number	Gate Drive (Note 15) (Sink/Src)	Input Threshold	Logic	Package
Dual 2 A	FAN3216T	+2.4 A / −1.6 A	TTL	Dual Inverting Channels	SOIC8
Dual 2 A	FAN3217T	+2.4 A / −1.6 A	TTL	Dual Non-Inverting Channels	SOIC8
Dual 2 A	FAN3226T	+2.4 A / −1.6 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8
Dual 2 A	FAN3227C	+2.4 A / −1.6 A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8
Dual 2 A	FAN3227T	+2.4 A / −1.6 A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8
Dual 2 A	FAN3229T	+2.4 A / −1.6 A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8
Dual 2 A	FAN3268T	+2.4 A / −1.6 A	TTL	20 V Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
Dual 4 A	FAN3214T	+4.3 A / −2.8 A	TTL	Dual Non-Inverting Channels	SOIC8
Dual 4 A	FAD3224T	+4.3 A / −2.8 A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8

14. Typical currents with OUTx at 6 V and V_{DD} = 12 V.
15. Thresholds proportional to an externally supplied reference voltage.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial Data Sheet Release	9/2/2025

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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