

ESD Protection Diode

Micro-Packaged Diodes for ESD Protection

ESDL2011

The ESDL2011 is designed to protect voltage sensitive components that require low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, the part is well suited for use in high speed data line applications.

Features

- Low Capacitance 0.17 pF (Typ)
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.60 mm x 0.30 mm
- Low Body Height: 0.2 mm
- Stand-off Voltage: 1.0 V
- IEC61000-4-2 Level 4 ESD Protection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.x
- Thunderbolt 3.0

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Air Contact		±15 ±15	kV
Total Power Dissipation on FR-4 Board (Note 1) @ T _A = 25°C	P _D	313	mW
Thermal Resistance, Junction-to-Ambient	R _{θJA}	400	°C/W
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Lead Solder Temperature - Maximum (10 Second Duration)	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-4 = 28 mm² 1 oz. Cu JEDEC JESD51-3 two layer PCB.

See Application Note AND8308/D for further description of survivability specs.



DSN2
(Side wall isolated)
CASE 152AX

MARKING DIAGRAM



A = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
ESDL2011PFCT5G	DSN2 (Pb-Free)	10000 / Tape & Reel

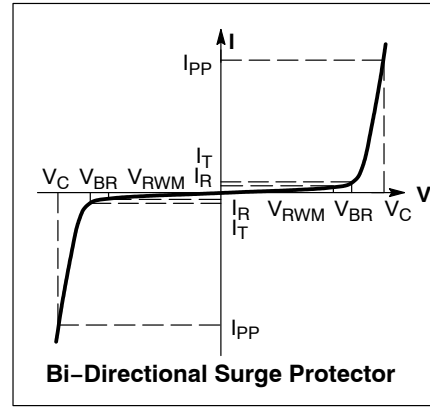
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			1.0	V
Breakdown Voltage	V_{BR}	$I_T = 1 \text{ mA}$, I/O Pin to GND	1.4	1.65	2.3	V
Reverse Leakage Current	I_R	$V_{RWM} = 1.0 \text{ V}$		30	500	nA
Clamping Voltage (Note 2)	V_C	IEC61000-4-2, $\pm 8 \text{ kV}$ Contact	Figures 1 and 2			V
Clamping Voltage 200 ns TLP	V_C	$I_{PP} = 4 \text{ A}$ } IEC61000-4-2 Level 1 Equivalent ($\pm 2 \text{ kV}$ Contact, $\pm 4 \text{ kV}$ Air)		3.5	4.0	V
		$I_{PP} = 8 \text{ A}$ } IEC61000-4-2 Level 2 Equivalent ($\pm 4 \text{ kV}$ Contact, $\pm 8 \text{ kV}$ Air)		4.8	6.0	
Reverse Peak Pulse Current per Figure 12	I_{PP}	per IEC61000-4-5 (1.2/50 μs), $R_{eq} = 12 \Omega$	3.5	4.5		A
Clamping Voltage 1.2/50 μs Waveform per Figure 12	V_C	$I_{PP} = 2.1 \text{ A}$, IEC61000-4-5 (1.2/50 μs), $R_{eq} = 12 \Omega$		2.9	3.5	V
Clamping Voltage 1.2/50 μs Waveform per Figure 12	V_C	$I_{PP} = 3.5 \text{ A}$, IEC61000-4-5 (1.2/50 μs), $R_{eq} = 12 \Omega$		3.6	4.0	V
Dynamic Resistance (TLP)	R_{DYN}	I/O Pin to GND (4 A to 8 A, 200 ns TLP)		0.34	0.5	Ω
Junction Capacitance	C_J	$V_R = 0 \text{ V}$, $f = 1 \text{ MHz}$		0.17	0.20	pF
Insertion Loss	I_L	$f = 5 \text{ GHz}$		0.165	0.20	dB
		$f = 10 \text{ GHz}$		0.34	0.40	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- For test procedure see application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: $Z_0 = 50 \Omega$, $t_p = 200 \text{ ns}$, $t_r = 4 \text{ ns}$, averaging window; $t_1 = 170 \text{ ns}$ to $t_2 = 190 \text{ ns}$.

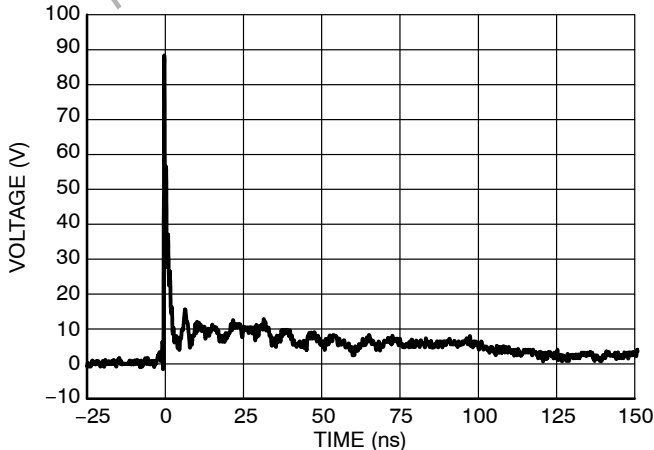


Figure 1. IEC61000-4-2 + 8 kV Contact ESD Clamping Voltage

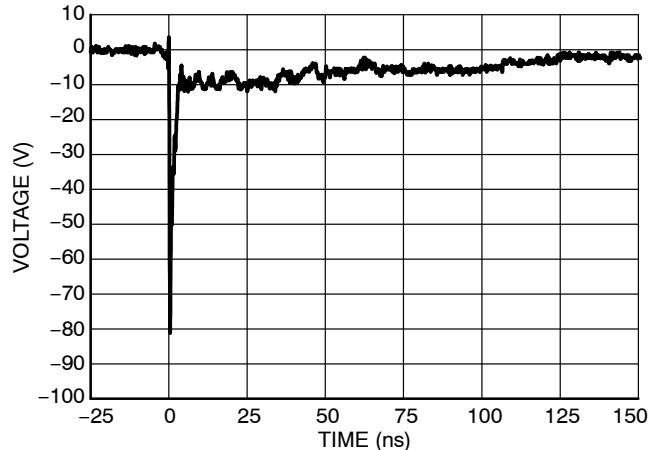


Figure 2. IEC61000-4-2 - 8 kV Contact ESD Clamping Voltage

TYPICAL CHARACTERISTICS

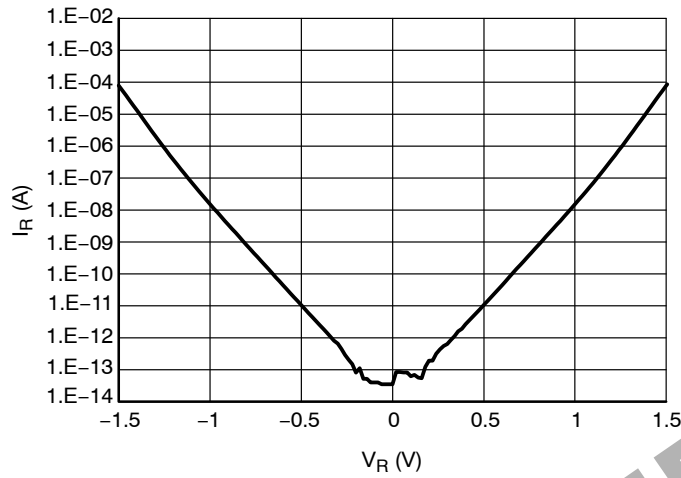


Figure 3. IV Characteristics

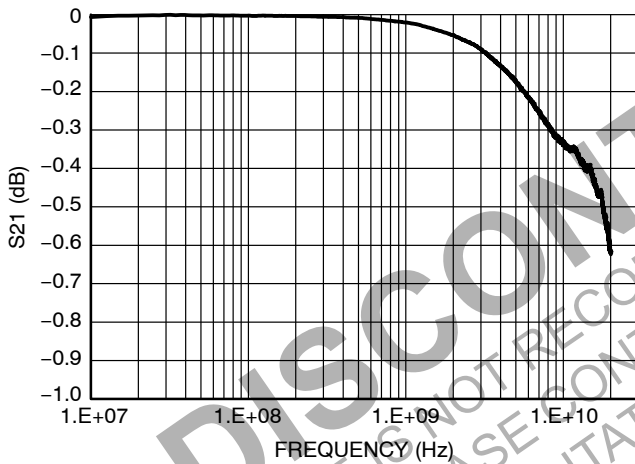


Figure 4. Insertion Loss

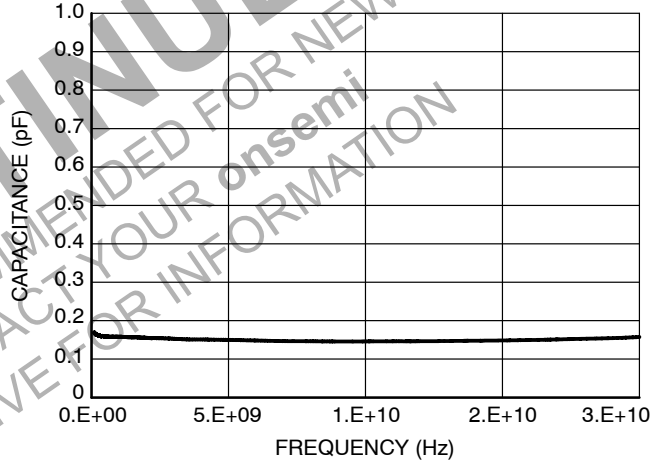


Figure 5. Typical Capacitance over Frequency

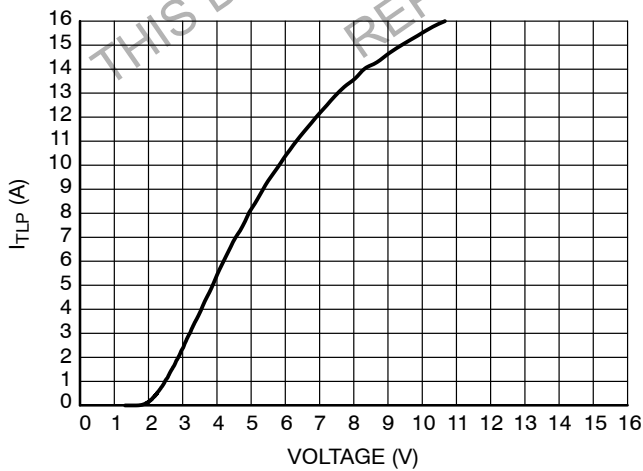


Figure 6. Positive 200 ns TLP IV Curve

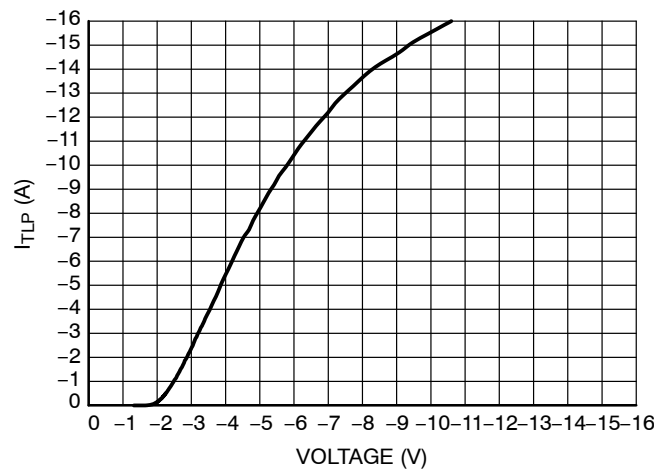


Figure 7. Negative 200 ns TLP IV Curve

TYPICAL CHARACTERISTICS

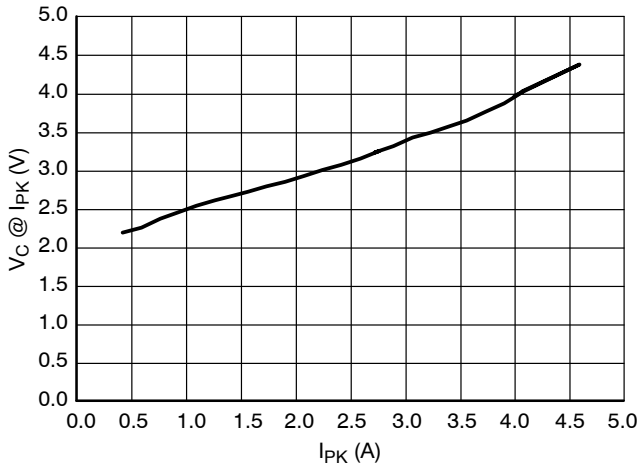


Figure 8. Positive Clamping Voltage vs. Peak Pulse Current (per IEC61000-4-5 ($t_p = 1.2/50 \mu s$, $R_{eq} = 12 \Omega$))

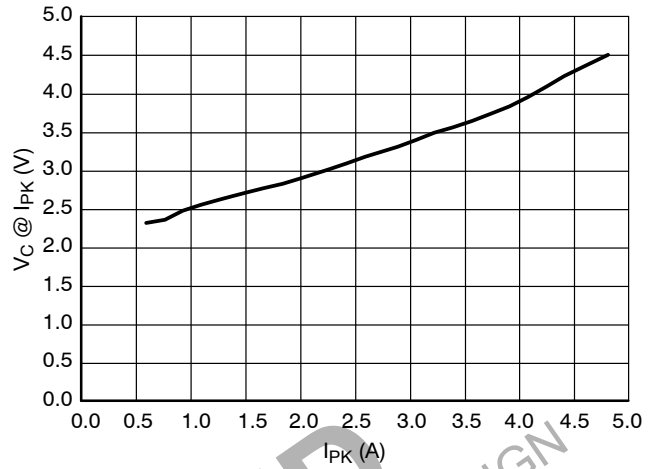


Figure 9. Negative Clamping Voltage vs. Peak Pulse Current (per IEC61000-4-5 ($t_p = 1.2/50 \mu s$, $R_{eq} = 12 \Omega$))

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi REPRESENTATIVE FOR INFORMATION

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 10. IEC61000-4-2 Spec

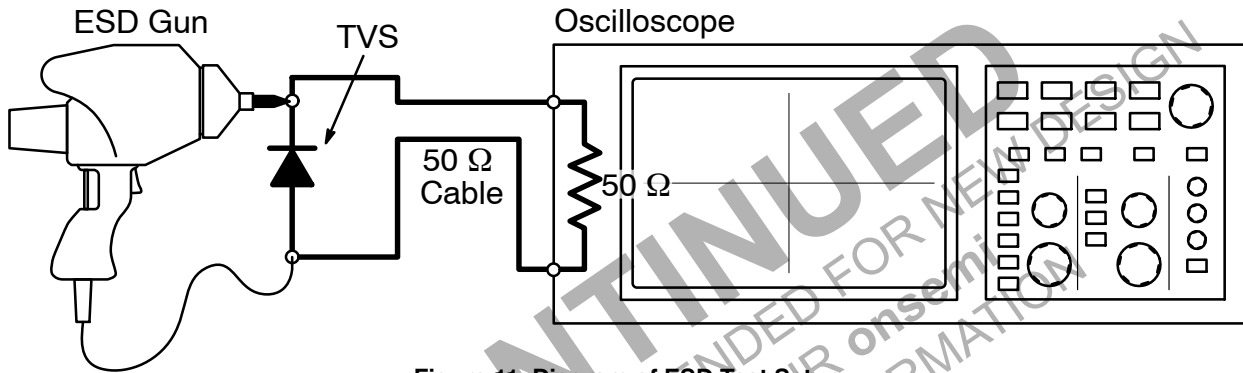


Figure 11. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not

clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

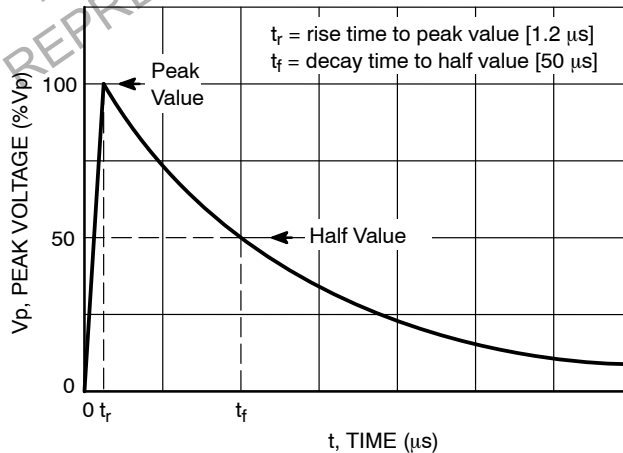
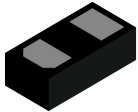
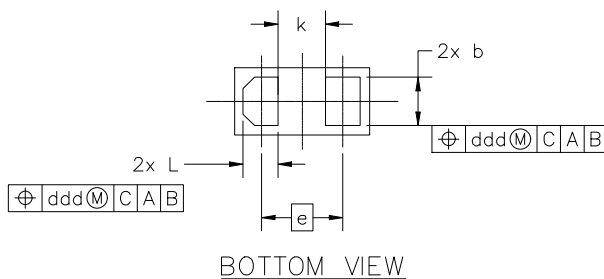
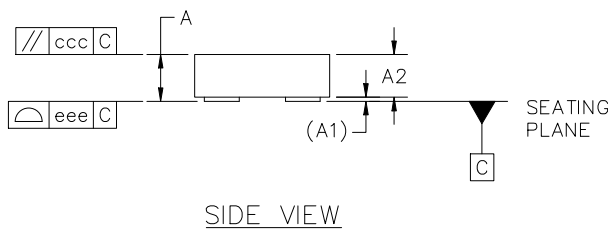
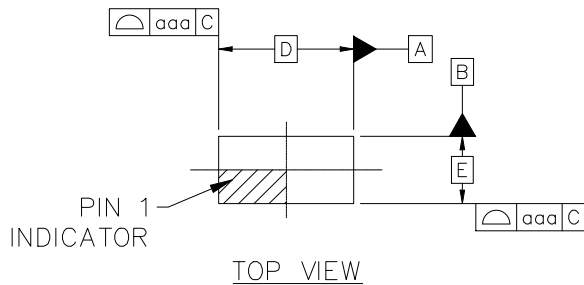


Figure 12. IEC61000-4-5 1.2/50 μs Pulse Waveform



X4DFN2, 0.60x0.30x0.19, 0.36P
CASE 152AX
ISSUE J

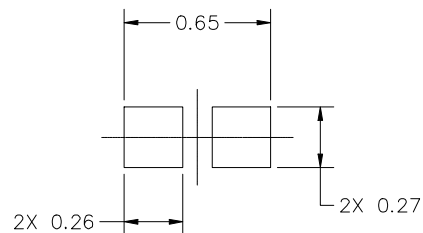
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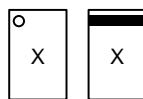
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.175	0.200	0.225
A1	0.018 REF		
A2	0.180	0.190	0.200
b	0.205	0.215	0.225
D	0.600 BSC		
E	0.300 BSC		
e	0.360 BSC		
k	0.180	---	---
L	0.145	0.155	0.165
TOLERANCE FORM AND POSITION			
aaa	0.025		
ccc	0.020		
ddd	0.050		
eee	0.010		

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.



GENERIC MARKING DIAGRAM*



X = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	X4DFN2, 0.60x0.30x0.19, 0.36P	PAGE 1 OF 1

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