STK672-740AN-E

Thick-Film Hybrid IC
2-phase Stepper Motor Driver

Overview
The STK672-740AN-E is a hybrid IC for use as a unipolar, 2-phase stepper motor driver with PWM current control.

Applications
- Office photocopiers, printers, etc.

Features
- Built-in overcurrent detection function, overheat detection function (output current OFF).
- FAULT signal (active low) is output when overcurrent or overheat is detected.
- Built-in power on reset function.
- Phase signal input driver activated with an active Low and incorporates a simultaneous ON prevention function.
- Supports schmitt input for 2.5V high level input.
- Incorporating a current detection resistor (0.089Ω: resistor tolerance ±2%), motor current can be set using two external resistors.
- The ENABLE pin can be used to cut output current while maintaining the excitation mode.
- Supports compatible pins with STK672-732AN-E.

Specifications

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum supply voltage 1</td>
<td>VCC max</td>
<td>No signal</td>
<td>52</td>
<td>V</td>
</tr>
<tr>
<td>Maximum supply voltage 2</td>
<td>VDD max</td>
<td>No signal</td>
<td>-0.3 to 6.0</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage</td>
<td>Vin max</td>
<td>Logic input pins</td>
<td>-0.3 to 6.0</td>
<td>V</td>
</tr>
<tr>
<td>Output current 1</td>
<td>IOP max</td>
<td>10μs 1 pulse (resistance load)</td>
<td>20</td>
<td>A</td>
</tr>
<tr>
<td>Output current 2</td>
<td>IOH max</td>
<td>VDD = 5V, More than 200Hz</td>
<td>4.0</td>
<td>A</td>
</tr>
<tr>
<td>Output current 3</td>
<td>IOF max</td>
<td>16pin Output current</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Allowable power dissipation 1</td>
<td>PdMF max</td>
<td>With an arbitrarily large heat sink, Per MOSFET</td>
<td>8.3</td>
<td>W</td>
</tr>
<tr>
<td>Allowable power dissipation 2</td>
<td>PdPK max</td>
<td>No heat sink</td>
<td>3.1</td>
<td>W</td>
</tr>
<tr>
<td>Operating substrate temperature</td>
<td>Tcmax</td>
<td></td>
<td>105</td>
<td>°C</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>Tjmax</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td></td>
<td>-40 to 125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION
See detailed ordering and shipping information on page 26 of this data sheet.
### Allowable Operating Ranges at Tc=25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating supply voltage 1</td>
<td>VCC</td>
<td>With signals applied</td>
<td>0 to 42</td>
<td>V</td>
</tr>
<tr>
<td>Operating supply voltage 2</td>
<td>VDD</td>
<td>With signals applied</td>
<td>5±5%</td>
<td>V</td>
</tr>
<tr>
<td>Input high voltage</td>
<td>VIH</td>
<td>Pins 10, 12, 13, 14, 15, 17, VDD=5±5%</td>
<td>2.5 to VDD</td>
<td>V</td>
</tr>
<tr>
<td>Input low voltage</td>
<td>VIL</td>
<td>Pins 10, 12, 13, 14, 15, 17, VDD=5±5%</td>
<td>0 to 0.8</td>
<td>V</td>
</tr>
<tr>
<td>Output current 1</td>
<td>IOH1</td>
<td>Tc=105°C, More than 200Hz, Continuous operation, duty=100%</td>
<td>3.0</td>
<td>A</td>
</tr>
<tr>
<td>Output current 2</td>
<td>IOH2</td>
<td>Tc=80°C, More than 200Hz, Continuous operation, duty=100%, See the motor current (IOH) derating curve</td>
<td>3.3</td>
<td>A</td>
</tr>
<tr>
<td>Recommended operating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>substrate temperature</td>
<td>Tc</td>
<td>No condensation</td>
<td>0 to 105</td>
<td>°C</td>
</tr>
<tr>
<td>Recommended Vref range</td>
<td>Vref</td>
<td>Tc=105°C</td>
<td>0.14 to 1.31</td>
<td>V</td>
</tr>
</tbody>
</table>

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### Electrical Characteristics at Tc=25°C, VCC=24V, VDD=5.0V *1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD supply current</td>
<td>ICCD</td>
<td>VDD=5.0V, ENABLE=Low</td>
<td>4.4</td>
<td>8.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Output average current *2</td>
<td>Ioave</td>
<td>R/L=1Ω,0.62mH in each phase</td>
<td>0.519</td>
<td>0.625</td>
<td>0.731</td>
<td>A</td>
</tr>
<tr>
<td>FET diode forward voltage</td>
<td>Vdf</td>
<td>If=1A (RL=23Ω)</td>
<td>0.83</td>
<td>1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output saturation voltage</td>
<td>Vsat</td>
<td>RL=23Ω</td>
<td>0.20</td>
<td>0.33</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Control Input pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input high voltage</td>
<td>VIH</td>
<td>Pins 10, 12, 13, 14, 15, 17</td>
<td>2.5</td>
<td>VDD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input low voltage</td>
<td>VIL</td>
<td>Pins 10, 12, 13, 14, 15, 17</td>
<td>–0.3</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>5V level input current</td>
<td>IILH</td>
<td>Pins 10, 12, 13, 14, 15, 17=5V</td>
<td>0.25</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>GND level input current</td>
<td>IILL</td>
<td>Pins 10, 12, 13, 14, 15=GND</td>
<td>10</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FAULT pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output low voltage</td>
<td>VOLF</td>
<td>Pin 16 (IOL=5mA)</td>
<td>0.25</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>5V level leakage current</td>
<td>IILF</td>
<td>Pin 16 =5V</td>
<td>10</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vref input bias current</td>
<td>IIB</td>
<td>Pin 19 =1.0V</td>
<td>10</td>
<td>15</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>PWM frequency</td>
<td>Fc</td>
<td></td>
<td>29</td>
<td>45</td>
<td>61</td>
<td>kHz</td>
</tr>
<tr>
<td>Overheat detection temperature</td>
<td>TSD</td>
<td>Design guarantee</td>
<td>144</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain-source cut-off current</td>
<td>IDSS</td>
<td>VDS=100V, Pins 2, 6, 9, 18=GND</td>
<td>1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes

*1: A fixed-voltage power supply must be used.
*2: The value for Ioave assumes that the lead frame of the product is soldered to the mounting circuit board.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
Notes

- The current range given above represents conditions when output voltage is not in the avalanche state.
- If the output voltage is in the avalanche state, see the allowable avalanche energy for STK672-7** series hybrid ICs given in a separate document.
- The operating substrate temperature, Tc, given above is measured while the motor is operating. Because Tc varies depending on the ambient temperature, Ta, the value of IOH, and the continuous or intermittent operation of IOH, always verify this value using an actual set.
- The Tc temperature should be checked in the center of the metal surface of the product package.
Measurement Circuit

(The terminal which is not appointed is open. The measurement circuit of STK672-740AN-E is the same as STK672-732AN-E.)

1. $V_{df}$

2. $I_{ILF}, I_{ILH}, I_{ILL}, I_{IB}$

3. $V_{sat}$

4. $I_{cco}, I_{ave}, f_c, V_{OLF}$
Sample Application Circuit

Precautions

[GND wiring]
- To reduce noise on the 5V/24V system, be sure to place the GND of C01 in the circuit given above as close as possible to Pin 2 and Pin 6 of the hybrid IC.
- In addition, in order to set the current accurately, the GND side of RO2 of Vref must be connected to the shared ground terminal used by the Pin 18 (S.G) GND, P.G1 and P.G2.

[Input pins]
- If VDD is being applied, use care that each input pin does not apply a negative voltage less than -0.3V to S. GND, Pin 18. Measures must also be taken so that a voltage equal to or greater than VDD is not input.
- Do not wire by connecting the circuit pattern on the P.C.B side to Pins 4, 8, or 11 on the N.C. shown in the internal block diagram.
- Apply 2.5V high level input to pins 10, 12, 13, 14, 15, and 17.
- Since the input pins do not have built-in pull-up resistors, when the open-collector type pins 10, 12, 13, 14, 15, and 17 are used as inputs, a 1 to 20kΩ pull-up resistor (to VDD) must be used.
- At this time, use a device for the open collector driver that has output current specifications that pull the voltage down to less than 0.8V at Low level (less than 0.8V at Low level when IOL=5mA).

[Current setting Vref]
- Considering the specifications for the Vref input bias current IIB, we recommend a value 1kΩ or less for R02.
- If the motor current is temporarily reduced, the circuit given below (STK672-740AN: IOH>0.3A) is recommended.
[Setting the motor current]
The motor current, IOH, is set using the Pin 19 voltage, Vref, of the hybrid IC. Equations related to IOH and Vref are given below.

\[
V_{ref} \approx \left( \frac{RO2}{RO2+RO1} \right) \times V_{DD}(5V)
\]  \hspace{1cm} (1)

\[
IOH \approx \left( \frac{V_{ref}}{4.9} \right) \div R_s
\]  \hspace{1cm} (2)

The value of 4.9 in Equation (2) above represents the Vref voltage as divided by a circuit inside the control IC. Rs : 0.089Ω (Current detection resistor inside the hybrid IC)

[Smoke Emission Precautions]
If Pin 18 (S.G terminal) is attached to the board without using solder, overcurrent may flow into the MOSFET at VCCON (24V ON), causing the STK672-740AN-E to emit smoke because 5V circuits cannot be controlled.

In addition, as long as one of the output Pins, 1, 3, 5, or 7, is open, inductance energy stored in the motor results in electrical stress on the driver, possibly resulting in the emission of smoke.

### Input Pin Functions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Function</th>
<th>Input Conditions When Operating</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΦA</td>
<td>13</td>
<td>Phase signal input of 5pin (phase A output).</td>
<td>Low active (with a function to prevent simultaneous ON of ΦA and ΦAB, or ΦB and ΦBB.</td>
</tr>
<tr>
<td>ΦAB</td>
<td>17</td>
<td>Phase signal input of 7pin (phase AB output).</td>
<td></td>
</tr>
<tr>
<td>ΦB</td>
<td>12</td>
<td>Phase signal input of 3pin (phase B output).</td>
<td></td>
</tr>
<tr>
<td>ΦBB</td>
<td>10</td>
<td>Phase signal input of 1pin (phase BB output).</td>
<td></td>
</tr>
<tr>
<td>RESETB</td>
<td>14</td>
<td>System reset Initial state of A and BB phase excitation in the timing charts is set by switching from low to high.</td>
<td>A reset is applied by a low level</td>
</tr>
<tr>
<td>ENABLE</td>
<td>15</td>
<td>The A, AB, B, and BB outputs are turned off, and after operation is restored by returning the ENABLE pin to the high level, operation continues with the same excitation timing as before the low-level input.</td>
<td>The A, AB, B, and BB outputs are turned off by a low-level input.</td>
</tr>
</tbody>
</table>

### Output Pin Functions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Function</th>
<th>Input Conditions When Operating</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAULT</td>
<td>16</td>
<td>Monitor pin used when over-current detection or overheat detection function is activated.</td>
<td>Low level is output when detected.</td>
</tr>
</tbody>
</table>

Note : See the timing chart for the concrete details on circuit operation.
Timing Charts
2-phase excitation

VDD
Power on reset (or RESETB)
φA
φAB
φB
φBB
ENABLE
FAO
FAB
FBO
FBB

1-2 phase excitation

VDD
Power on reset (or RESETB)
φA
φAB
φB
φBB
ENABLE
FAO
FAB
FBO
FBB
1-2 phase excitation (ENABLE)

1-2 phase excitation (Hold operation results during fixed CLOCK)
Package Dimensions
unit : mm

SIP19 29.2x14.4
CASE 127CF
ISSUE O
Technical data

1. Input Pins and Functional Overview
2. STK672-740AN-E over current detection, thermal shutdown detection.
3. STK672-740AN-E Allowable Avalanche Energy
4. STK672-740AN-E Internal Loss Calculation
5. Thermal Design
6. Package Power Loss PdPK Derating Curve for the Ambient Temperature Ta
7. Example of Stepper Motor Driver Output Current Path (1-2 phase excitation)
8. Other usage notes
1. I/O Pins and Functions of the Control Block

<table>
<thead>
<tr>
<th>HIC pin</th>
<th>Pin Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>RESETB</td>
<td>System reset</td>
</tr>
<tr>
<td>15</td>
<td>ENABLE</td>
<td>Motor current OFF</td>
</tr>
<tr>
<td>16</td>
<td>FAULT</td>
<td>Overcurrent/over-heat detection output</td>
</tr>
<tr>
<td>19</td>
<td>Vref</td>
<td>Current value setting</td>
</tr>
</tbody>
</table>

Description of each pin

1-1. [RESETB (System-wide reset)]
   The reset signal is formed by the power-on reset function built into the HIC and the RESETB terminal. When activating the internal circuits of the HIC using the power-on reset signal within the HIC, be sure to connect Pin 14 of the HIC to VDD.

1-2. [ENABLE (Forcible OFF control of excitation drive output A, AB, B, and BB, and selecting operation/hold status inside the HIC)]
   ENABLE=1: Normal operation
   When ENABLE=0: Motor current goes OFF, and excitation drive output is forcibly turned OFF.
   The system clock inside the HIC stops at this time, with no effect on the HIC even if input pins other than RESET input vary. In addition, since current does not flow to the motor, the motor shaft becomes free.
   If the \( \phi_A \) to \( \phi_{BB} \) signal input used for motor rotation suddenly stops, the motor shaft may advance beyond the control position due to inertia. A SLOW DOWN setting where the \( \phi_A \) to \( \phi_{BB} \) signal input cycle gradually decreases is required in order to stop at the control position.

1-3. [FAULT]
   FAULT is an open drain output. It outputs low level when overcurrent, or overheat is detected.

1-4. [Vref (Voltage setting to be used for the current setting reference)]
   Input voltage is in the voltage range of 0.14V to 1.31V.
   The recommended Vref voltage is 0.14V or higher because the output offset voltage of Vref/4.9 amplifier cannot be controlled down to 0V.
   Note: Pin type is analog input configuration and input pull-down resistance 100 k\(\Omega\).
   The internal impedance 100 k\(\Omega\) is designed so that the increase in current is prevented while Pin 19 is open.

1-5. [Input timing]
   The control IC of the driver is equipped with a power on reset function capable of initializing internal IC operations when power is supplied. A 4V typ setting is used for power on reset. Because the specification for the MOSFET gate voltage is 5V\(\pm5\%), conduction of current to output at the time of power on reset adds electromotive stress to the MOSFET due to lack of gate voltage. To prevent electromotive stress, be sure to set ENABLE=Low while V\(\text{DD}\) which is outside the operating supply voltage, is less than 4.75V.

![Control IC power (V\(\text{DD}\)) rising edge](image)

![Control IC power on reset](image)

![RESETB signal input](image)

![ENABLE signal input](image)

![\(\phi_A \) to \(\phi_{BB} \) signal input](image)

RESETB, ENABLE, \(\phi_A \) to \(\phi_{BB} \) Signals Input Timing
1-6. [Configuration of control block I/O pins]

<Configuration of the \( \phi A, \phi AB, \phi B, \phi BB, \) ENABLE, and RESETB input pins>

Input pins 13,17,12,10,15,14pin

The input pins of this driver all use Schmitt input. Typical specifications at \( T_c=25^\circ C \) are given below. Hysteresis voltage is 0.3V (VIHa-VILa).

When rising

\[ \text{Input voltage} - 1.8V_{\text{typ}} \]

When falling

\[ \text{Input voltage} + 1.5V_{\text{typ}} \]

Input voltage specifications are as follows.

\[ V_{\text{IH}}=2.5V_{\text{min}} \]
\[ V_{\text{IL}}=0.8V_{\text{max}} \]

<Configuration of the Vref input pin>

<Configuration of the FAULT output pin>
2. Overcurrent detection, overheat detection functions

Each detection function operates using a latch system and turns output off. Because a RESET signal is required to restore output operations, once the power supply, VDD, is turned off, you must either again apply power on reset with VDDON or apply a RESETE=High→Low→High signal.

2-1.[Overcurrent detection]
This hybrid IC is equipped with a function for detecting overcurrent that arises when the motor burns out or when there is a short between the motor terminals.
Overcurrent detection occurs at 3.5A typ with the STK672-732AN-E, and 5.5A typ with the STK672-740AN-E.

Overcurrent detection begins after an interval of no detection (a dead time of 5.5μs typ) during the initial ringing part during PWM operations. The no detection interval is a period of time where overcurrent is not detected even if the current exceeds IOH.

2-2. [Overheat detection]
Rather than directly detecting the temperature of the semiconductor device, overheat detection detects the temperature of the aluminum substrate (144°C typ).
Within the allowed operating range recommended in the specification manual, if a heat sink attached for the purpose of reducing the operating substrate temperature, TC, comes loose, the semiconductor can operate without breaking. However, we cannot guarantee operations without breaking in the case of operations other than those recommended, such as operations at a current exceeding IOH max that occurs before overcurrent detection is activated.
3. Allowable Avalanche Energy Value

(1) Allowable Range in Avalanche Mode

When driving a 2-phase Stepper motor with constant current chopping using an STK672-7** Series hybrid IC, the waveforms shown in Figure 1 below result for the output current, $I_D$, and voltage, $V_{DS}$.

In the case of voltage that rises suddenly, voltage is restricted by the MOSFET $V_{DSS}$. Voltage restriction by $V_{DSS}$ results in a MOSFET avalanche. During avalanche operations, $I_D$ flows and the instantaneous energy at this time, $E_{AVL1}$, is represented by Equation (3-1).

$$E_{AVL1} = V_{DSS} \times I_{AVL} \times 0.5 \times t_{AVL}$$  \hspace{1cm} (3-1)

$V_{DSS}$: V units, $I_{AVL}$: A units, $t_{AVL}$: sec units

The coefficient 0.5 in Equation (3-1) is a constant required to convert the $I_{AVL}$ triangle wave to a square wave.

During STK672-7** Series operations, the waveforms in the figure above repeat due to the constant current chopping operation. The allowable avalanche energy, $E_{AVL}$, is therefore represented by Equation (3-2) used to find the average power loss, $P_{AVL}$, during avalanche mode multiplied by the chopping frequency in Equation (3-1).

$$P_{AVL} = V_{DSS} \times I_{AVL} \times 0.5 \times t_{AVL} \times f_c$$  \hspace{1cm} (3-2)

$f_c$: Hz units (set to the PWM frequency of 50kHz.)

For $V_{DSS}$, $I_{AVL}$, and $t_{AVL}$, be sure to actually operate the STK672-7** Series and substitute values when operations are observed using an oscilloscope.

Ex. If $V_{DSS}=110V$, $I_{AVL}=1A$, $t_{AVL}=0.2\mu s$, the result is:

$$P_{AVL}=110 \times 1 \times 0.5 \times 0.2 \times 10^{-6} \times 50 \times 10^3 = 0.55 W$$

$V_{DSS}=110 V$ is a value actually measured using an oscilloscope.

The allowable loss range for the allowable avalanche energy value, $P_{AVL}$, is shown in the graph in Figure 3. When examining the avalanche energy, be sure to actually drive a motor and observe the $I_D$, $V_{DSS}$, and $t_{AVL}$ waveforms during operation, and then check that the result of calculating Equation (3-2) falls within the allowable range for avalanche operations.
Although the waveforms during avalanche mode are given in Figure 1, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.
- Poor coupling of the motor’s phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).
- Increase in the lead inductance of the harness caused by the circuit pattern of the board and motor.
- Increases in VDSS, tAVL, and IAVL in Figure 1 due to an increase in the supply voltage from 24V to 36V.

If the factors above are negligible, the waveforms shown in Figure 1 become waveforms without avalanche as shown in Figure 2.

Under operations shown in Figure 2, avalanche does not occur and there is no need to consider the allowable loss range of PAVL shown in Figure 3.

**Figure 2 Output Current, ID, and Voltage, VDS, Waveforms 2 of the STK672-7** Series when Driving a 2-Phase Stepper Motor with Constant Current Chopping

**Figure 3 Allowable Loss Range, PAVL-IOH During STK672-740AN-E Avalanche Operations**

Note:
The operating conditions given above represent a loss when driving a 2-phase stepper motor with constant current chopping.

Because it is possible to apply 3W or more at IOH=0A, be sure to avoid using the MOSFET body diode that is used to drive the motor as a zener diode.
4. Calculating STK672-740AN-E HIC Internal Power Loss

The average internal power loss in each excitation mode of the STK672-740AN-E can be calculated from the following formulas. *1

Each excitation mode

2-phase excitation mode

\[ 2PdAVex = (V_{sat} + V_{df}) \times \left( \frac{1}{t_1 + t_2 + t_3} \right) \times IOH \times t_2 + \left( \frac{1}{t_1 + t_2 + t_3} \right) \times IOH \times (V_{sat} \times t_1 + V_{df} \times t_3) \]

1-2 Phase excitation mode

\[ 1-2PdAVex = (V_{sat} + V_{df}) \times \left( \frac{1}{t_1 + t_2 + t_3} \right) \times IOH \times t_2 + \left( \frac{1}{t_1 + t_2 + t_3} \right) \times IOH \times (V_{sat} \times t_1 + V_{df} \times t_3) \]

Motor hold mode

\[ \text{HoldPdAVex} = (V_{sat} + V_{df}) \times IOH \]

\( V_{sat} \) : Combined voltage represented by the Ron voltage drop + shunt resistor

\( V_{df} \) : Combined voltage represented by the MOSFET body diode + shunt resistor

\( t_1, t_2, \) and \( t_3 \) represent the waveforms shown in the figure below.

\( t_1 \) : Time required for the winding current to reach the set current \( (IOH) \)

\( t_2 \) : Time in the constant current control (PWM) region

\( t_3 \) : Time from end of phase input signal until inverse current regeneration is complete

For the values of \( V_{sat} \) and \( V_{df} \), be sure to substitute from \( V_{sat} \) vs \( IOH \) and \( V_{df} \) vs \( IOH \) at the setting current value \( IOH \). (See pages to follow)

Then, determine if a heat sink is necessary by comparing with the \( \Delta Tc \) vs \( Pd \) graph (see next page) based on the calculated average output loss, HIC.

For heat sink design, be sure to see ‘5. Thermal Design’.

The HIC average power, \( PdAVex \) described above, represents loss when not in avalanche mode.

To add the loss in avalanche mode, be sure to add \( PAVL \) using the formula (for average power loss, \( PAVL \), for STK672-7** during avalanche mode, described below to \( PdAVex \) described above.)

When using this IC without a fin, always check for temperature increases in the set, because the HIC substrate temperature, \( Tc \), varies due to effects of convection around the HIC.
4-2. [Calculating the average power loss, PAVL, during avalanche mode]

The allowable avalanche energy, EAVL, during fixed current chopping operation is represented by Equation (3-2) used to find the average power loss, PAVL, during avalanche mode that is calculated by multiplying Equation (3-1) by the chopping frequency.

\[ PAVL = V_{DSS} \times I_{AVL} \times 0.5 \times t_{AVL} \times f_c \]  \hspace{1cm} (3-2)

\( f_c \) : Hz units (fc is set to the PWM frequency of 50kHz.)

Be sure to actually operate an STK672-7** series and substitute values found when observing operations on an oscilloscope for \( V_{DSS} \), \( I_{AVL} \), and \( t_{AVL} \).

The sum of PAVL values for each excitation mode is multiplied by the constants given below and added to the average internal HIC loss equation, except in the case of 2-phase excitation.

- 1-2 excitation mode and higher: \( PAVL(1) = 0.7 \times PAVL \)  \hspace{1cm} (4-1)
- During 2-phase excitation mode and motor hold: \( PAVL(1) = 1 \times PAVL \)  \hspace{1cm} (4-2)
STK672-740AN-E Output Saturation Voltage $V_{sat}$ vs. Output Current

STK672-740AN-E Forward voltage, $V_{df}$ - Output current, IOH

Substrate temperature rise, $\Delta T_c$ (no heat sink) - Internal average power dissipation, $P_{dAV}$
5. Thermal design

[Operating range in which a heat sink is not used]
Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.
The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC.
The value of PdAV increases as the output current increases. To calculate PdAV, refer to “Calculating Internal HIC Loss” in the specification document.
Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations,

\[ P_{dAV} = \frac{T_1 \times P_1 + T_2 \times P_2 + T_3 \times 0}{T_0} \]  

(Here, P1 is the PdAV for IO1 and P2 is the PdAV for IO2)

If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]
Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of \( \theta_{c-a} \) in Equation (II) below and the graph depicted in Figure 3.

\[ \theta_{c-a} = \frac{(T_c \text{ max} - T_a) + P_{dAV}}{P_{dAV}} \]  

(II)

Tc max : Maximum operating substrate temperature = 105°C
Ta: HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.
The average HIC power loss, PdAV, described above represents the power loss when there is no avalanche operation.
To add the loss during avalanche operations, be sure to add Equation (3-2), “Allowable STK672-7** Avalanche Energy Value”, to PdAV.
Figure 2

![Graph showing the relationship between substrate temperature rise and internal average power dissipation.]

Substrate temperature rise, $\Delta T_c$ (no heat sink) - Internal average power dissipation, $P_{dAV}$

Figure 3

![Graph showing the relationship between heat sink thermal resistance and heat sink area.]

Heat sink area (Board thickness: 2mm) - $\theta_{c-a}$

- No surface finish
- Surface finished in black
6. Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta

Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink. The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta. Power loss of up to 3.1W is allowable at Ta=25°C, and of up to 1.75W at Ta=60°C.

* The package thermal resistance $\theta_{c-a}$ is 25.8°C/W.
7. Example of Stepper Motor Driver Output Current Path (1-2 phase excitation)

- **Phase A output current** \( IoA \)
- **Phase AB output current** \( IoAB \)

When PWM operations of \( IoA \) are OFF, for \( IoAB \), negative current flows through the parasitic diode, \( F2 \).

When PWM operations of \( IoAB \) are OFF, for \( IoA \), negative current flows through the parasitic diode, \( F1 \).
8. Other usage notes

In addition to the “Notes” indicated in the Sample Application Circuit, care should also be given to the following contents during use.

(1) Allowable operating range

Operation of this product assumes use within the allowable operating range. If a supply voltage or an input voltage outside the allowable operating range is applied, an overvoltage may damage the internal control IC or the MOSFET.

If a voltage application mode that exceeds the allowable operating range is anticipated, connect a fuse or take other measures to cut off power supply to the product.

(2) Input pins

If the input pins are connected directly to the board connectors, electrostatic discharge or overvoltage outside the specified range may be applied from the connectors and may damage the product. Current generated by this overvoltage can be suppressed to effectively prevent damage by inserting 100Ω to 1kΩ resistors in lines connected to the input pins.

Take measures such as inserting resistors in lines connected to the input pins.

(3) Power connectors

If the motor power supply VCC is applied by mistake without connecting the GND part of the power connector when the product is operated, such as for test purposes, an overcurrent flows through the VCC decoupling capacitor, C1, to the parasitic diode between the VDD of the internal control IC and GND, and may damage the power supply pin block of the internal control IC.

To prevent damage in this case, connect a 10Ω resistor to the VDD pin, or insert a diode between the VCC decoupling capacitor C1 GND and the VDD pin.

(4) Input Signal Lines

1) Do not use an IC socket to mount the driver, and instead solder the driver directly to the board to minimize fluctuations in the GND potential due to the influence of the resistance component and inductance component of the GND pattern wiring.

2) To reduce noise caused by electromagnetic induction to small signal lines, do not design small signal lines (sensor signal lines, and 5V or 3.3V power supply signal lines) that run parallel in close proximity to the motor output line A (Pin 5), AB (Pin 7), B (Pin 3), or BB (Pin 1) phases.
(5) When mounting multiple drivers on a single board
When mounting multiple drivers on a single board, the GND design should mount a VCC decoupling capacitor, C1, for each driver to stabilize the GND potential of the other drivers. The key wiring points are as follows.

(6) VCC operating limit
When the output (for example F1) of a 2-phase stepper motor driver is turned OFF, the AB phase back electromotive force eab produced by current flowing to the paired F2 parasitic diode is induced in the F1 side, causing the output voltage VFB to become twice or more the VCC voltage. This is expressed by the following formula.

\[ V_{FB} = V_{CC} + e_{ab} \]
\[ = V_{CC} + V_{CC} + I_{OH} \times R_{M} + V_{df} \times 1.5V \]

- \( V_{CC} \): Motor supply voltage
- \( I_{OH} \): Motor current set by Vref
- \( V_{df} \): Voltage drop due to F2 parasitic diode and current detection resistor R1, RM: Motor winding resistance value

Using the above formula, make sure that VFB is always less than the MOSFET withstand voltage of 100V. This is because there is a possibility that operating limit of VCC falls below the allowable operating range of 42V, due to the RM and I_OH specifications.

The oscillating voltage in excess of VFB is caused by LCRM (inductance, capacitor, resistor, mutual inductance) oscillation that includes micro capacitors C, not present in the circuit. Since M is affected by the motor characteristics, there is some difference in oscillating voltage according to the motor specifications. In addition, constant voltage drive without constant current drive enables motor rotation at \( V_{CC} \geq 0V \).
### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping (Qty / Packing)</th>
</tr>
</thead>
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<tr>
<td>STK672-740AN-E</td>
<td>SIP-19 (Pb-Free)</td>
<td>15 / Tube</td>
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</tbody>
</table>