

MOSFET – Power, for 1-Cell Lithium-ion Battery Protection, Dual N-Channel

12 V, 18 A, 5.9 mΩ

EFC6602R

This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-cell lithium-ion battery protection applications.

Features

- 2.5 V Drive
- 2 kV ESD HBM
- Common-Drain Type
- ESD Diode-Protected Gate
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

Typical Applications

- 1-Cell Lithium-ion Battery Charging and Discharging Switch

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Value	Unit
Source-to-Source Voltage	V _{SSS}	12	V
Gate-to-Source Voltage	V _{GSS}	±12	V
Source Current (DC)	I _S	18	A
Source Current (Pulse) PW ≤ 10 μs, duty cycle ≤ 1 %	I _{SP}	60	A
Total Dissipation (Note 1)	P _T	2.0	W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{STG}	- 55 to +150	°C

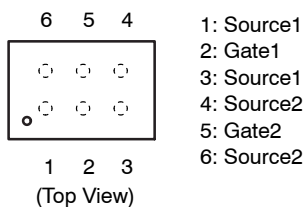
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

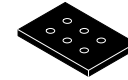
Parameter	Symbol	Value	Unit
Junction to Ambient (Note 1)	R _{θJA}	62.5	°C/W

1. Surface mounted on ceramic substrate (5000 mm² x 0.8 mm)

PIN ASSIGNMENT



V _{SSS}	R _{SS(on)} Max	I _S Max
12 V	5.9 mΩ @ 4.5 V	18 A
	6.3 mΩ @ 4.0 V	
	6.5 mΩ @ 3.8 V	
	8.2 mΩ @ 3.1 V	
	11 mΩ @ 2.5 V	



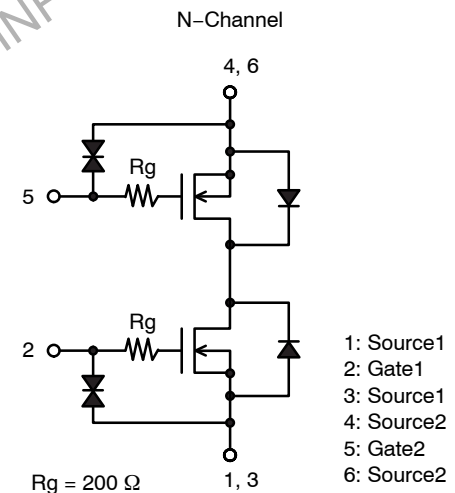
WLCSP6 1.81x2.70 / EFCP2718-6CE-020
CASE 567HS

MARKING DIAGRAM



- MB = Specific Device Code
- Y = Year of Production
- M = Assembly Operation Month
- ZZ = Assembly Lot Number

ELECTRICAL CONNECTION



ORDERING INFORMATION

Device	Package	Shipping
EFC6602R-TR	WLCSP6 (Pb-Free and Halogen Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Source-to-Source Breakdown Voltage	V _{(BR)SSS}	I _S = 1 mA, V _{GS} = 0 V	Test Circuit 1	12	-	-	V
Zero-Gate Voltage Source Current	I _{SSS}	V _{SS} = 10 V, V _{GS} = 0 V	Test Circuit 1	-	-	1	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = ±8 V, V _{SS} = 0 V	Test Circuit 2	-	-	±1	μA
Gate Threshold Voltage	V _{GS(th)}	V _{SS} = 6 V, I _S = 1 mA	Test Circuit 3	0.5	-	1.3	V
Forward Transconductance	g _{FS}	V _{SS} = 6 V, I _S = 3 A	Test Circuit 4	-	13	-	S
Static Source-to-Source On-State Resistance	R _{SS(on)}	I _S = 3 A, V _{GS} = 4.5 V	Test Circuit 5	3.1	4.5	5.9	mΩ
		I _S = 3 A, V _{GS} = 4.0 V	Test Circuit 5	3.3	4.8	6.3	mΩ
		I _S = 3 A, V _{GS} = 3.8 V	Test Circuit 5	3.5	5.0	6.5	mΩ
		I _S = 3 A, V _{GS} = 3.1 V	Test Circuit 5	4.0	5.8	8.2	mΩ
		I _S = 3 A, V _{GS} = 2.5 V	Test Circuit 5	5.2	7.5	11	mΩ
Turn-ON Delay Time	t _{d(on)}	V _{SS} = 6 V, V _{GS} = 4.5 V, I _S = 3 A	Test Circuit 6	-	530	-	ns
Rise Time	t _r			-	2100	-	ns
Turn-OFF Delay Time	t _{d(off)}			-	6200	-	ns
Fall Time	t _f			-	5500	-	ns
Total Gate Charge	Q _g	V _{SS} = 6 V, V _{GS} = 4.5 V, I _S = 18 A	Test Circuit 7	-	55	-	nC
Forward Source-to-Source Voltage	V _{F(S-S)}	I _S = 3 A, V _{GS} = 0 V	Test Circuit 8	-	0.76	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test circuits are example of measuring FET1 side.

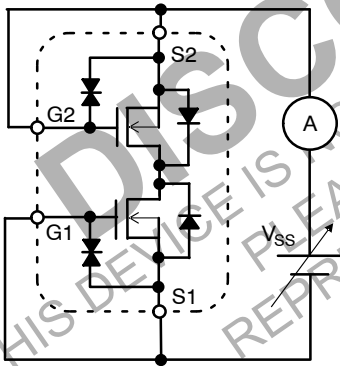


Figure 1. Test Circuit 1 - V_{(BR)SSS} / I_{SSS}

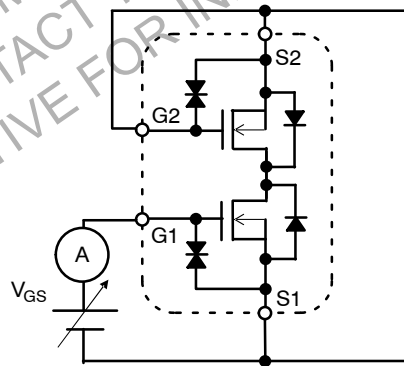


Figure 2. Test Circuit 2 - I_{GSS}

When FET1 is measured, Gate and Source of FET2 are short-circuited.

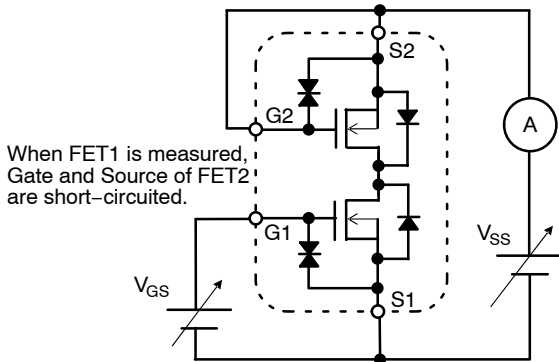


Figure 3. Test Circuit 3 - V_{GS(th)}

When FET1 is measured, Gate and Source of FET2 are short-circuited.

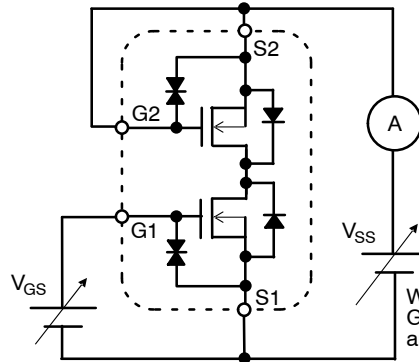


Figure 4. Test Circuit 4 - g_{FS}

When FET1 is measured, Gate and Source of FET2 are short-circuited.

TEST CIRCUITS (continued)

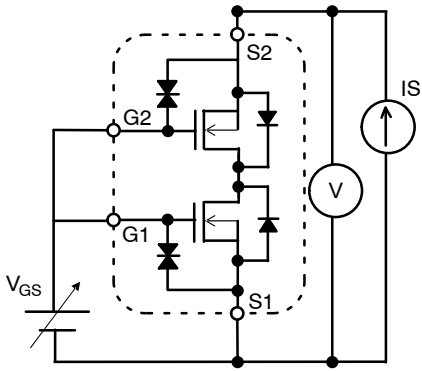


Figure 5. Test Circuit 5 - $R_{SS(on)}$

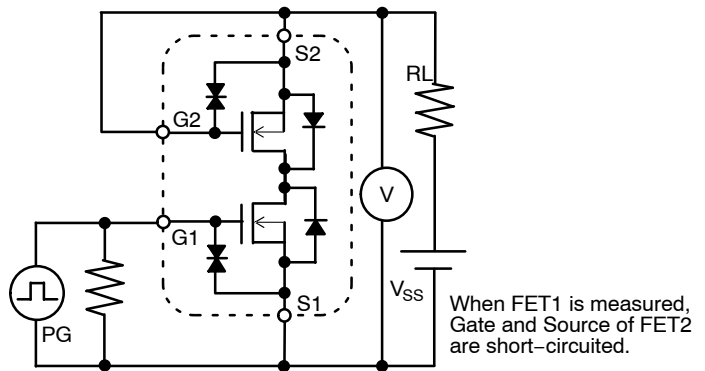


Figure 6. Test Circuit 6 - $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

When FET1 is measured, Gate and Source of FET2 are short-circuited.

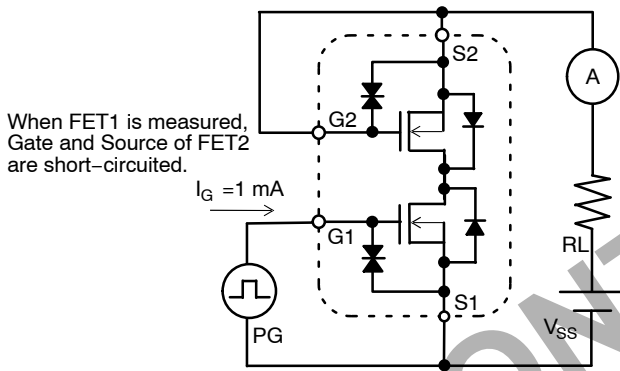


Figure 7. Test Circuit 7 - Q_g

When FET1 is measured, Gate and Source of FET2 are short-circuited.

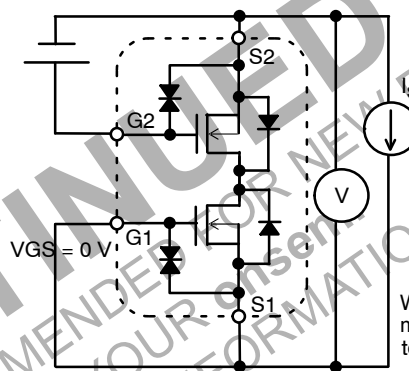


Figure 8. Test Circuit 8 - $V_{F(S-S)}$

When FET1 is measured, +4.5 V is added to V_{GS} of FET2.

When FET2 is measured, the position of FET1 and FET2 is switched.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR ONSEMI REPRESENTATIVE FOR INFORMATION

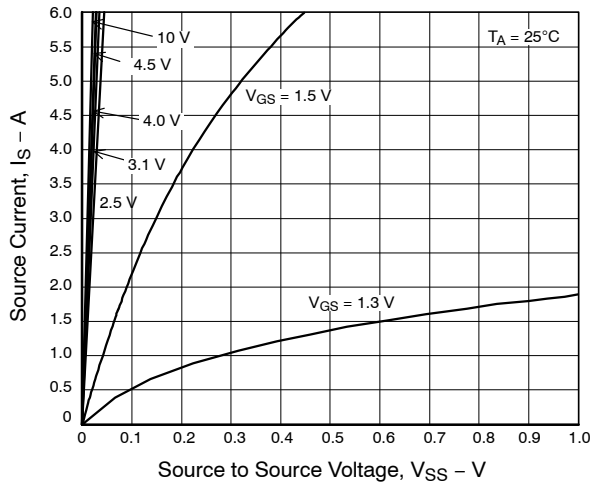


Figure 9. $I_D - V_{SS}$

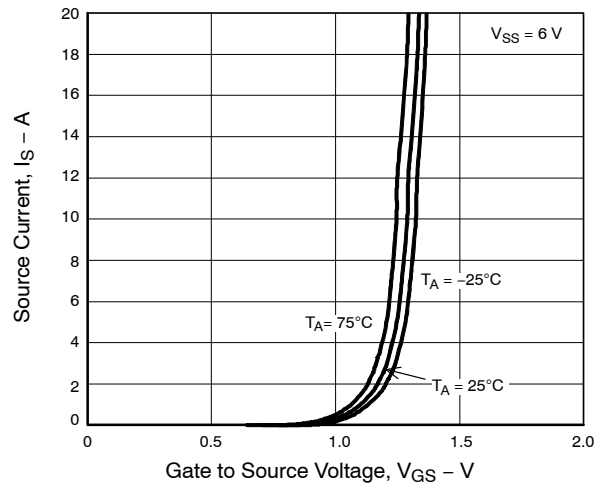


Figure 10. $I_S - V_{GS}$

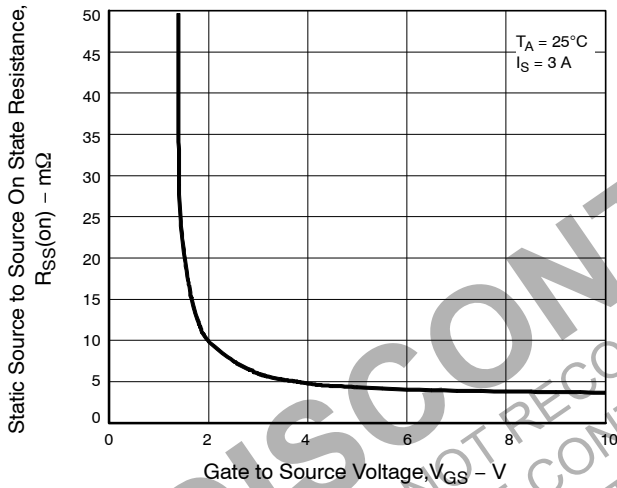


Figure 11. $R_{SS(on)} - V_{GS}$

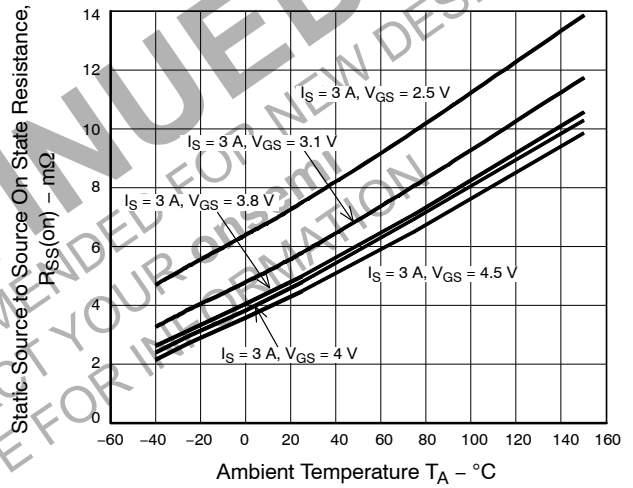


Figure 12. $R_{SS(on)} - T_A$

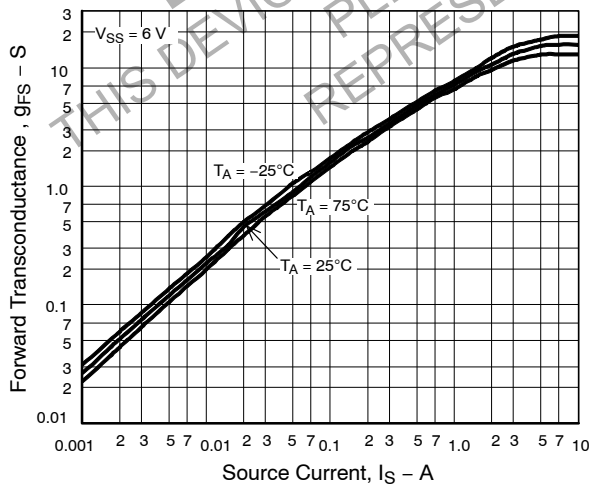


Figure 13. $g_{FS} - I_S$

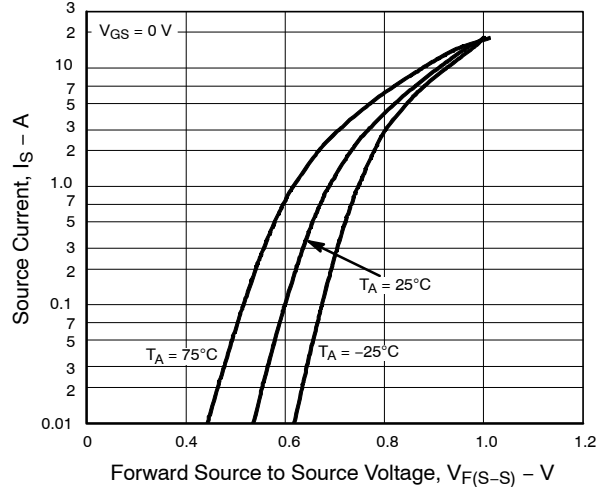


Figure 14. $I_S - V_{F(S-S)}$

EFC6602R

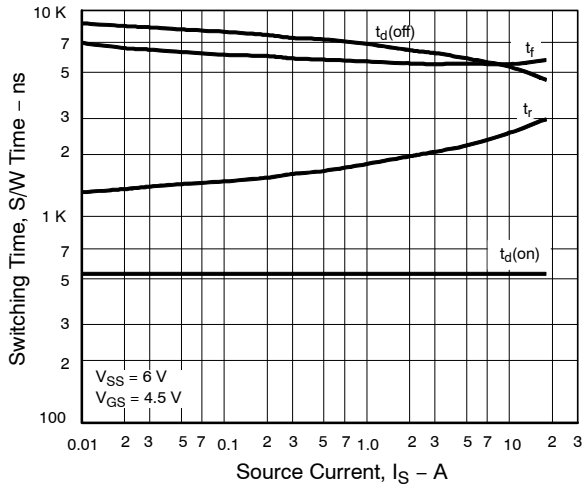


Figure 15. S/W Time - I_S

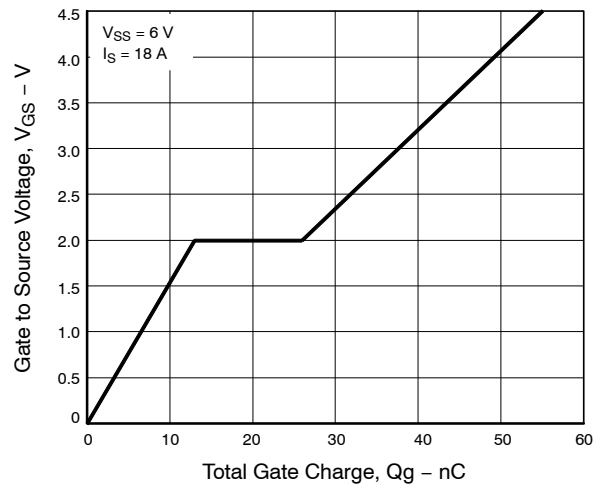


Figure 16. $V_{GS} - Q_g$

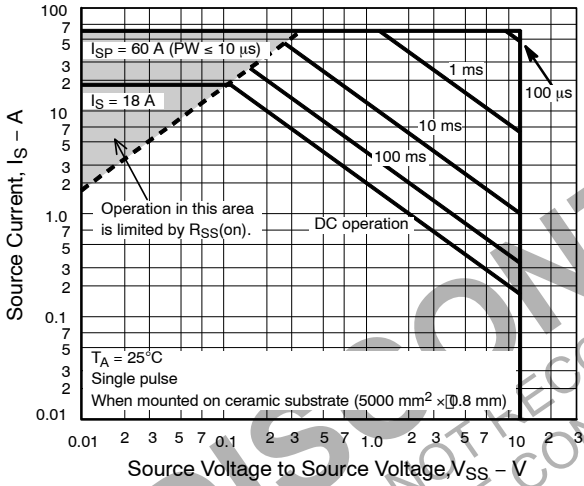


Figure 17. SOA

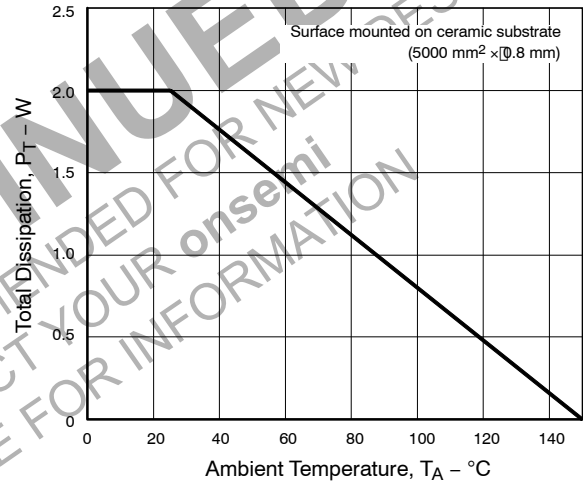


Figure 18. $P_T - T_A$

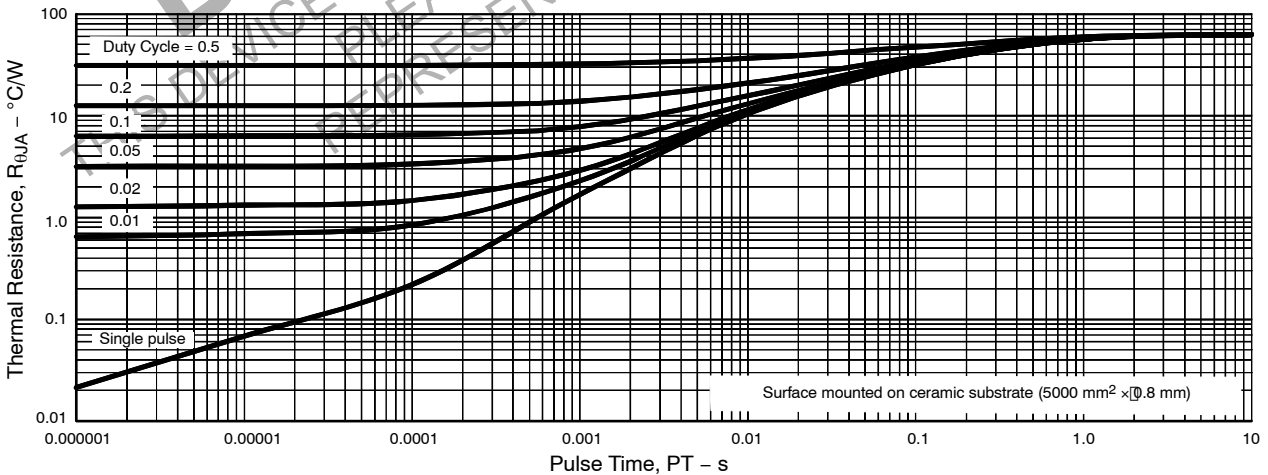
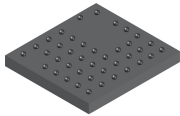


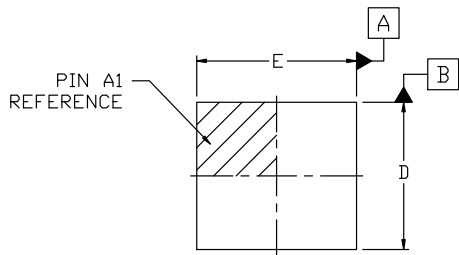
Figure 19. $R_{\theta JA} - \text{Pulse Time}$

Note on usage: Since the EFC6602R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

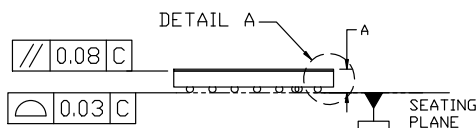


WLCSP40 2.301x2.499x0.369
CASE 567HU
ISSUE O

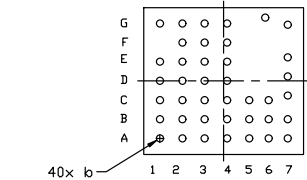
DATE 29 APR 2022



TOP VIEW

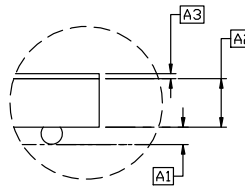


SIDE VIEW

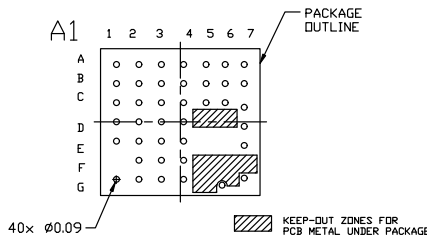


BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.333	0.369	0.405
A1	0.070	0.090	0.110
A2	0.254 REF		
A3	0.022	0.025	0.028
b	0.096	0.111	0.126
D	2.276	2.301	2.326
E	2.474	2.499	2.524



DETAIL A
SCALE 1:3



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

BALL POSITION TABLE					
BALL	X	Y	BALL	X	Y
A1	-1.00	-0.90	D1	-1.00	0.00
A2	-0.65	-0.90	D2	-0.65	0.00
A3	-0.30	-0.90	D3	-0.30	0.00
A4	0.05	-0.90	D4	0.05	0.00
A5	0.40	-0.90	D7	1.00	0.07
A6	0.70	-0.90	E1	-1.00	0.30
A7	1.00	-0.90	E2	-0.65	0.30
B1	-1.00	-0.60	E3	-0.30	0.30
B2	-0.65	-0.60	E4	0.05	0.30
B3	-0.30	-0.60	E7	1.00	0.37
B4	0.05	-0.60	F2	-0.65	0.60
B5	0.40	-0.60	F3	-0.30	0.60
B6	0.70	-0.60	F4	0.05	0.60
B7	1.00	-0.60	G1	-1.00	0.90
C1	-1.00	-0.30	G2	-0.65	0.90
C2	-0.65	-0.30	G3	-0.30	0.90
C3	-0.30	-0.30	G4	0.05	0.90
C4	0.05	-0.30	G6	0.65	0.99
C5	0.40	-0.30	G7	1.00	0.88
C6	0.70	-0.30			
C7	1.00	-0.23			

MOUNTING PAD POSITION TABLE					
BALL	X	Y	BALL	X	Y
A1	-1.00	0.90	D1	-1.00	0.00
A2	-0.65	0.90	D2	-0.65	0.00
A3	-0.30	0.90	D3	-0.30	0.00
A4	0.05	0.90	D4	0.05	0.00
A5	0.40	0.90	D7	1.00	-0.07
A6	0.70	0.90	E1	-1.00	-0.30
A7	1.00	0.90	E2	-0.65	-0.30
B1	-1.00	0.60	E3	-0.30	-0.30
B2	-0.65	0.60	E4	0.05	-0.30
B3	-0.30	0.60	E7	1.00	-0.37
B4	0.05	0.60	F2	-0.65	-0.60
B5	0.40	0.60	F3	-0.30	-0.60
B6	0.70	0.60	F4	0.05	-0.60
B7	1.00	0.60	G1	-1.00	-0.90
C1	-1.00	0.30	G2	-0.65	-0.90
C2	-0.65	0.30	G3	-0.30	-0.90
C3	-0.30	0.30	G4	0.05	-0.90
C4	0.05	0.30	G6	0.65	-0.99
C5	0.40	0.30	G7	1.00	-0.88
C6	0.70	0.30			
C7	1.00	0.23			

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