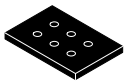
MOSFET – Power, N-Channel, Dual, EFCP

24 V, 13 A, 11.5 mΩ

EFC6601R



WLCSP6 1.81x2.70 / EFCP2718−6CE−020
CASE 567HS

Features

- 2.5 V Drive
- Common−drain Type
- 2 kV ESD HBM
- Protection Diode In
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

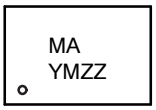
Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Source−to−Source Voltage	V_{SSS}		24	V
Gate−to−Source Voltage	V_{GSS}		±12	V
Source Current (DC)	I_S		13	A
Source Current (Pulse)	I_{SP}	PW ≤ 10 μs, duty cycle ≤1%	60	A
Total Dissipation	P_T	When mounted on ceramic substrate (5000 mm^2 x 0.8 mm)	2.0	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		− 55 to +150	°C

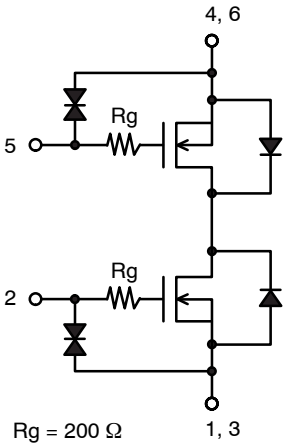
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM

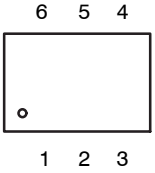


MA = Specific Device Code
Y = Year of Production
M = Assembly Operation Month
ZZ = Assembly Lot Number

ELECTRICAL CONNECTION



PIN ASSIGNMENT



1: Source1
2: Gate1
3: Source1
4: Source2
5: Gate2
6: Source2

ORDERING INFORMATION

Device	Package	Shipping
EFC6601R−TR	EFCP (Pb−Free and Halogen Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Source−to−Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V	Test Circuit 1	24	–	–	V
Zero−Gate Voltage Source Current	I_{SSS}	V_{SS} = 20 V, V_{GS} = 0 V	Test Circuit 1	–	–	1	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{SS} = 0 V	Test Circuit 2	–	–	±1	μA
Cutoff Voltage	V_{GS}(off)	V_{SS} = 10 V, I_S = 1 mA	Test Circuit 3	0.5	–	1.3	V
Forward Transfer Admittance	| yfs |	V_{SS} = 10 V, I_S = 3 A	Test Circuit 4	–	15.5	–	S
Static Source−to−Source On−State Resistance	R_{SS}(on)1	I_S = 3 A, V_{GS} = 4.5 V	Test Circuit 5	6.6	9.5	11.5	mΩ
	R_{SS}(on)2	I_S = 3 A, V_{GS} = 4.0 V	Test Circuit 5	7.0	10	12	mΩ
	R_{SS}(on)3	I_S = 3 A, V_{GS} = 3.8 V	Test Circuit 5	7.3	10.5	13	mΩ
	R_{SS}(on)4	I_S = 3 A, V_{GS} = 3.1 V	Test Circuit 5	8.0	11.5	15	mΩ
	R_{SS}(on)5	I_S = 3 A, V_{GS} = 2.5 V	Test Circuit 5	9.0	13	17	mΩ
Turn−ON Delay Time	t_d(on)	V_{DD} = 10 V, V_{GS} = 4.5 V, I_S = 3 A	Test Circuit 7	–	280	–	ns
Rise Time	t_r			–	630	–	ns
Turn−OFF Delay Time	t_d(off)			–	53000	–	ns
Fall Time	t_f			–	47000	–	ns
Total Gate Charge	Qg	V_{DD} = 10 V, V_{GS} = 4.5 V, I_S = 13 A	Test Circuit 8	–	48	–	nC
Forward Source−to−Source Voltage	$V_{F(S-S)}$	I_S = 3 A, V_{GS} = 0 V	Test Circuit 6	–	0.76	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test circuits are example of measuring FET1 side.

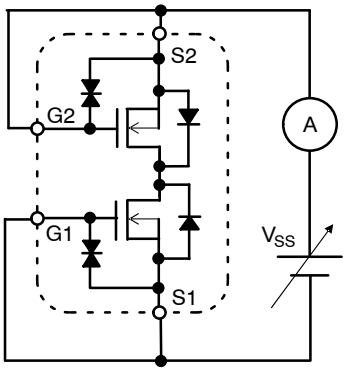
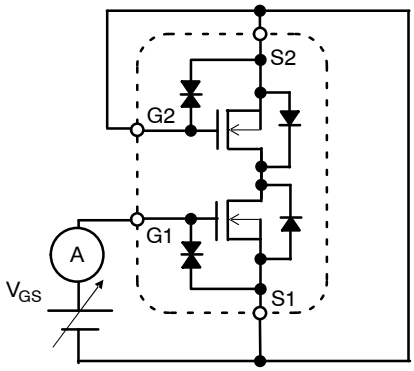
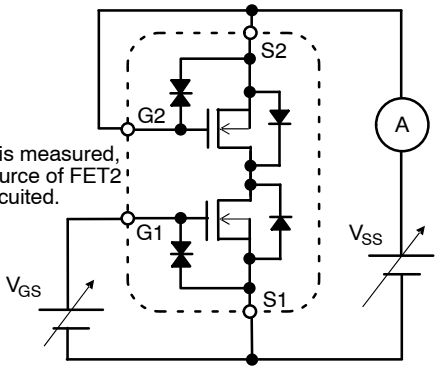


Figure 1. Test Circuit 1 – I_{SSS}



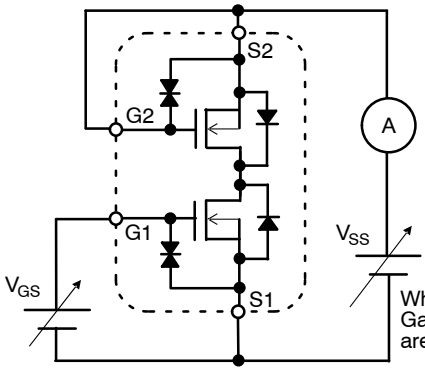
When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 2. Test Circuit 2 – I_{GSS}



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 3. Test Circuit 3 – V_{GS}(off)



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Figure 4. Test Circuit 4 – I yfs I

TEST CIRCUITS (continued)

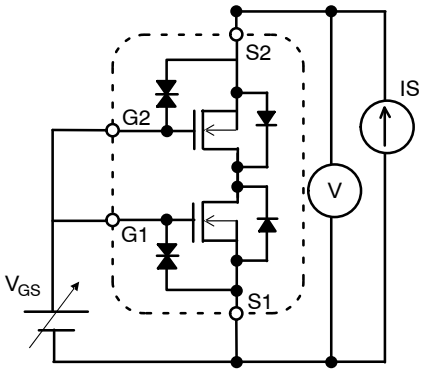


Figure 5. Test Circuit 5 – $R_{SS}(on)$

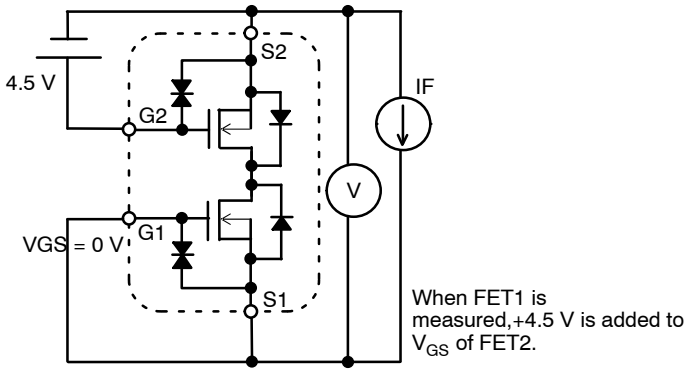


Figure 6. Test Circuit 6 – $V_{F(S-S)}$

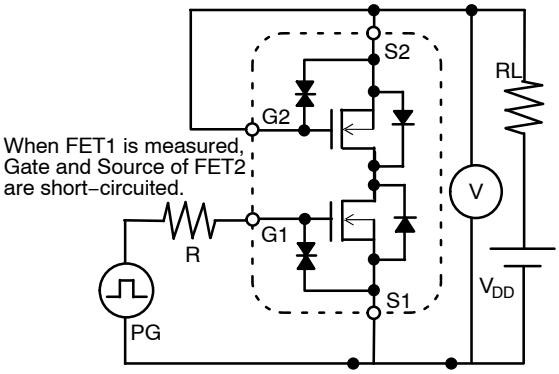


Figure 7. Test Circuit 7 – $t_d(on)$, t_r, $t_d(off)$, t_f

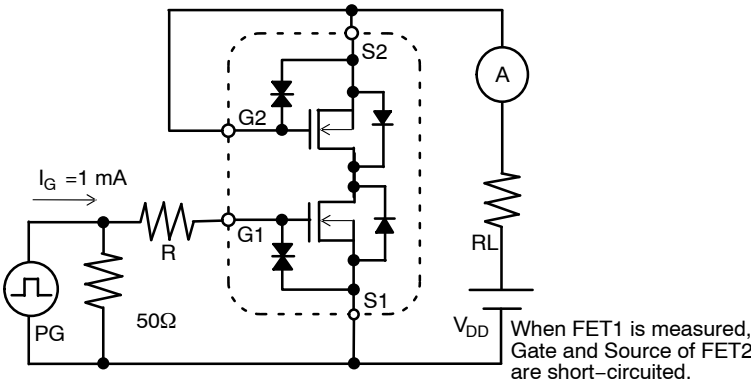


Figure 8. Test Circuit 8 – Qg

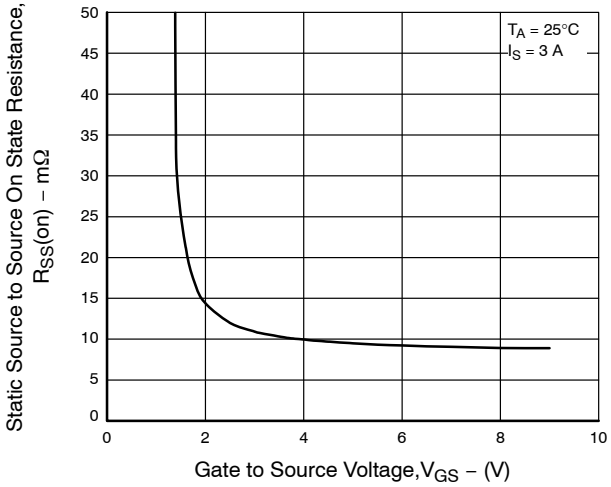


Figure 9. $R_{SS}(on)$ – V_{GS}

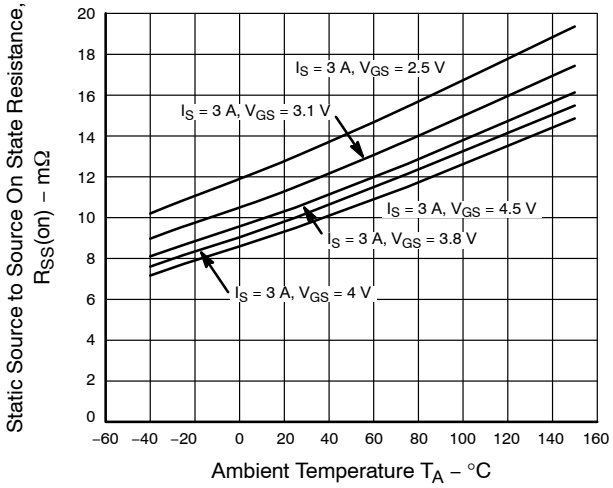


Figure 10. $R_{SS}(on)$ – T_A

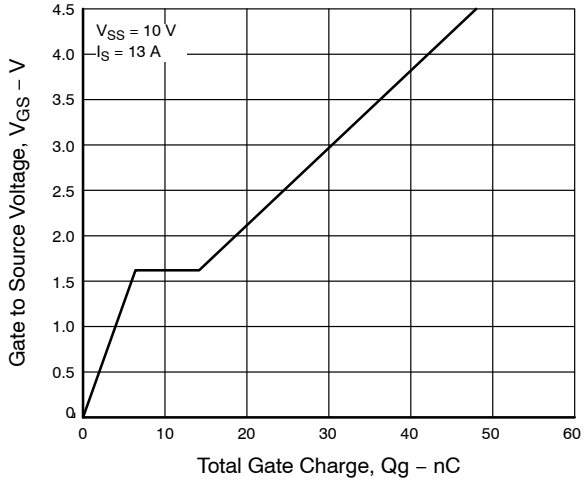


Figure 11. Qg – V_{GS}

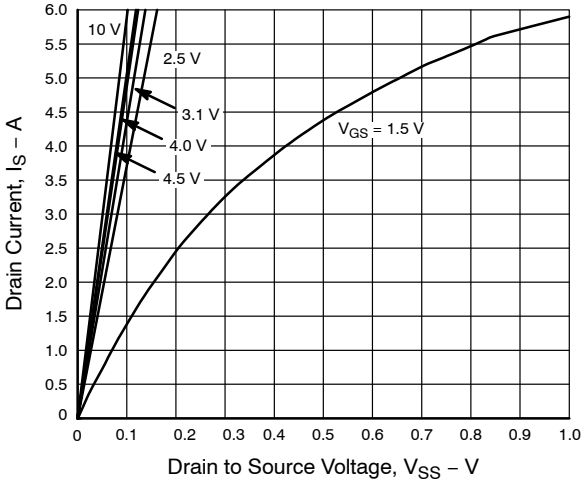


Figure 12. I_S – V_{SS}

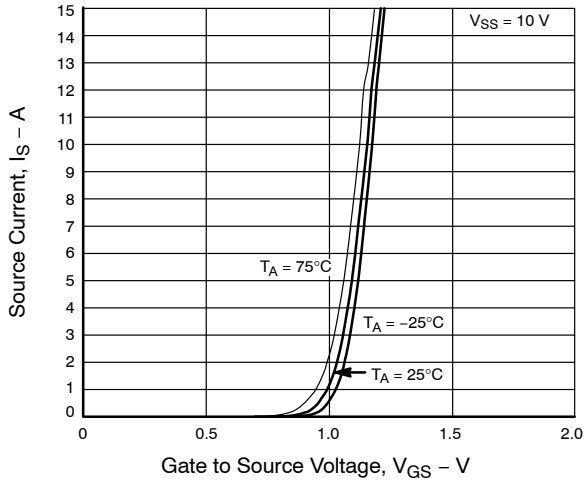


Figure 13. I_S – V_{GS}

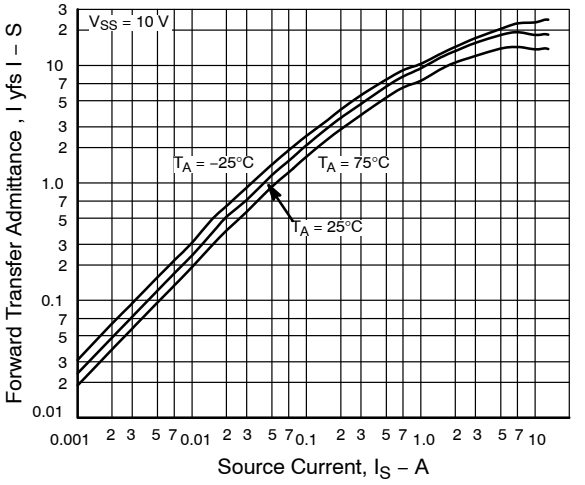


Figure 14. I yfs I – I_S

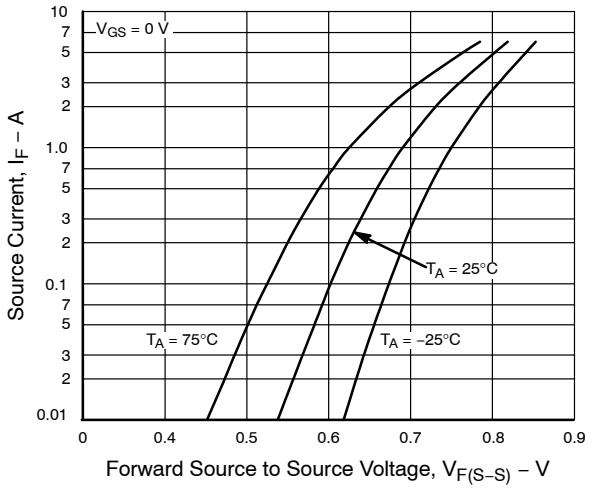


Figure 15. I_S – $V_{F(S-S)}$

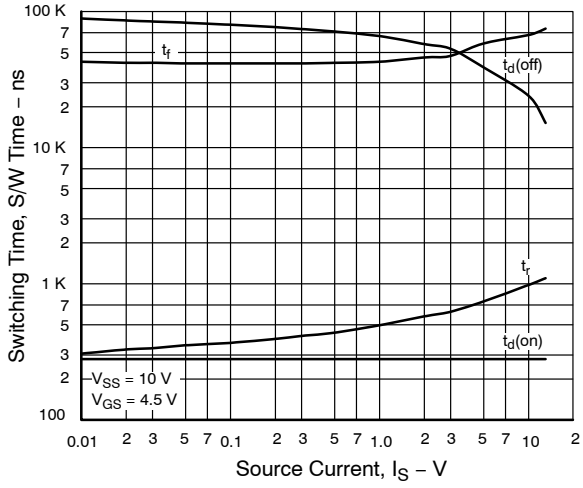


Figure 16. S/W Time – I_D

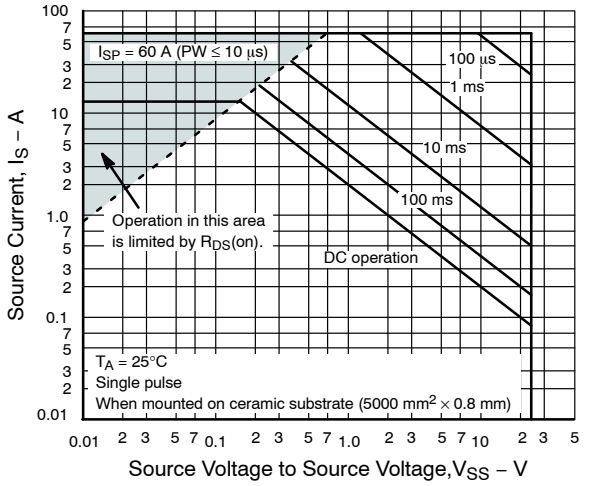


Figure 17. ASO

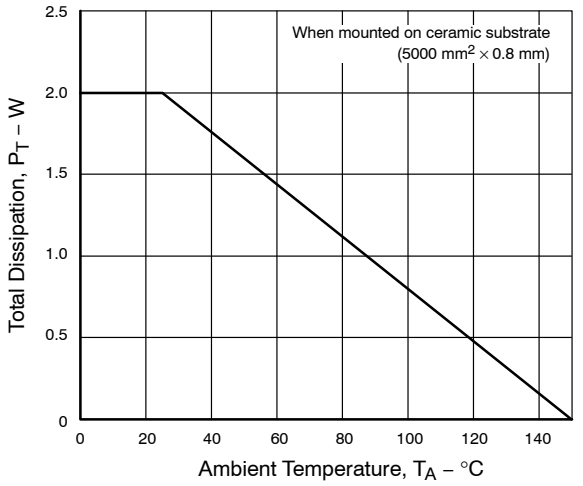


Figure 18. P_T – T_A

Note on usage: Since the EFC6601R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

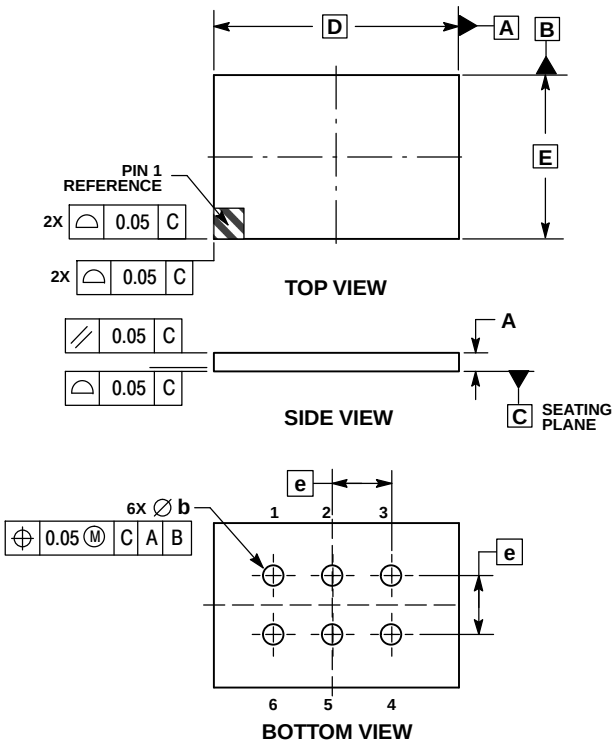
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 4:1

WLCSP6 1.81x2.70 / EFCP2718−6CE−020
CASE 567HS
ISSUE A

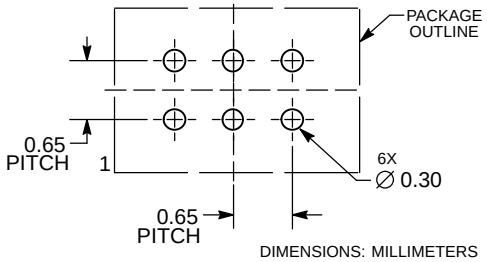
DATE 14 NOV 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.18	0.22
b	0.27	0.33
D	2.70 BSC	
E	1.81 BSC	
e	0.65 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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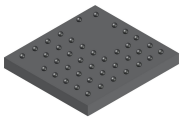
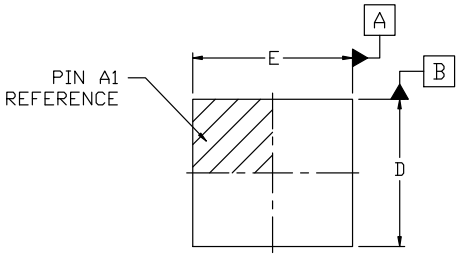
DESCRIPTION:	WLCSP6, 1.81X2.70 / EFCP2718−6CE−020		PAGE 1 OF 2

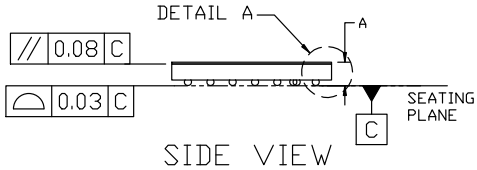


WLCSP40 2.301x2.499x0.369
CASE 567HU
ISSUE O

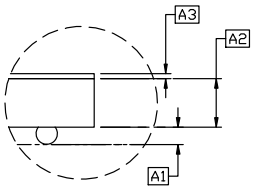
DATE 29 APR 2022



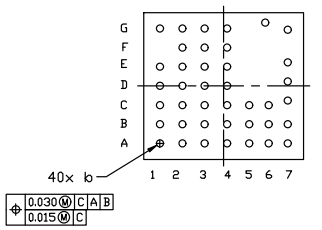
TOP VIEW



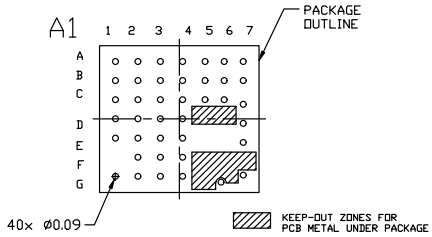
SIDE VIEW



DETAIL A
SCALE 1:3



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.333	0.369	0.405
A1	0.070	0.090	0.110
A2		0.254 REF	
A3	0.022	0.025	0.028
b	0.096	0.111	0.126
D	2.276	2.301	2.326
E	2.474	2.499	2.524

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

BALL POSITION TABLE					
BALL	X	Y	BALL	X	Y
A1	−1.00	−0.90	D1	−1.00	0.00
A2	−0.65	−0.90	D2	−0.65	0.00
A3	−0.30	−0.90	D3	−0.30	0.00
A4	0.05	−0.90	D4	0.05	0.00
A5	0.40	−0.90	D7	1.00	0.07
A6	0.70	−0.90	E1	−1.00	0.30
A7	1.00	−0.90	E2	−0.65	0.30
B1	−1.00	−0.60	E3	−0.30	0.30
B2	−0.65	−0.60	E4	0.05	0.30
B3	−0.30	−0.60	E7	1.00	0.37
B4	0.05	−0.60	F2	−0.65	0.60
B5	0.40	−0.60	F3	−0.30	0.60
B6	0.70	−0.60	F4	0.05	0.60
B7	1.00	−0.60	G1	−1.00	0.90
C1	−1.00	−0.30	G2	−0.65	0.90
C2	−0.65	−0.30	G3	−0.30	0.90
C3	−0.30	−0.30	G4	0.05	0.90
C4	0.05	−0.30	G6	0.65	0.99
C5	0.40	−0.30	G7	1.00	0.88
C6	0.70	−0.30			
C7	1.00	−0.23			

MOUNTING PAD POSITION TABLE					
BALL	X	Y	BALL	X	Y
A1	−1.00	0.90	D1	−1.00	0.00
A2	−0.65	0.90	D2	−0.65	0.00
A3	−0.30	0.90	D3	−0.30	0.00
A4	0.05	0.90	D4	0.05	0.00
A5	0.40	0.90	D7	1.00	−0.07
A6	0.70	0.90	E1	−1.00	−0.30
A7	1.00	0.90	E2	−0.65	−0.30
B1	−1.00	0.60	E3	−0.30	−0.30
B2	−0.65	0.60	E4	0.05	−0.30
B3	−0.30	0.60	E7	1.00	−0.37
B4	0.05	0.60	F2	−0.65	−0.60
B5	0.40	0.60	F3	−0.30	−0.60
B6	0.70	0.60	F4	0.05	−0.60
B7	1.00	0.60	G1	−1.00	−0.90
C1	−1.00	0.30	G2	−0.65	−0.90
C2	−0.65	0.30	G3	−0.30	−0.90
C3	−0.30	0.30	G4	0.05	−0.90
C4	0.05	0.30	G6	0.65	−0.99
C5	0.40	0.30	G7	1.00	−0.88
C6	0.70	0.30			
C7	1.00	0.23			

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP40 2.301x2.499x0.369**		**PAGE 1 OF 1**

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