MOSFET - Power for 1-Cell Lithium-ion Battery Protection

EFC2K103NUZ

12 V, 1.8 mΩ, 40 A, Dual N-Channel

This power MOSFET features a low on−state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1−cell lithium−ion battery applications.

Features

- 2.5 V drive
- Common−Drain type
- ESD Diode−Protected Gate
- Pb−Free, Halogen Free and RoHS Compliance

Typical Applications

- 1−Cell Lithium−ion Battery Charging and Discharging Switch

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	±8	V
Source Current (DC)	I_S	40	A
Source Current (Pulse) PW ≤ 10 μS, Duty Cycle ≤ 1%	I_{SP}	140	A
Total Dissipation (Note 1)	P_T	3.3	W
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 1)	$R_{\theta JA}$	37	°C/W

1. Surface mounted on ceramic substrate (5000 $mm^2 \times 0.8$ mm)

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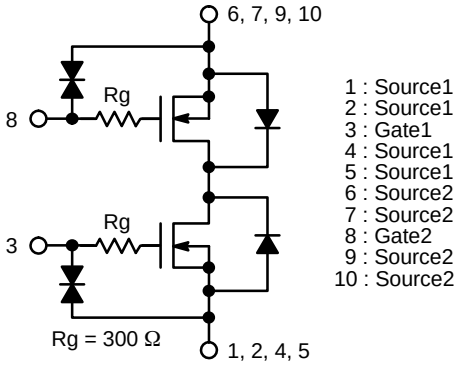
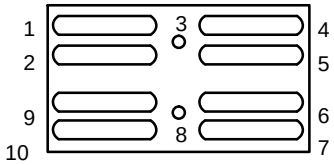
V_{SSS}	$R_{SS(ON)}$ MAX	I_S MAX
12 V	1.8 mΩ @ 4.5 V	40 A
	1.9 mΩ @ 3.8 V	
	2.6 mΩ @ 3.1 V	
	4.2 mΩ @ 2.5 V	

ELECTRICAL CONNECTION

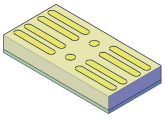
N−Channel

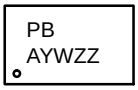


PIN ASSIGNMENT



MARKING DIAGRAM





WLCSP10
3.54x1.77x0.140
CASE 567XB

PB = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Parameter	Symbol	Conditions		Value Min	Value Typ	Value Max	Unit
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V	Test Circuit 1	12	−	−	V
Zero Gate Voltage Source Current	I_{SSS}	V_{SS} = 10 V, V_{GS} = 0 V	Test Circuit 1	−	−	1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{SS} = 0 V	Test Circuit 2	−	−	±1	μA
Gate Threshold Voltage	V_{GS}(th)	V_{SS} = 6 V, I_S = 1 mA	Test Circuit 3	0.4	−	1.3	V
Static Source to Source On−State Resistance	R_{SS}(on)	I_S = 5 A, V_{GS} = 4.5 V	Test Circuit 4	0.8	1.25	1.8	mΩ
		I_S = 5 A, V_{GS} = 3.8 V	Test Circuit 4	0.85	1.35	1.9	mΩ
		I_S = 5 A, V_{GS} = 3.1 V	Test Circuit 4	1.0	1.7	2.6	mΩ
		I_S = 5 A, V_{GS} = 2.5 V	Test Circuit 4	1.2	2.1	4.2	mΩ
Turn−ON Delay Time	t_d(on)	V_{SS} = 6 V, V_{GS} = 3.8 V, I_S = 5 A, R_G = 10 kΩ Test Circuit 5		−	25	−	μs
Rise Time	t_r			−	100	−	μs
Turn−OFF Delay Time	t_d(off)			−	165	−	μs
Fall Time	t_f			−	148	−	μs
Total Gate Charge	Qg	V_{SS} = 6 V, V_{GS} = 3.8 V, I_S = 5 A Test Circuit 6		−	62	−	nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S = 3 A, V_{GS} = 0 V	Test Circuit 7	−	0.75	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)†
EFC2K103NUZTDG	PB	WLCSP10, 3.54 × 1.77 × 0.140 (Pb−Free / Halogen Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

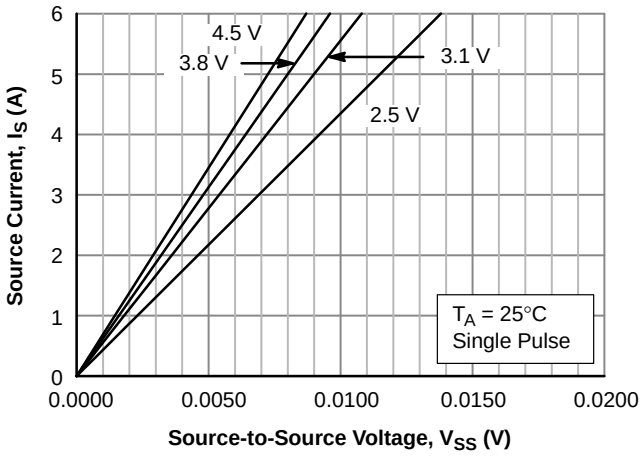


Figure 1. I_S − V_{SS}

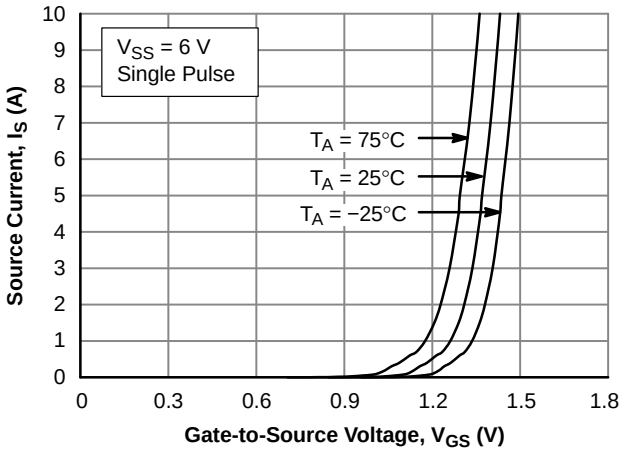


Figure 2. I_S − V_{GS}

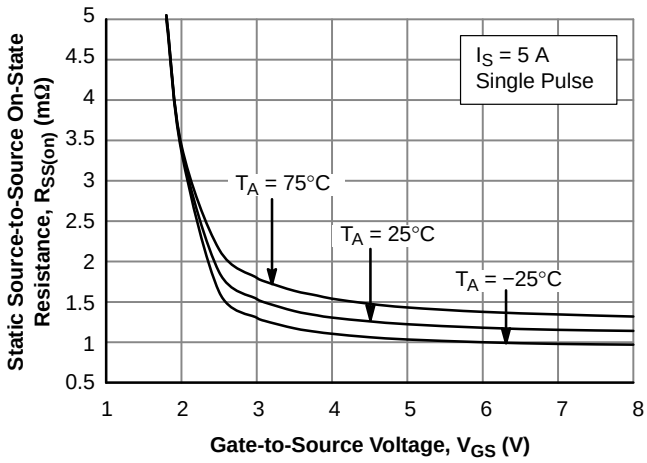


Figure 3. $R_{SS(on)}$ − V_{GS}

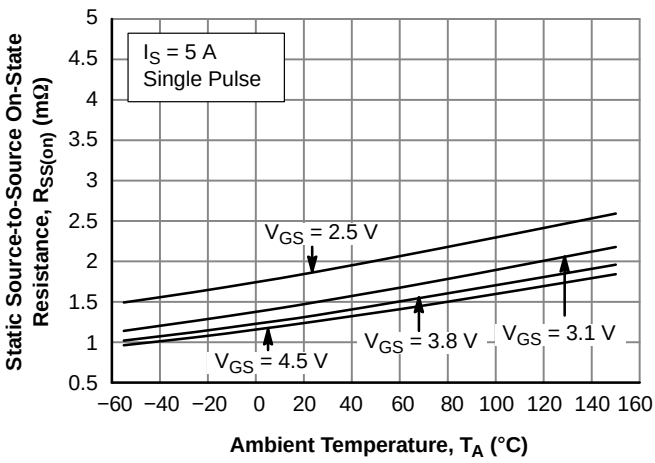


Figure 4. $R_{SS(on)}$ − T_A

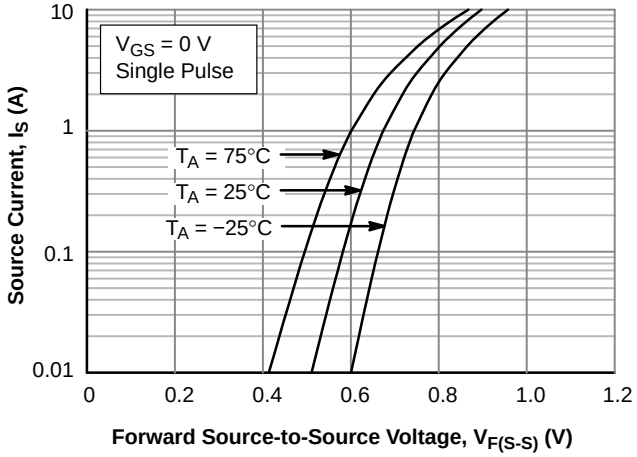


Figure 5. I_S − $V_{F(S-S)}$

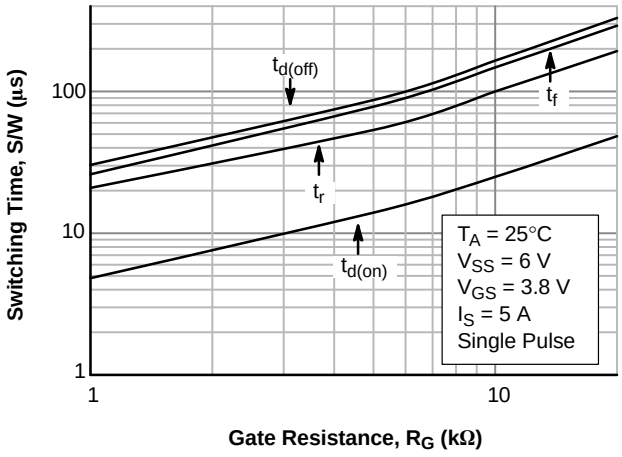


Figure 6. SW Time − R_G

TYPICAL CHARACTERISTICS (Continued)

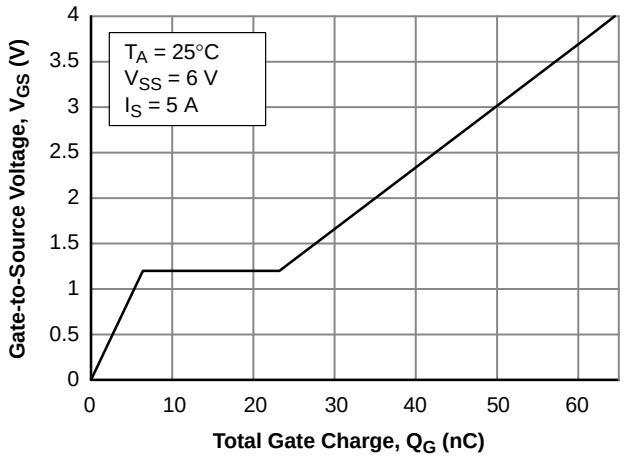


Figure 7. V_{GS} − Q_G

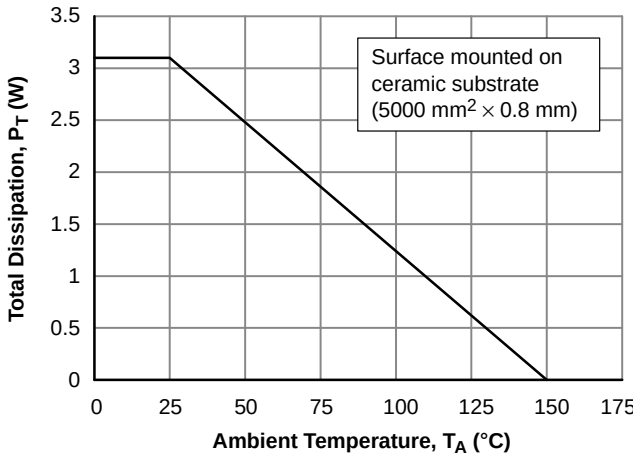


Figure 8. P_T − T_A

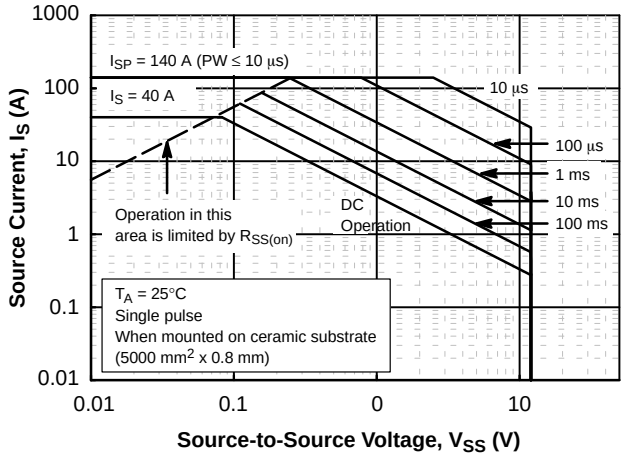


Figure 9. Safe Operating Area

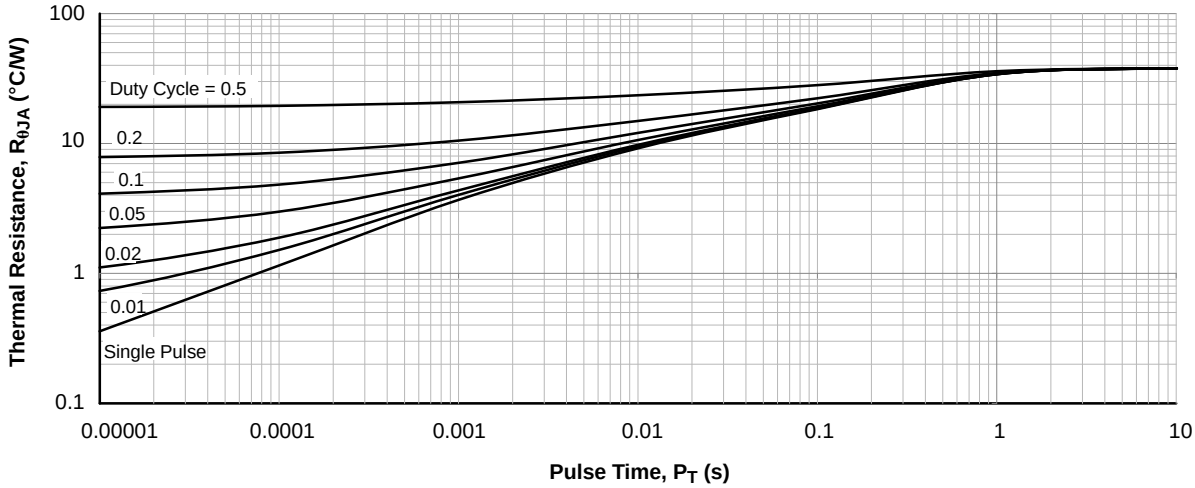


Figure 10. Thermal Response

TEST CIRCUITS ARE EXAMPLES OF MEASURING FET1 SIDE

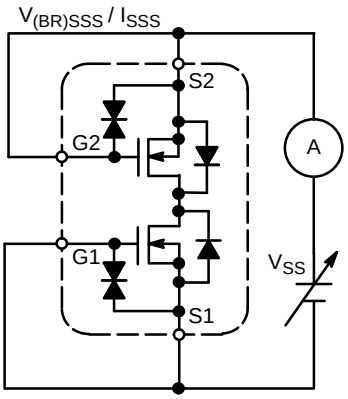


Figure 11. Test Circuit 1

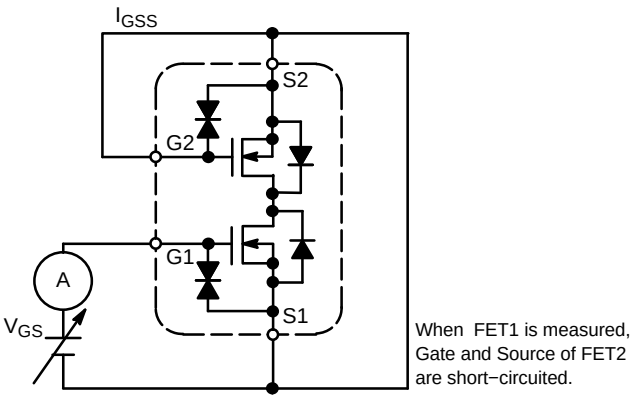


Figure 12. Test Circuit 2

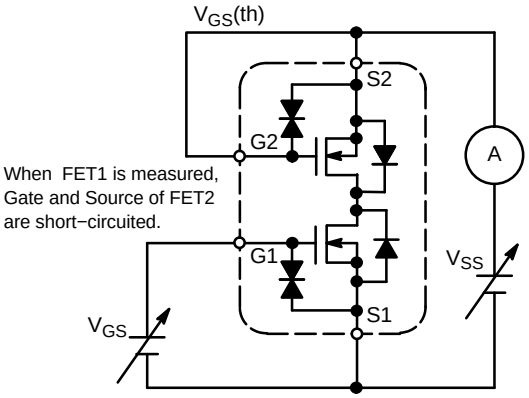


Figure 13. Test Circuit 3

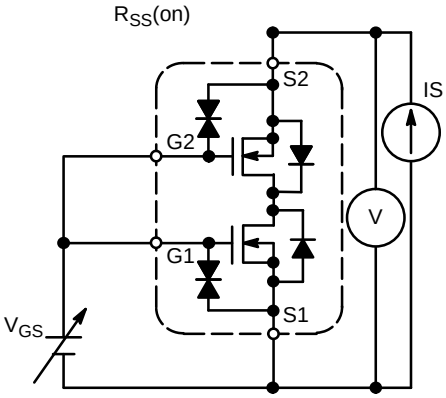


Figure 14. Test Circuit 4

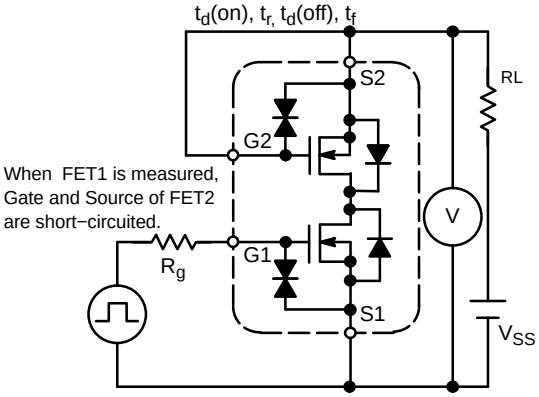


Figure 15. Test Circuit 5

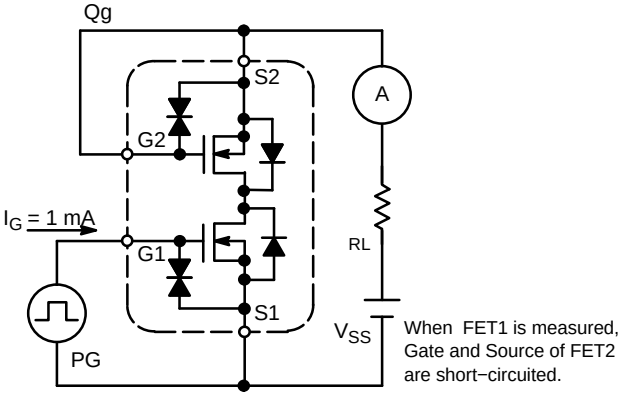


Figure 16. Test Circuit 6

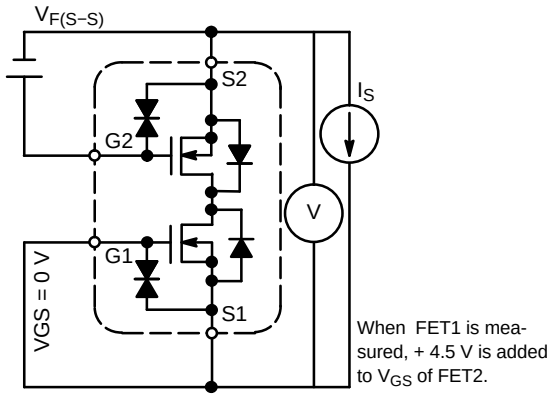


Figure 17. Test Circuit

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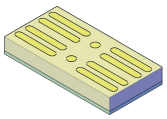
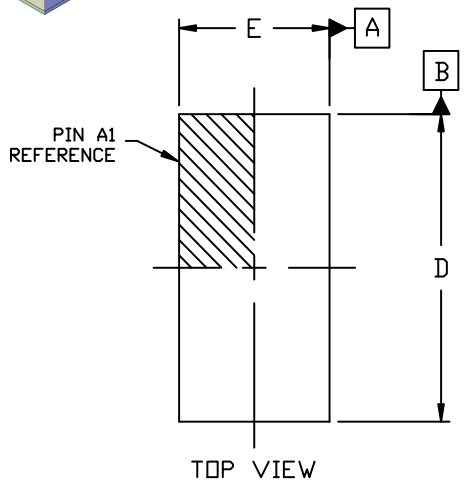
NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

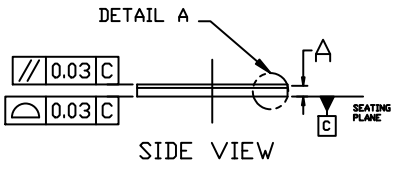
NOTE: Since the EFC2K103NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

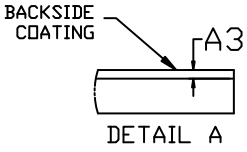


WLCSP10, 3.54x1.77x0.14
CASE 567XB
ISSUE O

DATE 09 OCT 2018



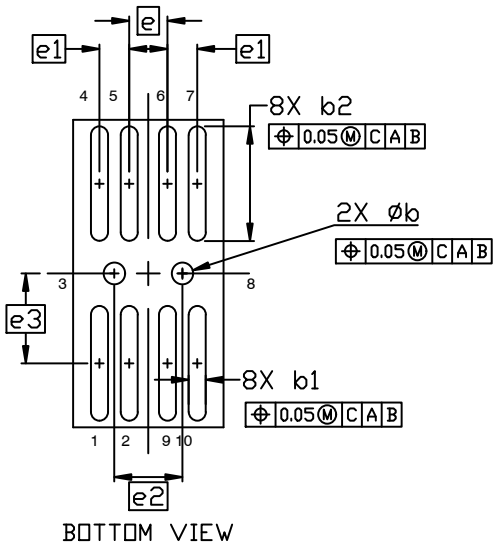


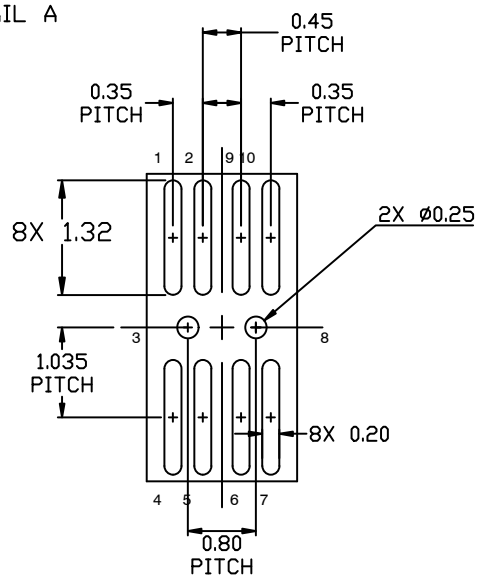


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.11	0.14	0.17
A3		0.04 REF	
b	0.22	0.25	0.28
b1	0.17	0.20	0.23
b2	1.29	1.32	1.35
D	3.51	3.54	3.57
E	1.74	1.77	1.80
e		0.45 BSC	
e1		0.35 BSC	
e2		0.80 BSC	
e3		1.035 BSC	





GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON98952G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WLCSP10, 3.54x1.77x0.14**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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