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CS5303

Three-Phase Buck Controller with Integrated Gate Drivers

The CS5303 is a three−phase step down controller which incorporates all control functions required to power high performance processors and high current power supplies. Proprietary multi−phase architecture guarantees balanced load current distribution and reduces overall solution cost in high current applications. Enhanced V^2™ control architecture provides the fastest possible transient response, excellent overall regulation, and ease of use.

The CS5303 multi−phase architecture reduces output voltage and input current ripple, allowing for a significant reduction in inductor values and a corresponding increase in inductor current slew rate. This approach allows a considerable reduction in input and output capacitor requirements, as well as reducing overall solution size and cost.

Features

- Enhanced V^2 Control Method
- 5−Bit DAC with 1.0% Accuracy
- Adjustable Output Voltage Positioning
- 6 On−Board Gate Drivers
- 200 kHz to 800 kHz Operation Set by Resistor
- Current Sensed through Buck Inductors, Sense Resistors, or V−S Control
- Hiccup Mode Current Limit
- Individual Current Limits for Each Phase
- On−Board Current Sense Amplifiers
- 3.3 V, 1.0 mA Reference Output
- 5.0 V and/or 12 V Operation
- On/Off Control (through COMP Pin)

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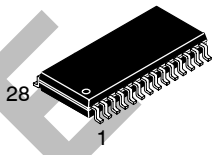
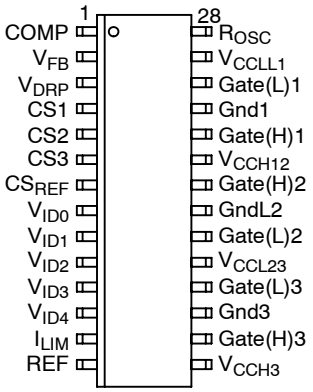


SO−28L
DW SUFFIX
CASE 751F

MARKING DIAGRAM

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
CS5303GDW28	SO−28L	27 Units/Rail
CS5303GDWR28	SO−28L	1000 Tape & Reel

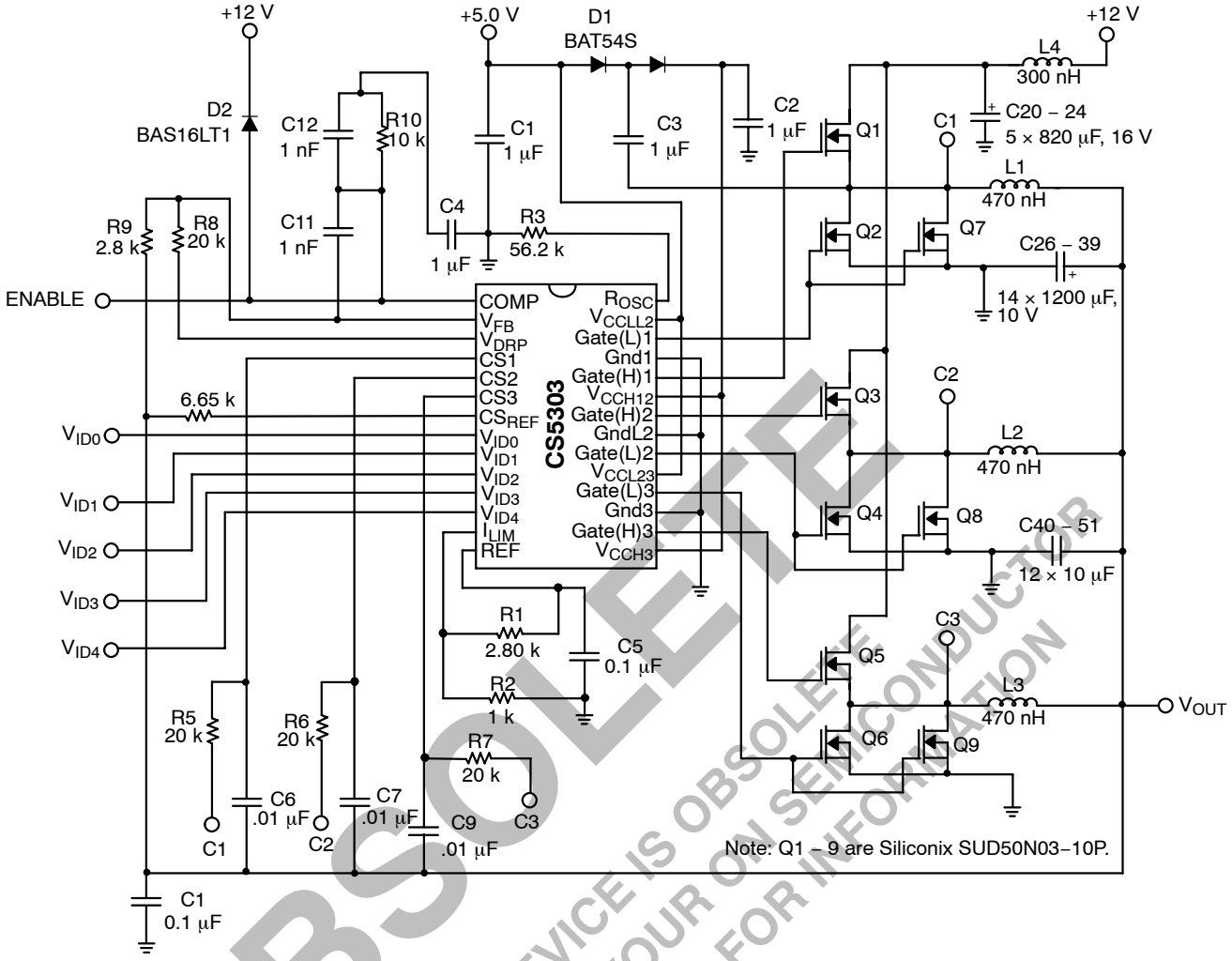


Figure 1. Application Diagram, 12 V to 1.5 V, 60 A Converter

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
Operating Junction Temperature	150	°C
Lead Temperature Soldering: : Reflow: (SMD styles only) (Note 1)	230 peak,	°C
Storage Temperature Range	−65 to +150	°C
ESD Susceptibility (Human Body Model)	2.0	kV

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
Power for logic and Gate(L)1	V_{CCLL1}	16 V	−0.3 V	N/A	1.5 A, 1.0 μs 200 mA DC
Power for Gate(L)2 and Gate(L)3	V_{CCL23}	16 V	−0.3 V	N/A	1.5 A, 1.0 μs 200 mA DC
Power for Gate(H)1 and Gate(H)2	V_{CCH12}	20 V	−0.3 V	N/A	1.5 A, 1.0 μs 200 mA DC
Power Gate(H)3	V_{CCH3}	20 V	−0.3 V	N/A	1.5 A, 1.0 μs 200 mA DC

ABSOLUTE MAXIMUM RATINGS (continued)

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
Voltage Feedback Compensation Network	COMP	6.0 V	−0.3 V	1.0 mA	1.0 mA
Voltage Feedback Input	V_{FB}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Output for adjusting adaptive voltage positioning	V_{DRP}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Frequency Resistor	R_{OSC}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Reference Output	REF	6.0 V	−0.3 V	1.0 mA	50 mA
High−Side FET Drivers	Gate(H)1−3	20 V	−0.3 V −2 V for 100 nS	1.5 A, 1.0 μs 200 mA DC	1.5 A, 1 μs 200 mA DC
Low−Side FET Drivers	Gate(L)1−3	16 V	−0.3 V −2 V for 100 nS	1.5 A, 1.0 μs 200 mA DC	1.5 A, 1.0 μs 200 mA DC
Return for #1 Driver	Gnd1	0.3 V	−0.3 V	2 A, 1.0 μs 200 mA DC	N/A
Return for logic and #2 Driver	GndL2	N/A	N/A	2.0 A, 1.0 μs 200 mA DC	N/A
Return for #3 Driver	Gnd3	0.3 V	−0.3 V	2.0 A, 1.0 μs 200 mA DC	N/A
Current Sense for phases 1 − 3	CS1−CS3	6.0 V	−0.3 V	1.0 mA	1.0 mA
Current Limit Set Point	I_{LIM}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Current Sense Reference	CS_{REF}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Voltage ID DAC Inputs	VID0−4	6.0 V	−0.3 V	1.0 mA	1.0 mA

ELECTRICAL CHARACTERISTICS (0°C < T_A < 70°C; 0°C < T_J < 125°C; 4.7 V < V_{CCL} < 14 V; 8 V < V_{CCH} < 20 V; $C_{GATE(H)}$ = 3.3 nF, $C_{GATE(L)}$ = 3.3 nF, $R_{R(OSC)}$ = 53.6 k, C_{COMP} = 0.1 μF, C_{REF} = 0.1μF, DAC Code 10000, C_{VCC} = 1.0 μF, I_{LIM} ≥ V; unless otherwise specified.)

Characteristic					Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC (0 = Connected to V_{SS}; 1 = Open or Pull−up to 3.3 V)									
Accuracy (all codes)					Measure V_{FB} = COMP			±.0	%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}					
1	1	1	1	1	–	1.064	1.075	1.086	V
1	1	1	1	0	–	1.089	1.100	1.111	V
1	1	1	0	1	–	1.114	1.125	1.136	V
1	1	1	0	0	–	1.139	1.150	1.162	V
1	1	0	1	1	–	1.163	1.175	1.187	V
1	1	0	1	0	–	1.188	1.200	1.212	V
1	1	0	0	1	–	1.213	1.225	1.237	V
1	1	0	0	0	–	1.238	1.250	1.263	V
1	0	1	1	1	–	1.262	1.275	1.288	V
1	0	1	1	0	–	1.287	1.300	1.313	V
1	0	1	0	1	–	1.312	1.325	1.338	V
1	0	1	0	0	–	1.337	1.350	1.364	V
1	0	0	1	1	–	1.361	1.375	1.389	V
1	0	0	1	0	–	1.386	1.400	1.414	V
1	0	0	0	1	–	1.411	1.425	1.439	V
1	0	0	0	0	–	1.436	1.450	1.465	V

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.7\ V < V_{CCL} < 14\ V$; $8\ V < V_{CCH} < 20\ V$; $C_{GATE(H)} = 3.3\ nF$, $C_{GATE(L)} = 3.3\ nF$, $R_{R(OSC)} = 53.6\ k$, $C_{COMP} = 0.1\ \mu F$, $C_{REF} = 0.1\mu F$, DAC Code 10000, $C_{VCC} = 1.0\ \mu F$, $I_{LIM} \geq$ [illegible] V; unless otherwise specified.)

Characteristic					Test Conditions	Min	Typ	Max	Unit
Voltage Identification DAC (0 = Connected to V_{SS}; 1 = Open or Pull−up to 3.3 V)									
0	1	1	1	1	–	1.460	1.475	1.490	V
0	1	1	1	0	–	1.485	1.500	1.515	V
0	1	1	0	1	–	1.510	1.525	1.540	V
0	1	1	0	0	–	1.535	1.550	1.566	V
0	1	0	1	1	–	1.559	1.575	1.591	V
0	1	0	1	0	–	1.584	1.600	1.616	V
0	1	0	0	1	–	1.609	1.625	1.641	V
0	1	0	0	0	–	1.634	1.650	1.667	V
0	0	1	1	1	–	1.658	1.675	1.692	V
0	0	1	1	0	–	1.683	1.700	1.717	V
0	0	1	0	1	–	1.708	1.725	1.742	V
0	0	1	0	0	–	1.733	1.750	1.768	V
0	0	0	1	1	–	1.757	1.775	1.793	V
0	0	0	1	0	–	1.782	1.800	1.818	V
0	0	0	0	1	–	1.807	1.825	1.843	V
0	0	0	0	0	–	1.832	1.850	1.869	V
Input Threshold					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	1.00	1.25	1.50	V
Input Pull−up Resistance					V_{ID4}, V_{ID3}, V_{ID2}, V_{ID1}, V_{ID0}	25	50	100	kΩ
Pull−up Voltage					–	3.15	3.30	3.45	V

Voltage Feedback Error Amplifier

V_{FB} Bias Current (Note 2)	$1.0\ V < V_{FB} < 1.9\ V$	16.8	19.0	21.5	μA
COMP Source Current	COMP = 0.5 V to 2.0 V; V_{FB} = 1.8 V; DAC = 00000	15	30	60	μA
COMP Sink Current	COMP = 0.5 V to 2.0 V; V_{FB} = 1.9 V; DAC = 00000	15	30	60	μA
COMP Discharge Threshold Voltage	–	0.20	0.27	0.34	V
Transconductance	$-10\ \mu A < I_{COMP} < +10\ \mu A$	–	32	–	mmho
Output Impedance	–	–	2.5	–	MΩ
Open Loop DC Gain	Note 3	60	90	–	–
Unity Gain Bandwidth	0.01 μF COMP Capacitor	–	400	–	kHz
PSRR @ 1 kHz	–	–	70	–	dB
COMP Max Voltage	V_{FB} = 1.8 V; COMP Open; DAC = 00000	2.4	2.7	–	V
COMP Min Voltage	V_{FB} = 1.9 V; COMP Open; DAC = 00000	–	0.1	0.2	V
Hiccup Latch Discharge Current	–	2.0	5.0	10	μA
COMP Discharge Ratio	–	4.0	6.0	10	–

2. The V_{FB} Bias Current changes with the value of R_{OSC} per Figure 4.
3. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.7\ V < V_{CCL} < 14\ V$; $8\ V < V_{CCH} < 20\ V$; $C_{GATE(H)} = 3.3$ nF, $C_{GATE(L)} = 3.3$ nF, $R_{R(OSC)} = 53.6$ k, $C_{COMP} = 0.1\ \mu F$, $C_{REF} = 0.1 \mu F$, DAC Code 10000, $C_{VCC} = 1.0\ \mu F$, $I_{LIM} \geq 1$ V;unless otherwise specified)

Characteristic	Test Conditions	Min	Typ	Max	Unit
PWM Comparators					
Minimum Pulse Width	Measured from CSx to GATE(H) $V(V_{FB}) = V(CS_{REF}) = 1.0$ V, V(COMP) = 1.5 V 60 mV step applied between V_{CSX} and V_{CREF}	–	350	515	ns
Channel Start Up Offset	V(CS1) = V(CS2) = V(CS3) = $V(V_{FB})$ = 0.3 $V(CS_{REF})$ = 0 V; Measure V(COMP) when GATE1(H), 2(H), 3(H) switch high	0.4	0.5	–	V
Gate(H) and Gate(L)					
High Voltage (AC)	Note 4 Measure V_{CCLX} – Gate(L) or V_{CCHX} – Gate(H)	–	0	1.0	V
Low Voltage (AC)	Note 4, Measure Gate(L) or Gate(H)	–	0	0.5	V
Rise Time Gate(H)x	1.0 V < GATE < 8.0 V; V_{CCHX} = 10 V	–	35	80	ns
Rise Time Gate(L)x	1.0 V < GATE < 8.0 V; V_{CCLX} = 10 V	–	35	80	ns
Fall Time Gate(H)x	8.0 V > GATE > 1.0 V; V_{CCHX} = 10 V	–	35	80	ns
Fall Time Gate(L)	8.0 V > GATE > 1.0 V; V_{CCLX} = 10 V	–	35	80	ns
Gate(H) to Gate(L) Delay	Gate(H) < 2.0 V, Gate(L) > 2 V	30	65	110	ns
Gate(L) to Gate(H) Delay	Gate(L) < 2.0 V, Gate(H) > 2 V	30	65	110	ns
GATE Pull−down	Force 100 μA into Gate Driver with no power applied to V_{CCHX} and V_{CCLX} = 2 V.	–	1.2	1.6	V
Oscillator					
Switching Frequency	Measure any phase (R_{OSC} = 53.6 k)	220	250	280	kHz
Switching Frequency	Note 4 Measure any phase (R_{OSC} = 32.4 k)	300	400	500	kHz
Switching Frequency	Note 4 Measure any phase (R_{OSC} = 16.2 k)	600	800	1000	kHz
R_{OSC} Voltage	–	–	1.00	–	V
Phase Delay	–	105	120	135	deg
Adaptive Voltage Positioning					
V_{DRP} Output Voltage to DAC_{OUT} Offset	CS1 = CS2 = CS3 = CS_{REF}, V_{FB} = COMP Measure V_{DRP} – COMP	−20	–	20	mV
Maximum V_{DRP} Voltage	|(CS1 = CS2 = CS3) – C_{REF}| = 50 mV, V_{FB} = COMP, Measure V_{DRP} – COMP	360	465	570	mV
Current Sense Amp to V_{DRP} Gain	–	2.4	3.0	3.8	V/V
Current Sensing and Sharing					
CS1−CS3 Input Bias Current	V(CSx) = $V(CS_{REF})$ = 0 V	–	0.2	2.0	μA
CS_{REF} Input Bias Current	–	–	0.6	6.0	μA
Current Sense Amplifiers Gain	–	3.8	4.3	4.8	V/V
Current Sense Amp Mismatch (The sum of offset and gain errors)	Note 4 $0 \leq (CSx - CS_{REF}) \leq 50$ mV	−5.0	–	5.0	mV
Current Sense Amplifiers Input Common Mode Range Limit	Note 4 7 V < V_{CCLL1} < 12 V	0	–	$V_{CCLL1} - 2$	V
Current Sense Input to I_{LIM} Gain	0.25 V < I_{LIM} < 1.20 V	5.0	6.5	8.0	V/V
Current Limit Filter Slew Rate	Note 4	7.5	15.0	40.0	mV/μs

4. Guaranteed by design. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.7\ V < V_{CCL} < 14\ V$; $8\ V < V_{CCH} < 20\ V$; $C_{GATE(H)} = 3.3\ nF$, $C_{GATE(L)} = 3.3\ nF$, $R_{R(OSC)} = 53.6\ k$, $C_{COMP} = 0.1\ \mu F$, $C_{REF} = 0.1 \mu F$, DAC Code 10000, $C_{VCC} = 1.0\ \mu F$, $I_{LIM} \geq 1\ V$;unless otherwise specified)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Current Sensing and Sharing					
I_{LIM} Bias Current	$0 < I_{LIM} < 1.0\ V$	–	0.1	1.0	μA
Single Phase Pulse by Pulse Current Limit: $V(CSx) - V(CS_{REF})$	–	60	70	90	mV
Current Share Amplifier Bandwidth	Note 5	1.0	–	–	mHz
Reference Output					
V_{REF} Output Voltage	$0\ mA < I(V_{REF}) < 1.0\ mA$	3.15	3.25	3.35	V
General Electrical Specifications					
V_{CCLL1} Operating Current	V_{FB} = COMP(no switching)	–	23	28	mA
V_{CCL23} Operating Current	V_{FB} = COMP(no switching)	–	8.0	11	mA
V_{CCH12} Operating Current	V_{FB} = COMP(no switching)	–	5.5	7.0	mA
V_{CCH3} Operating Current	V_{FB} = COMP(no switching)	–	2.5	3.5	mA
V_{CCLL1} Start Threshold	GATEs switching, COMP charging	4.05	4.40	4.70	V
V_{CCLL1} Stop Threshold	GATEs stop switching, COMP discharging	3.75	4.20	4.60	V
V_{CCLL1} Hysteresis	GATEs not switching, COMP not charging	100	200	300	mV
V_{CCH12} Start Threshold	GATEs switching, COMP charging	1.7	1.9	2.1	V
V_{CCH12} Stop Threshold	GATEs stop switching, COMP discharging	1.55	1.75	1.90	V
V_{CCH12} Hysteresis	GATEs not switching, COMP not charging	100	200	300	mV

5. Guaranteed by design. Not tested in production.

PACKAGE PIN DESCRIPTION

PACKAGE PIN # 28 Lead SO Wide	PIN SYMBOL	FUNCTION
1	COMP	Output of the error amplifier and input for the PWM comparators.
2	V_{FB}	Voltage Feedback Pin. To use Adaptive Voltage Positioning (AVP) select an offset voltage at light load and connect a resistor between V_{FB} and V_{OUT}. The input bias current of the V_{FB} pin and the resistor value determine output voltage offset for zero output current. Short V_{FB} to V_{OUT} for no AVP.
3	V_{DRP}	Current sense output for AVP. The offset of this pin above the DAC voltage is proportional to the output current. Connect a resistor from this pin to V_{FB} to set amount AVP or leave this pin open for no AVP.
4–6	CS1–CS3	Current sense amplifier inputs. Connect current sense network for the corresponding phase to each input.
7	CS_{REF}	Reference for current sense amplifiers. To balance input offset voltages between the inverting and noninverting inputs of the current sense amplifiers, connect a resistor between CS_{REF} and the output voltage. The value should be 1/3 of the value of the resistors connected to the CSx pins.
8–12	VID4–VID0	Voltage ID DAC inputs. These pins are internally pulled up to 3.3 V if left open.
13	I_{LIM}	Sets threshold for current limit. Connect to reference through a resistive divider.

PACKAGE PIN DESCRIPTION (continued)

PACKAGE PIN # 28 Lead SO Wide	PIN SYMBOL	FUNCTION
14	REF	Reference output. Decouple with 0.1 μF to GndL2
15	V_{CCH3}	Power for Gate(H)3.
16	Gate(H)3	High side driver #3.
17	Gnd3	Return for #3 drivers.
18	Gate(L)3	Low side driver #3.
19	V_{CCL23}	Power for Gate(L)2 and Gate(L)3.
20	Gate(L)2	Low side driver #2.
21	GndL2	Return for #2 driver, internal control circuits and IC substrate connection.
22	Gate(H)2	High side driver #2.
23	V_{CCH12}	Power for Gate(H)1 and Gate(H)2. UVLO Sense for High Side Driver supply connects to this pin.
24	Gate(H)1	High side driver #1.
25	Gnd1	Return for #1 drivers.
26	Gate(L)1	Low side driver #1.
27	V_{CCLL1}	Power for internal control circuits and Gate(L)1. UVLO Sense for Logic and Low Side Driver supply connects to this pin.
28	R_{OSC}	A resistor from this pin to ground sets operating frequency and V_{FB} bias current.

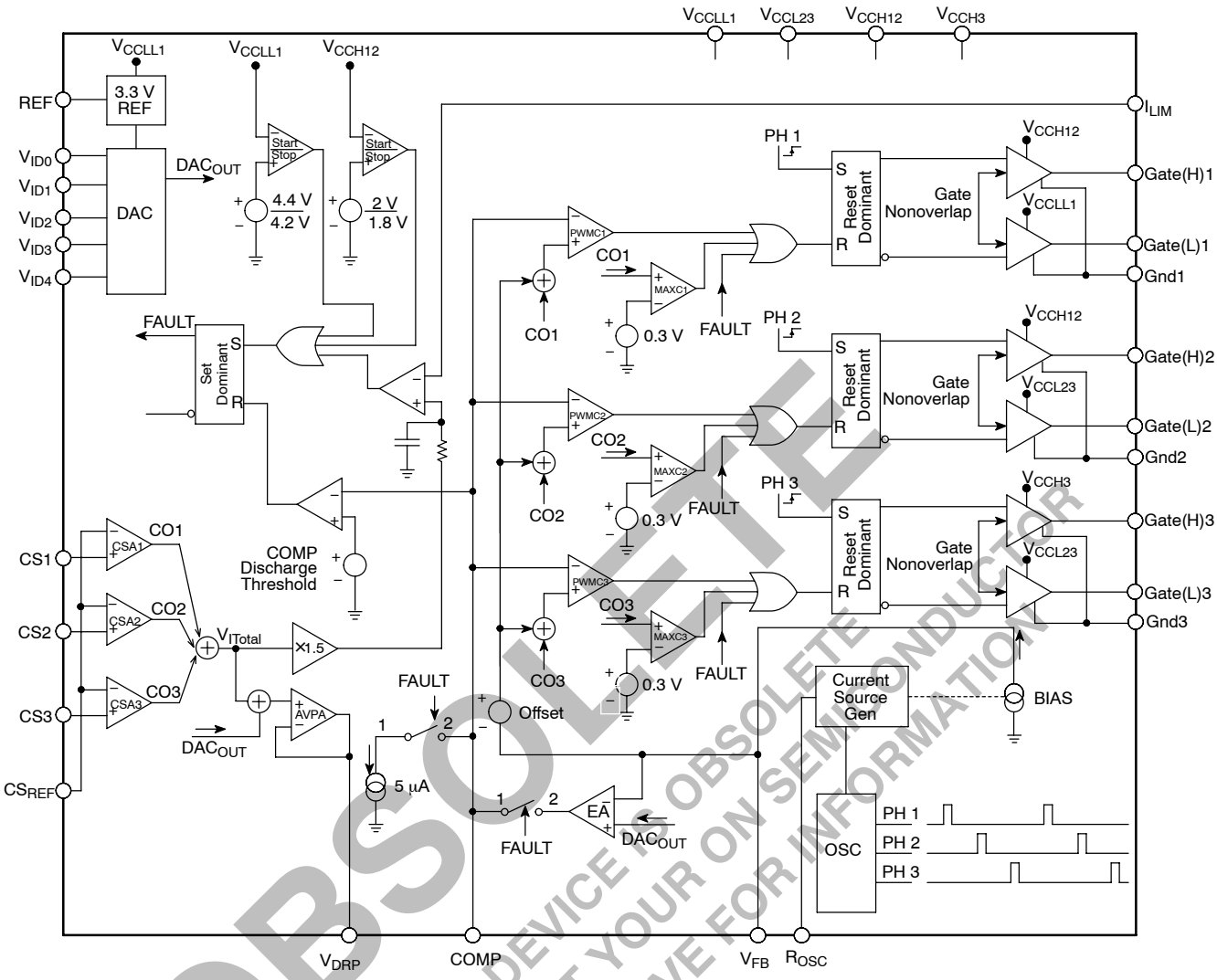


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

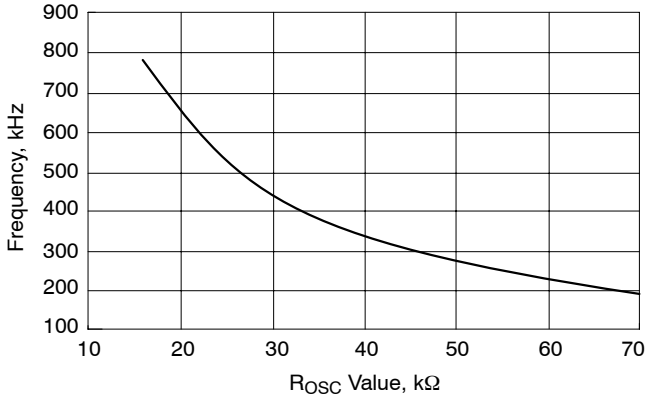


Figure 3. Oscillator Frequency

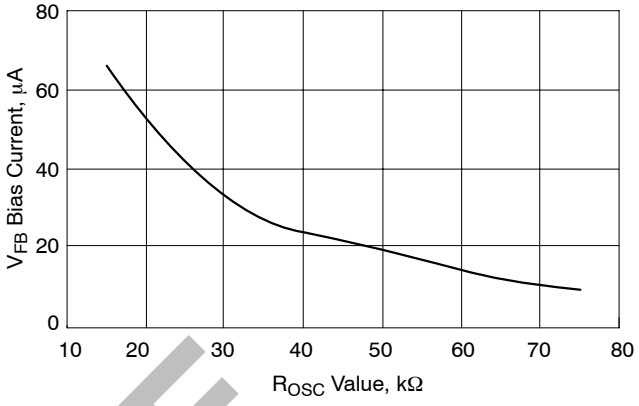


Figure 4. V_{FB} Bias Current vs. R_{OSC} Value

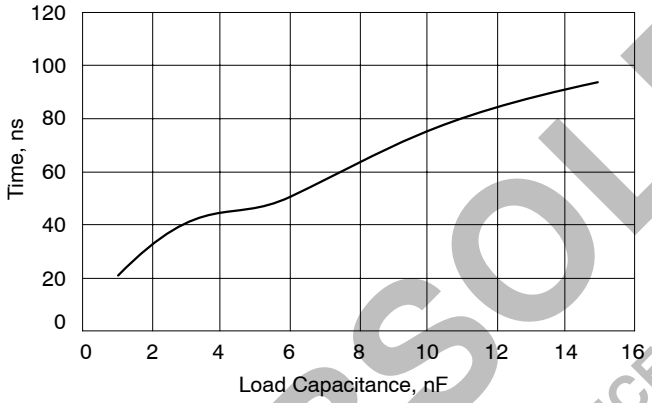


Figure 5. Gate(H) Rise−time vs. Load Capacitance measured from 1 V to 4 V with V_{CC} at 5 V.

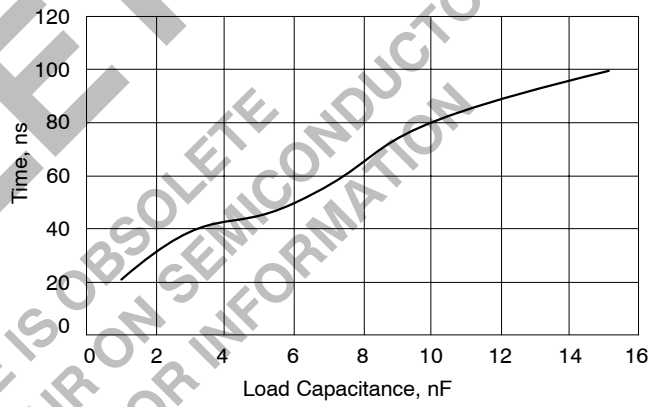


Figure 6. Gate(L) Rise−time vs. Load Capacitance measured from 4 V to 1 V with V_{CC} at 5 V.

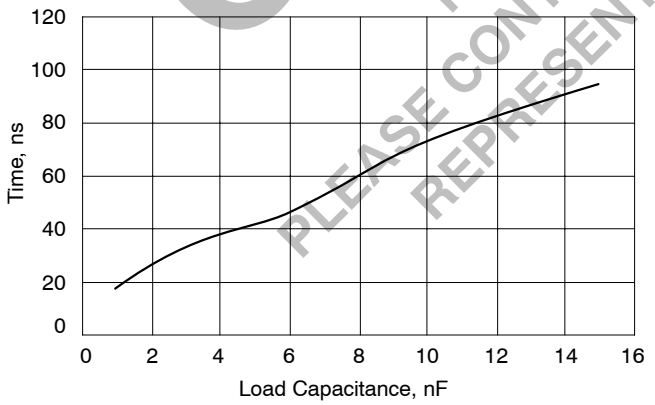


Figure 7. Gate(H) Fall−time vs. Load Capacitance measured from 4 V to 1 V with V_{CC} at 5 V.

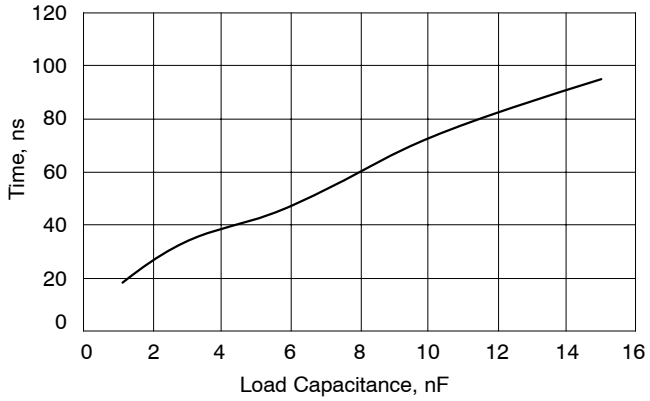


Figure 8. Gate(L) Fall−time vs. Load Capacitance measured from 4 V to 1 V with V_{CC} at 5 V.

APPLICATIONS INFORMATION

FIXED FREQUENCY MULTI−PHASE CONTROL

In a multi−phase converter, multiple converters are connected in parallel and are switched on at different times. This reduces output current from the individual converters and increases the apparent ripple frequency. Because several converters are connected in parallel, output current can ramp up or down faster than a single converter (with the same value output inductor) and heat is spread among multiple components.

The CS5303 uses a three−phase, fixed frequency, enhanced V^2 architecture. Each phase is delayed 120° from the previous phase. Normally GATE(H) transitions high at the beginning of each oscillator cycle. Inductor current ramps up until the combination of the current sense signal and the output ripple trip the PWM comparator and bring GATE(H) low. Once GATE(H) goes low, it will remain low until the beginning of the next oscillator cycle. While GATE(H) is high, the enhanced V^2 loop will respond to line and load transients. Once GATE(H) is low, the loop will not respond again until the beginning of the next cycle. Therefore, constant frequency enhanced V^2 will typically respond within the off−time of the converter.

The enhanced V^2 architecture measures and adjusts current in each phase. An additional input (C_X) for inductor current information has been added to the V^2 loop for each phase as shown in Figure 9.

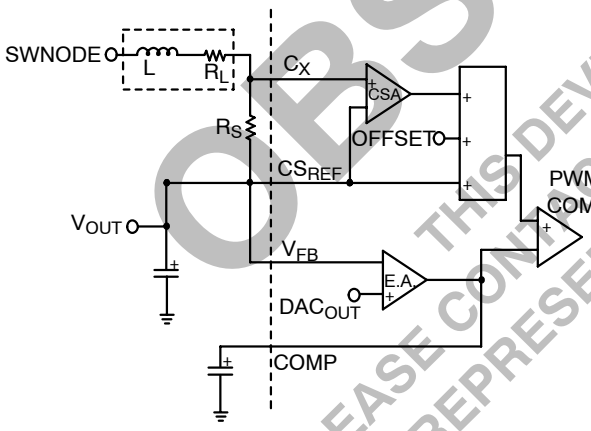


Figure 9. Enhanced V^2 Feedback and Current Sense Scheme

The inductor current is measured across R_S, amplified by CSA and summed with the OFFSET and Output Voltage at the non−inverting input of the PWM comparator. The inductor current provides the PWM ramp and as inductor current increases the voltage on the positive pin of the pwm comparator rises and terminates the pwm cycle. If the inductor starts the cycle with a higher current the PWM cycle will terminate earlier providing negative feedback. The CS5303 provides a C_X input for each phase, but the CS_{REF}, V_{FB} and COMP inputs are common to all phases. Current sharing is accomplished by referencing all phases to the same V_{FB} and COMP pins, so that a phase with a larger current signal will turn off earlier than phases with a smaller current signal.

Including both current and voltage information in the feedback signal allows the open loop output impedance of the power stage to be controlled. If the COMP pin is held steady and the inductor current changes there must also be a change in the output voltage. Or, in a closed loop configuration when the output current changes, the COMP pin must move to keep the same output voltage. The required change in the output voltage or COMP pin depends on the scaling of the current feedback signal and is calculated as

$$\Delta V = R_S \times \text{CSA Gain} \times \Delta I$$

The single−phase power stage output impedance is;

$$\text{Single Stage Impedance} = \Delta V/\Delta I = R_S \times \text{CSA Gain}.$$

The multi−phase power stage output impedance is the single−phase output impedance divided by the number of phases. The output impedance of the power stage determines how the converter will respond during the first few μs of a transient before the feedback loop has repositioned the COMP pin.

The peak output current of each phase can also be calculated from;

$$I_{pkout\ (per\ phase)} = \frac{V_{COMP} - V_{FB} - V_{OFFSET}}{R_S \times \text{CSA Gain}}$$

Figure 10 shows the step response of a single phase with the COMP pin at a fixed level. Before T1 the converter is in normal steady state operation. The inductor current provides the pwm ramp through the Current Share Amplifier. The pwm cycle ends when the sum of the current signal, voltage signal and OFFSET exceed the level of the COMP pin. At T1 the output current increases and the output voltage sags. The next pwm cycle begins and the cycle continues longer than previously while the current signal increases enough to make up for the lower voltage at the V_{FB} pin and the cycle ends at T2. After T2 the output voltage remains lower than at light load and the current signal level is raised so that the sum of the current and voltage signal is the same as with the original load. In a closed loop system the COMP pin would move higher to restore the output voltage to the original level.

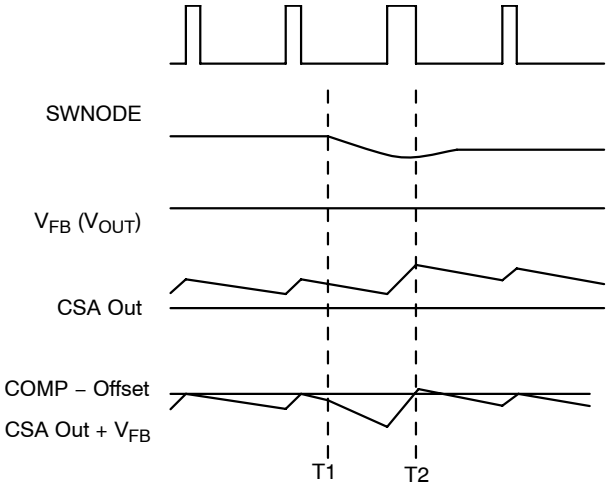


Figure 10. Open Loop Operation

Inductive Current Sensing

For lossless sensing current can be sensed across the inductor as shown below in Figure 11. In the diagram L is the output inductance and R_L is the inherent inductor resistance. To compensate the current sense signal the values of R1 and C1 are chosen so that $L/R_L = R1 \times C1$. If this criteria is met the current sense signal will be the same shape as the inductor current, the voltage signal at Cx will represent the instantaneous value of inductor current and the circuit can be analyzed as if a sense resistor of value R_L was used as a sense resistor (R_S).

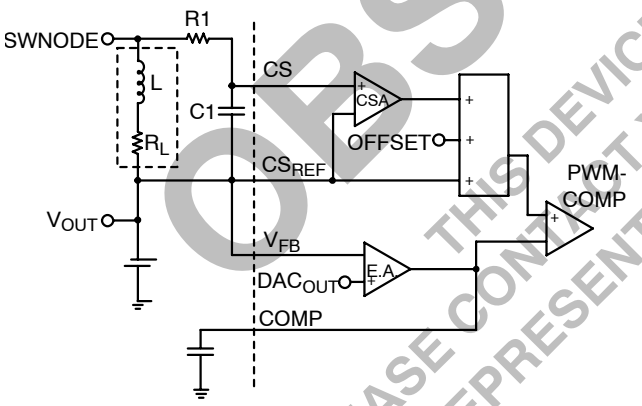


Figure 11. Lossless Inductive Current Sensing with Enhanced V^2

When choosing or designing inductors for use with inductive sensing, tolerances and temperature effects should be considered. Cores with a low permeability material or a large gap will usually have minimal inductance change with temperature and load. Copper magnet wire has a temperature coefficient of 0.39% per °C. The increase in winding resistance at higher temperatures should be considered when setting the I_{LIM} threshold. If a more accurate current sense is required than inductive sensing can provide, current can be sensed through a resistor as shown in Figure 9.

Current Sharing Accuracy

PCB traces that carry inductor current can be used as part of the current sense resistance depending on where the current sense signal is picked off. For accurate current sharing, the current sense inputs should sense the current at the same point for each phase and the connection to the CS_{REF} should be made so that no phase is favored. (In some cases, especially with inductive sensing, resistance of the pcb can be useful for increasing the current sense resistance.) The total current sense resistance used for calculations must include any pcb trace between the CS inputs and the CS_{REF} input that carries inductor current.

Current Sense Amplifier Input Mismatch and the value of the current sense element will determine the accuracy of current sharing between phases. The worst case Current Sense Amplifier Input Mismatch is 5 mV and will typically be within 3 mV. The difference in peak currents between phases will be the CSA Input Mismatch divided by the current sense resistance. If all current sense elements are of equal resistance a 3 mV mismatch with a 2 mΩ sense resistance will produce a 1.5 A difference in current between phases.

Operation at > 50% Duty Cycle

For operation at duty cycles above 50% Enhanced V^2 will exhibit subharmonic oscillation unless a compensation ramp is added to each phase. A circuit like the one on the left side of Figure 12 can be added to each current sense network to implement slope compensation. The value of R1 can be varied to adjust the ramp size.

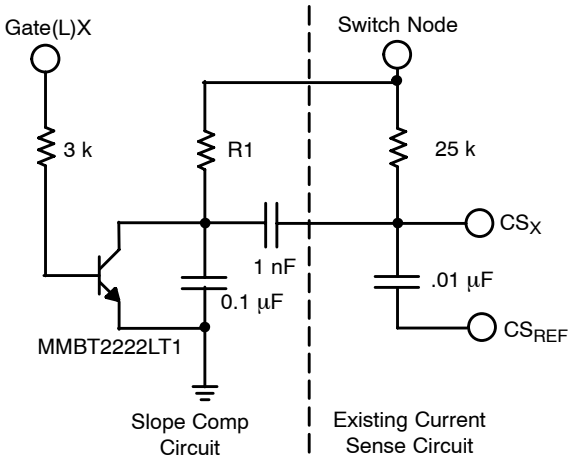


Figure 12. External Slope Compensation Circuit

Ramp Size and Current Sensing

Because the current ramp is used for both the PWM ramp and to sense current, the inductor and sense resistor values will be constrained. A small ramp will provide a quick transient response by minimizing the difference over which the COMP pin must travel between light and heavy loads, but a steady state ramp of 25 mV_{P-P} or greater is typically required to prevent pulse skipping and minimize pulse width jitter. For resistive current sensing the combination of the inductor and sense resistor values must be chosen to provide a large enough steady state ramp. For large inductor values the sense resistor value must also be increased.

For inductive current sensing the RC network must meet the requirement of $L/R_L = R \times C$ to accurately sense the AC and DC components of the current the signal. Again the values for L and R_L will be constrained in order to provide a large enough steady state ramp with a compensated current sense signal. A smaller L, or a larger R_L than optimum might be required. But unlike resistive sensing, with inductive sensing small adjustments can be made easily with the values of R and C to increase the ramp size if needed.

If RC is chosen to be smaller (faster) than L/R_L, the AC portion of the current sensing signal will be scaled larger than the DC portion. This will provide a larger steady state ramp, but circuit performance will be affected and must be evaluated carefully. The current signal will overshoot during transients and settle at the rate determined by $R \times C$. It will eventually settle to the correct DC level, but the error will decay with the time constant of $R \times C$. If this error is excessive it will effect transient response, adaptive positioning and current limit. During transients the COMP pin will be required to overshoot along with the current signal in order to maintain the output voltage. The V_{DRP} pin will also overshoot during transients and possibly slow the response. Single phase overcurrent will trip earlier than it would if compensated correctly and hiccup mode current limit will have a lower threshold for fast rise step loads than for slowly rising output currents.

The waveforms in Figure 13 show a simulation of the current sense signal and the actual inductor current during a positive step in load current with values of L = 500 nH, R_L = 1.6 mΩ, R1 = 20 k and C1 = .01 μF. For ideal current signal compensation the value of R1 should be 31 kΩ. Due to the faster than ideal RC time constant there is an overshoot of 50% and the overshoot decays with a 200 μs time constant. With this compensation the I_{LIM} pin threshold must be set more than 50% above the full load current to avoid triggering hiccup mode during a large output load step.

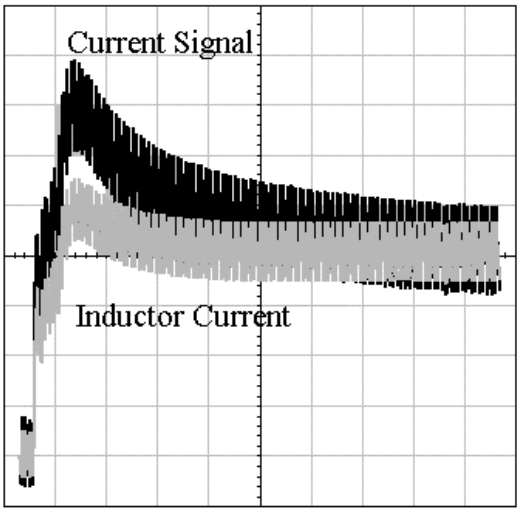


Figure 13. Inductive Sensing waveform during a Step with Fast RC Time Constant (50 μs/div)

Current Limit

Two levels of overcurrent protection are provided. Any time the voltage on a Current Sense pin exceeds CS_{REF} by more than the Single Phase Pulse by Pulse Current Limit, the pwm comparator for that phase is turned off. This provides fast peak current protection for individual phases. The outputs of all the currents are also summed and filtered to compare an averaged current signal to the voltage on the I_{LIM} pin. If this voltage is exceeded, the fault latch trips and the SS capacitor is discharged by a 5 μA source until the COMP pin reaches 0.2 V. Then soft−start begins. The converter will continue to operate in this mode until the fault condition is corrected.

Overvoltage Protection

Overvoltage protection (OVP) is provided as a result of the normal operation of the enhanced V^2 control topology with synchronous rectifiers. The control loop responds to an overvoltage condition within 400 ns, causing the top MOSFET's to shut off, and the synchronous MOSFET's to turn on. This results in a "crowbar" action to clamp the output voltage and prevents damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low.

Transient Response and Adaptive Positioning

For applications with fast transient currents the output filter is frequently sized larger than ripple currents require in

order to reduce voltage excursions during transients. Adaptive voltage positioning can reduce peak−peak output voltage deviations during load transients and allow for a smaller output filter. The output voltage can be set higher at light loads to reduce output voltage sag when the load current is stepped up and set lower during heavy loads to reduce overshoot when the load current is stepped up. For low current applications a droop resistor can provide fast accurate adaptive positioning. However at high currents, the loss in a droop resistor becomes excessive. For example; in a 50 A converter a 1 mΩ resistor to provide a 50 mV change in output voltage between no load and full load would dissipate 2.5 Watts.

Lossless adaptive positioning is an alternative to using a droop resistor, but must respond quickly to changes in load current. Figure 14 shows how adaptive positioning works. The waveform labeled normal shows a converter without adaptive positioning. On the left, the output voltage sags when the output current is stepped up and later overshoots when current is stepped back down. With fast (ideal) adaptive positioning the peak to peak excursions are cut in half. In the slow adaptive positioning waveform the output voltage is not repositioned quickly enough after current is stepped up and the upper limit is exceeded.

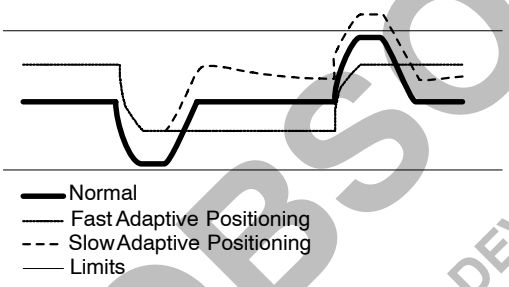


Figure 14. Adaptive Positioning

The CS5303 uses two methods to provide fast and accurate adaptive positioning. For low frequency positioning the V_{FB} and V_{DRP} pins are used to adjust the output voltage with varying load currents. For high frequency positioning, the current sense input pins can be used to control the power stage output impedance. The transition between fast and slow positioning is adjusted by the error amp compensation.

The CS5303 can be configured to adjust the output voltage based on the output current of the converter. The adaptive positioning circuit is designed to select the DAC setting as the maximum output voltage. (Refer to Application Diagram on page 2.)

To set the no−load positioning a resistor (R9) is placed between the output voltage and V_{FB} pin. The V_{FB} bias current will develop a voltage across the resistor to decrease the output voltage. The V_{FB} bias current is dependent on the value of ROSC. See Figure 4 on the datasheet.

During no load conditions the V_{DRP} pin is at the same voltage as the V_{FB} pin, so none of the V_{FB} bias current flows through the V_{DRP} resistor (R8). When output current increases the V_{DRP} pin increases proportionally and the V_{DRP} pin current offsets the V_{FB} bias current and causes the output voltage to further decrease.

The V_{FB} and V_{DRP} pins take care of the slower and DC voltage positioning. The first few μs are controlled primarily by the ESR and ESL of the output filter. The transition between fast and slow positioning is controlled by the ramp size and the error amp compensation. If the ramp size is too large or the error amp too slow there will be a long transition to the final voltage after a transient. This will be most apparent with lower capacitance output filters.

Note: Large levels of adaptive positioning can cause pulse width jitter.

Error Amp Compensation

The transconductance error amplifier can be configured to provide both a slow soft−start and a fast transient response. C4 in the main applications diagram controls soft−start. A 0.1 μF capacitor with the 30 μA error amplifier output capability will allow the output to ramp up at 0.3 V/ms or 1.5 V in 5 ms.

R10 is connected in series with C4 to allow the error amplifier to slew quickly over a narrow range during load transients. Here the 30 μA error amplifier output capability works against 10 kΩ (R10) to limit the window of fast slewing too 300 mV − enough to allow for fast transients, but not enough to interfere with soft−start. This window will be noticeable as a step in the COMP pin voltage at start−up. The size of this step must be kept smaller than the Channel Start−Up Offset (nominally 0.4 V) for proper soft−start operation. If adaptive positioning is used the R9 and R8 form a divider with the V_{DRP} end held at the DAC voltage during start−up, which effectively makes the Channel Start−Up Offset larger.

C12 is included for error amp stability. A capacitive load is required on the error amp output. Use of values less than 1 nF may result in error amp oscillation of several MHz.

C11 and the parallel resistance of the V_{FB} resistor (R9) and the V_{DRP} resistor (R8) are used to roll off the error amp gain. The gain is rolled off at a high enough frequency to give a quick transient response, but low enough to cross zero dB well below the switching frequency to minimize ripple and noise on the COMP pin.

UVLO

The CS5303 has undervoltage lockout functions connected to two pins. One intended for the logic and low−side drivers with a 4.4 V turn−on threshold is connected to the V_{CCLL1} pin. A second for the high side drivers has a 2 V threshold and is connected to the V_{CCH12} pin.

The UVLO threshold for the high side drivers was chosen at a low value to allow for flexibility in the part and an input voltage as low as 3.3 V. In many applications this will be

disabled or will only check that the applicable supply is on – not that it is at a high enough voltage to run the converter.

For the 12 V_{IN} converter in the application diagram on page 2 the UVLO pin for the high side driver is pulled up by the 5 V supply (through two diode drops) and the function is not used. The diode between the COMP pin and the 12 V supply holds the COMP pin near Gnd and prevents start−up while the 12 V supply is off. In an application where a higher UVLO threshold is necessary a circuit like the one in Figure 15 will lock out the converter until the 12 V supply exceeds 9 V.

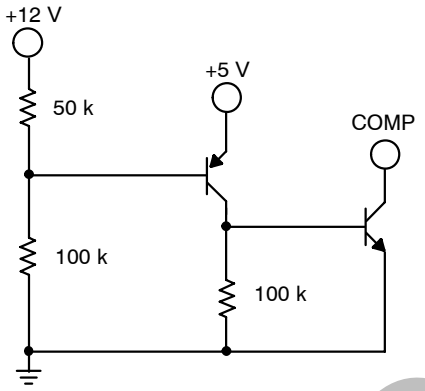


Figure 15. External UVLO Circuit

Layout Guidelines

With the fast rise, high output currents of microprocessor applications parasitic inductance and resistance should be considered when laying out the power, filter and feedback signal sections of the board. Typically a multi−layer board with at least one ground plane is recommended. If the layout is such that high currents can exist in the ground plane underneath the controller or control circuitry, the ground plane can be slotted to reroute the currents away from the controller. The slots should typically not be placed between the controller and the output voltage or in the return path of the gate drive. Additional power and ground planes or islands can be added as required for a particular layout.

Output filter components should be placed on wide planes connected directly to the load to minimize resistive drops during heavy loads and inductive drops and ringing during transients. If required, the planes for the output voltage and return can be interleaved to minimize inductance between the filter and load.

Voltage feedback should be taken from a point of the output or the output filter that doesn't favor any one phase. If the feedback connection is closer to one inductor than the others the ripple associated with that phase may appear larger than the ripple associated with the other phases and poor current sharing can result.

The current sense signal is typically tens of milli−volts. Noise pick−up should be avoided wherever possible. Current feedback traces should be routed away from noisy areas such as switch nodes and gate drive signals. The paths should be matched as well as possible. It is especially important that all current sense signals be picked off at similar points for accurate current sharing. If the current signal is taken from a place other than directly at the inductor any additional resistance between the pick−off point and the inductor appears as part of the inherent inductor resistance and should be considered in design calculations. Capacitors for the current feedback networks should be placed as close to the current sense pins as practical.

DESIGN PROCEDURE

Current Sensing, Power Stage and Output Filter Components

1. Choose the output filter components to meet peak transient requirements. The formula below can be used to provide an approximate starting point for capacitor choice, but will be inadequate to calculate actual values.

$$\Delta V_{PEAK} = (\Delta I/\Delta T) \times ESL + \Delta I \times ESR$$

Ideally the output filter should be simulated with models including ESR, ESL, circuit board parasitics and delays due to switching frequency and converter response. Typically both bulk capacitance (electrolytic, Oscon, etc.) and low impedance capacitance (ceramic chip) will be required. The bulk capacitance provides "hold up" during the converter response. The low impedance capacitance reduces steady state ripple and bypasses the bulk capacitance during slewing of output current.

2. For inductive current sensing (only) choose the current sense network RC to provide a 25 mV minimum ramp during steady state operation.

$$R = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}/V_{IN}}{F \times C \times 25\ mV}$$

Then choose the inductor value and inherent resistance to satisfy $L/R_L = R \times C$.

For ideal current sense compensation the ratio of L and R_L is fixed, so the values of L and R_L will be a compromise typically with the maximum value R_L limited by conduction losses or inductor temperature rise and the minimum value of L limited by ripple current.

3. For resistive current sensing choose L and R_S to provide a steady state ramp greater than 25 mV.

$$L/R_S = (V_{IN} - V_{OUT}) \times T_{ON}/25\ mV$$

Again the ratio of L and R_L is fixed and the values of L and R_S will be a compromise.

4. Calculate the high frequency output impedance (ConverterZ) of the converter during transients. This is the impedance of the Output filter ESR in parallel with the power stage output impedance (PwrstgZ) and will indicate how far from the original level (ΔVR) the output voltage will typically recover to within one switching cycle. For a good transient response ΔVR should be less than the peak output voltage overshoot or undershoot.

$$\Delta VR = ConverterZ \times ESR$$

$$ConverterZ = \frac{PwrstgZ \times ESR}{PwrstgZ + ESR}$$

where:

$$PwrstgZ = R_S \times CSA\ Gain/3$$

Multiply the converterZ by the output current step size to calculate where the output voltage should recover to within the first switching cycle after a transient. If the ConverterZ is higher than the value required to recover to where the adaptive positioning is set the remainder of the recovery will be controlled by the error amp compensation and will typically recover in 10 – 20 μs.

$$\Delta VR = \Delta I_{OUT} \times ConverterZ$$

Make sure that ΔVR is less than the expected peak transient for a good transient response.

5. Adjust L and R_L or R_S as required to meet the best combination of transient response, steady state output voltage ripple and pulse width jitter.

Current Limit

When the sum of the Current Sense amplifiers (V_{ITOTAL}) exceeds the voltage on the I_{LIM} pin the part will enter hiccup mode. For inductive sensing the I_{LIM} pin voltage should be set based on the inductor resistance (or current sense resistor) at max temperature and max current. To set the level of the I_{LIM} pin:

6. $V_{I(LIM)} = R \times I_{OUT(LIM)} \times CS\ to\ I_{LIM}\ Gain$

where:

R is R_L or R_S;

$I_{OUT(LIM)}$ is the current limit threshold.

For the overcurrent to work properly the inductor time constant (L/R) should be ≤ the Current sense RC. If the RC is too fast, during step loads the current waveform will appear larger than it is (typically for a few hundred μs) and may trip the current limit at a level lower than the DC limit.

Adaptive Positioning

7. To set the amount of voltage positioning below the DAC setting at no load connect a resistor ($R_{V(FB)}$) between the output voltage and the V_{FB} pin. Choose $R_{V(FB)}$ as:

$$R_{V(FB)} = NL\ Position/V_{FB}\ Bias\ Current$$

See Figure 4 for V_{FB} Bias Current.

8. To set the difference in output voltage between no load and full load, connect a resistor ($R_{V(DRP)}$) between the V_{DRP} and V_{FB} pins. $R_{V(DRP)}$ can be calculated in two steps. First calculate the difference between the V_{DRP} and V_{FB} pin at full load. (The V_{FB} voltage should be the same as the DAC voltage during closed loop operation.) Then choose the $R_{V(DRP)}$ to source enough current across $R_{V(FB)}$ for the desired change in output voltage.

$$\Delta V_{V(DRP)} = I_{OUTFL} \times R \times CS\ to\ V_{DRP}\ Gain$$

where:

R = R_L or R_S for one phase;

I_{OUTFL} is the full load output current.

$$R_{V(DRP)} = \Delta V_{DRP} \times R_{V(FB)}/\Delta V_{OUT}$$

DESIGN EXAMPLE

Choose the component values for lossless current sensing, adaptive positioning and current limit for a 60 A converter. The adaptive positioning is chosen 50 mV below the maximum V_{OUT} at no load and 50 mV below the no−load position with 60 A out. The peak output voltage transient is 100 mV max during a 60 A step current. The overcurrent limit is nominally 75 A.

Current Sensing, Power Stage and Output Filter Components

1. Assume 1.5 mΩ of output filter ESR.
2. $R = (V_{IN} - V_{OUT}) \times (V_{OUT}/V_{IN})/(F \times C \times 25\ mV)$
   $= (12 - 1.5) \times (1.5/12)/(250\ k \times .01\ \mu F \times 25\ mV)$
   $= 21\ k\Omega \Rightarrow$ Choose 20 kΩ
   $L/R_L = .01\ \mu F \times 20\ k\Omega = 200\ \mu s$
   Choose $R_L = 2\ m\Omega$
   $L = 2\ m\Omega \times 200\ \mu s = 400\ nH$
3. n/a
4. $PwrstgZ = R_L \times CSA\ Gain/3$
   $= 1.5\ m\Omega \times 4.2/3 = 2.1\ m\Omega$

$$ConverterZ = \frac{PwrstgZ \times ESR}{PwrstgZ + ESR} = \frac{2.8\ m\Omega \times 1.5\ m\Omega}{2.8\ m\Omega + 1.5\ m\Omega} \cong 1\ m\Omega$$

$\Delta VR = 1.2\ m\Omega \times 60\ A = 60\ mV$

5. n/a

Current Limit

6. $V_{I(LIM)} = R_L \times I_{OUT(LIM)} \times$ CS to I_{LIM} Gain
$= 1.5\ m\Omega \times 75\ A \times 6.5 = 731\ mV$

Adaptive Positioning

7. $R_{V(FB)}$ = NL Position/V_{FB} Bias Current
$= 50\ mV/19\ \mu A = 2.63\ k\Omega$

8. $\Delta V_{DRP} = R_L \times I_{OUT} \times$ Current Sense to V_{DRP} Gain
$= 2\ m\Omega \times 60\ A \times 3 = 360\ mV$

$R_{V(DRP)} = \Delta V_{DRP} \times R_{V(FB)}/\Delta V_{OUT}$
$= 360\ mV \times 2.63\ k\Omega/50\ mV = 18.9\ k\Omega$

ADDITIONAL APPLICATION DIAGRAMS

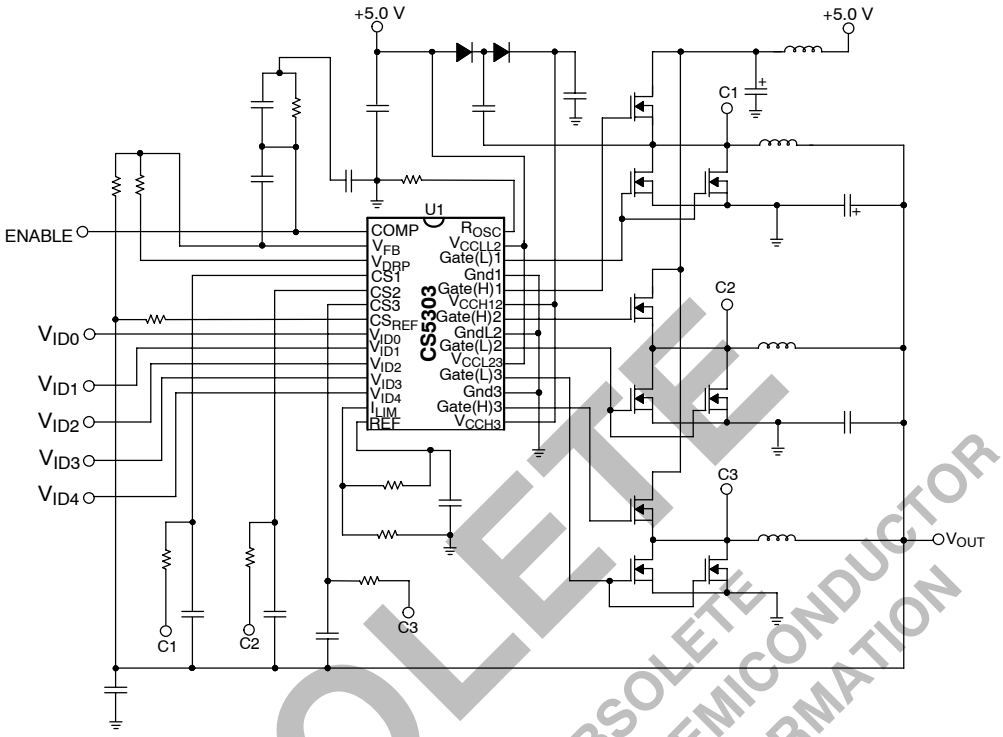


Figure 16. 5 V only to 1.2 V

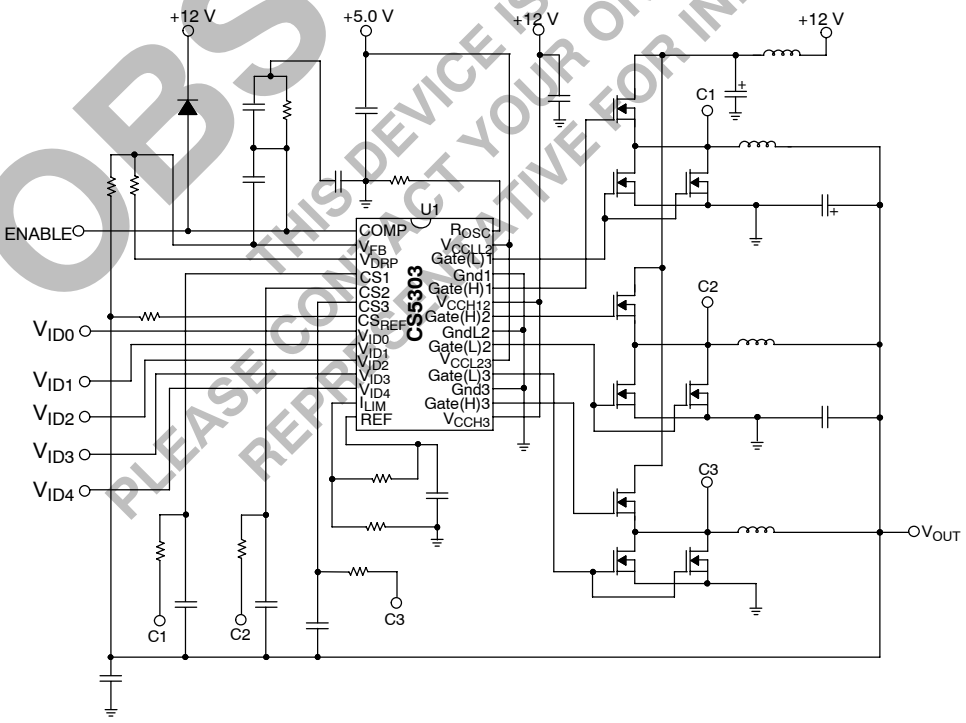


Figure 17. 5 V to 1.2 V with 12 V Bias

ADDITIONAL APPLICATION DIAGRAMS

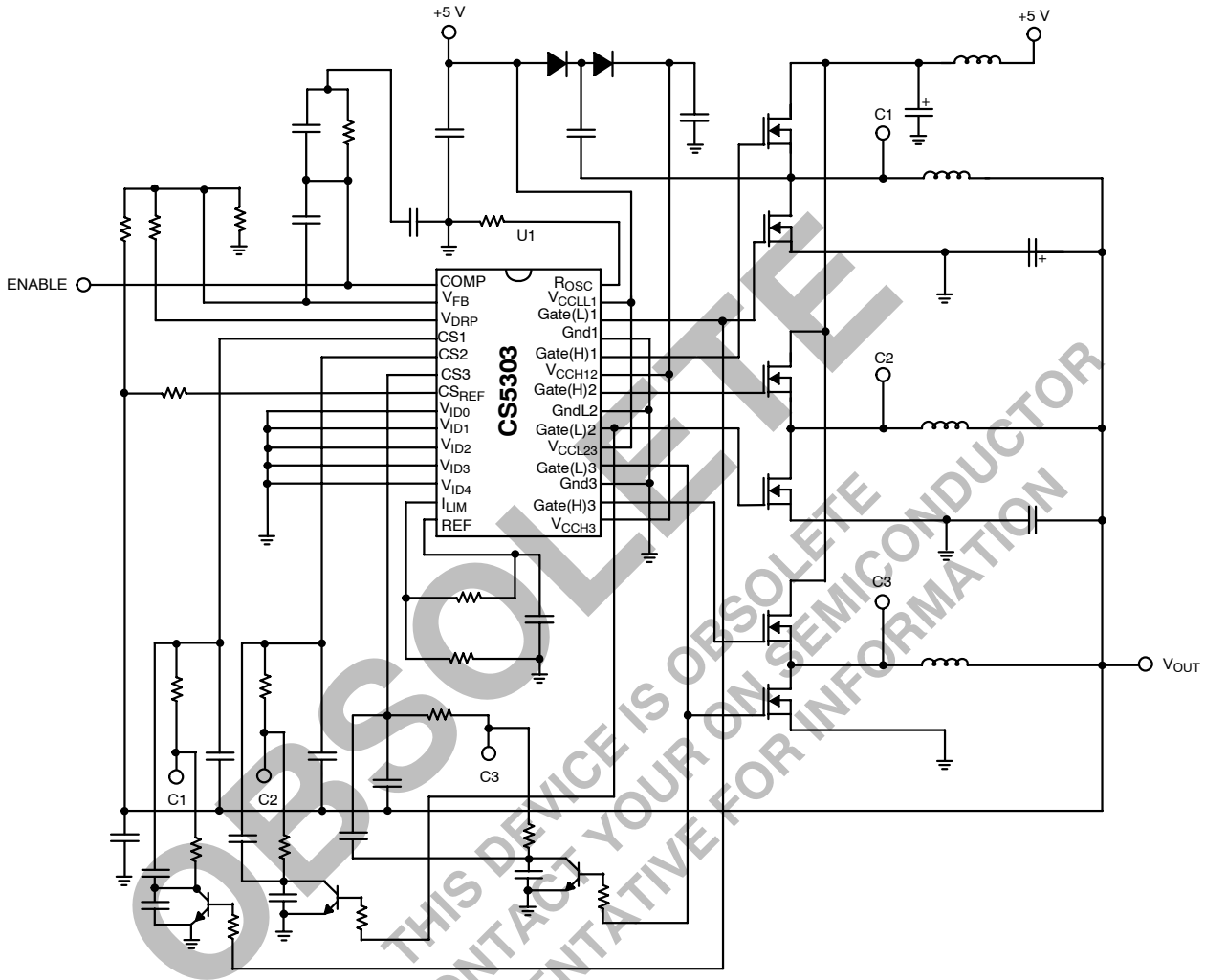


Figure 18. 5 V only to 2.5 V

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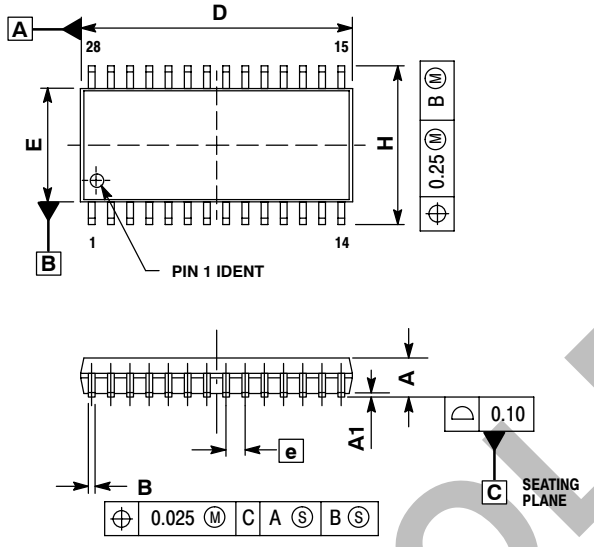

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A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

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