**CM3202-00**

**DDR VDDQ and VTT Termination Voltage Regulator**

**Product Description**

The CM3202-00 is a dual-output low noise linear regulator designed to meet SSTL-2 and SSTL-3 specifications for DDR-SDRAM $V_{DDQ}$ supply and termination voltage $V_{TT}$ supply. With integrated power MOSFETs, the CM3202-00 can source up to 2 A of $V_{DDQ}$ continuous current, and source or sink up to 2 A $V_{TT}$ continuous current. The typical dropout voltage for $V_{DDQ}$ is 500 mV at 2 A load current.

The CM3202-00 provides fast response to transient load changes. Load regulation is excellent, from no load to full load. It also has built-in over-current limits and thermal shutdown at 170°C.

The CM3202-00 supports Suspend–To–RAM (STR) and ACPI compliance with shutdown mode which tri–states $V_{TT}$ to minimize quiescent system current.

The CM3202-00 is packaged in an easy–to–use WDFN8. Low thermal resistance allows it to withstand high power dissipation at 85°C ambient. It operates over the industrial ambient temperature range of –40°C to 85°C.

**Features**

- Two Linear Regulators
  - Maximum 2 A Current from $V_{DDQ}$
  - Source and Sink Up to 2 A $V_{TT}$ Current
- 1.7 V to 2.8 V Adjustable $V_{DDQ}$ Output Voltage
- 500 mV Typical $V_{DDQ}$ Dropout Voltage at 2 A
- $V_{TT}$ Tracking at 50% of $V_{DDQ}$
- Excellent Load and Line Regulation, Low Noise
- Fast Transient Response
- Meet JEDEC DDR–I and DDR–II Memory Power Spec.
- Linear Regulator Design Requires No Inductors and Has Low External Component Count
- Integrated Power MOSFETs
- Dual Purpose ADJ/Shutdown Pin
- Built–In Over–Current Limit and Thermal Shutdown for $V_{DDQ}$ and $V_{TT}$
- Fast Transient Response
- Low Quiescent Current
- These Devices are Pb–Free and are RoHS Compliant

**Applications**

- DDR Memory and Active Termination Buses
- Desktop Computers, Servers
- Residential and Enterprise Gateways
- DSL Modems
- Routers and Switchers
- DVD Recorders
- 3D AGP Cards
- LCD TV and STB

**MARKING DIAGRAM**

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Shipping†</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM3202–00DE</td>
<td>WDFN8</td>
<td>3000/Tape &amp; Reel</td>
</tr>
</tbody>
</table>

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
TYPICAL APPLICATION

VIN = 3.3 V to 3.6 V

CM3202

VTT = 1.25 V/2 A

VDDQ = 2.5 V/2 A

FUNCTIONAL BLOCK DIAGRAM
Table 1. PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Lead(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN</td>
<td>Input supply voltage pin. Bypass with a 220 μF capacitor to GND.</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>Not internally connected. For better heat flow, connect to GND (exposed pad).</td>
</tr>
<tr>
<td>3</td>
<td>VTT</td>
<td>VTT regulator output pin, which is preset to 50% of VDDQ.</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>Not internally connected. For better heat flow, connect to GND (exposed pad).</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground pin (analog).</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>Ground pin (power).</td>
</tr>
<tr>
<td>7</td>
<td>ADJS</td>
<td>This pin is for VDDQ output voltage adjustment. It is available as long as VDDQ is enabled. During Manual/Thermal shutdown, it is tightened to GND. The VDDQ output voltage is set using an external resistor divider connected to ADJSD: VDDQ = 1.25 V \times \left(\frac{R1 + R2}{R2}\right) Where R1 is the upper resistor and R2 is the ground–side resistor. In addition, the ADJSD pin functions as a Shutdown pin. When ADJSD voltage is higher than 2.7 V (SHDN_H), the circuit is in Shutdown mode. When ADJSD voltage is below 1.5 V (SHDN_L), both VDDQ and VTT are enabled. A low–leakage Schottky diode in series with ADJSD pin is recommended to avoid interference with the voltage adjustment setting.</td>
</tr>
<tr>
<td>8</td>
<td>VDDQ</td>
<td>VDDQ regulator output voltage pin.</td>
</tr>
<tr>
<td>EPad</td>
<td>GND</td>
<td>The backside exposed pad which serves as the package heatsink. Must be connected to GND.</td>
</tr>
</tbody>
</table>
# SPECIFICATIONS

## Table 2. ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN to GND</td>
<td>[GND – 0.3] to +6.0</td>
<td>V</td>
</tr>
<tr>
<td>Pin Voltages</td>
<td>[GND – 0.3] to +6.0</td>
<td>V</td>
</tr>
<tr>
<td>VDDQ, VTT to GND</td>
<td>[GND – 0.3] to +6.0</td>
<td>V</td>
</tr>
<tr>
<td>ADJSD to GND</td>
<td>[GND – 0.3] to +6.0</td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td>2.0 / ±2.0</td>
<td>A</td>
</tr>
<tr>
<td>VDDQ / VTT, Continuous (Note 1)</td>
<td>2.0 / ±2.0</td>
<td>A</td>
</tr>
<tr>
<td>VDDQ / VTT, Peak</td>
<td>2.8 / ±2.8</td>
<td>A</td>
</tr>
<tr>
<td>VDDQ Source + VTT Source</td>
<td>3</td>
<td>A</td>
</tr>
<tr>
<td>Temperature</td>
<td>–40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Operating Ambient</td>
<td>–40 to +170</td>
<td>°C</td>
</tr>
<tr>
<td>Storage</td>
<td>–40 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Resistance, RJJA (Note 2)</td>
<td>55</td>
<td>°C / W</td>
</tr>
<tr>
<td>WDFN8, 3 mm x 3 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous Power Dissipation (Note 2)</td>
<td>2.6 / 1.5</td>
<td>W</td>
</tr>
<tr>
<td>WDFN8, T_A = 25°C / 85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD Protection (HBM)</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec)</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Despite the fact that the device is designed to handle large continuous/peak output currents, it is not capable of handling these under all conditions. Limited by the package thermal resistance, the maximum output current of the device cannot exceed the limit imposed by the maximum power dissipation value.
2. Measured with the package using a 4 in² / 2 layers PCB with thermal vias.

## Table 3. STANDARD OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Operating Temperature Range</td>
<td>–40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>VDDQ Regulator</td>
<td>3.1 to 3.6</td>
<td>V</td>
</tr>
<tr>
<td>DDR–1 Supply Voltage, VIN</td>
<td>0 to 2</td>
<td>A</td>
</tr>
<tr>
<td>Load Current, Continuous</td>
<td>2.5</td>
<td>A</td>
</tr>
<tr>
<td>C_DDDQ</td>
<td>220</td>
<td>μF</td>
</tr>
<tr>
<td>VTT Regulator</td>
<td>3.1 to 3.6</td>
<td>V</td>
</tr>
<tr>
<td>DDR–1 Supply Voltage, VIN</td>
<td>0 to ±2.0</td>
<td>A</td>
</tr>
<tr>
<td>Load Current, Continuous</td>
<td>±2.50</td>
<td>A</td>
</tr>
<tr>
<td>C_TTT</td>
<td>220</td>
<td>μF</td>
</tr>
<tr>
<td>V_IN Supply Voltage Range</td>
<td>3.10 to 3.60</td>
<td>V</td>
</tr>
<tr>
<td>VDDQ Source + VTT Source</td>
<td>2.5</td>
<td>A</td>
</tr>
<tr>
<td>Load Current, Continuous</td>
<td>3.5</td>
<td>A</td>
</tr>
<tr>
<td>Junction Operating Temperature Range</td>
<td>–40 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>
### Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>General</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent Current</td>
<td>$I_{DDQ} = 0$, $I_{TT} = 0$</td>
<td>8</td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SHDN}$</td>
<td>Shutdown Current</td>
<td>$V_{ADJSD} = 3.3$ V (Shutdown)</td>
<td>0.1</td>
<td>0.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>SHDN_H</td>
<td>ADJSD Logic High</td>
<td>(Note 2)</td>
<td>2.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SHDN_L</td>
<td>ADJSD Logic Low</td>
<td></td>
<td></td>
<td></td>
<td>1.50</td>
<td>V</td>
</tr>
<tr>
<td>UVLO</td>
<td>Under−Voltage Lockout</td>
<td>Hysteresis = 100 mV</td>
<td>2.40</td>
<td>2.70</td>
<td>2.90</td>
<td>V</td>
</tr>
<tr>
<td>$T_{OVERRIDE}$</td>
<td>Thermal SHDN Threshold</td>
<td></td>
<td>150</td>
<td>170</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$T_{HYS}$</td>
<td>Thermal SHDN Hysteresis</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>TEMPCO</td>
<td>$V_{DDQ}$, $V_{TT}$ TEMP CO</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>ppm/°C</td>
</tr>
<tr>
<td><strong>VDDQ Regulator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DDQ_DEF}$</td>
<td>VDDQ Output Voltage</td>
<td>$I_{DDQ} = 100$ mA</td>
<td>2.450</td>
<td>2.500</td>
<td>2.550</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDQ_LOAD}$</td>
<td>VDDQ Load Regulation</td>
<td>$10$ mA $\leq I_{DDQ} \leq 2$ A (Note 3)</td>
<td>10</td>
<td>25</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{DDQ_LINE}$</td>
<td>VDDQ Line Regulation</td>
<td>$3.1$ V $\leq V_{IN} \leq 3.6$ V, $I_{DDQ} = 0.1$ A</td>
<td>5</td>
<td>25</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{DROP}$</td>
<td>VDDQ Dropout Voltage</td>
<td>$I_{DDQ} = 2$ A (Note 4)</td>
<td>500</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$I_{ADJ}$</td>
<td>ADJSD Bias Current</td>
<td></td>
<td>0.8</td>
<td>3.0</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$I_{DDQ_LIM}$</td>
<td>VDDQ Current Limit</td>
<td></td>
<td>2.0</td>
<td>2.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>VTT Regulator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{TT_DEF}$</td>
<td>VTT Output Voltage</td>
<td>$I_{TT} = 100$ mA</td>
<td>1.225</td>
<td>1.250</td>
<td>1.275</td>
<td>V</td>
</tr>
<tr>
<td>$V_{TT_LOAD}$</td>
<td>VTT Load Regulation</td>
<td>$Source$, $0 \leq I_{TT} \leq 2$ A (Note 3)</td>
<td>10</td>
<td>30</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{TT_LINE}$</td>
<td>VTT Line Regulation</td>
<td>$Sink$, $-2$ A $\leq I_{TT} \leq 0$ (Note 3)</td>
<td>5</td>
<td>15</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$I_{TT_LIM}$</td>
<td>ITT Current Limit</td>
<td>$Source$ / $Sink$ (Note 3)</td>
<td>±2.0</td>
<td>±2.5</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td>$I_{TT_OFF}$</td>
<td>VTT Shutdown Leakage Current</td>
<td>Thermal Shutdown Enabled</td>
<td>10</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
</tbody>
</table>

1. $V_{IN} = 3.3$ V, $V_{DDQ} = 2.50$ V, $V_{TT} = 1.25$ V (default values), $C_{DDQ} = C_{TT} = 47$ μF, $T_A = 25^\circ$C unless otherwise specified.
2. ShDN Logic High value is normally satisfied for full input voltage range by using a low leakage current (below 1 μA). Schottky diode at ADJSD control pin.
3. Load and line regulation are measured at constant junction temperature by using pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account separately. Load and line regulation values are guaranteed up to the maximum power dissipation.
4. Dropout voltage is input to output voltage differential at which output voltage has dropped 100 mV from the nominal value obtained at 3.3 V input. It depends on load current and junction temperature.
APPLICATION INFORMATION

Powering DDR Memory

Double-Data-Rate (DDR) memory has provided a huge step in performance for personal computers, servers and graphic systems. As is apparent in its name, DDR operates at double the data rate of earlier RAM, with two memory accesses per cycle versus one. DDR SDRAM’s transmit data at both the rising and falling edges of the memory bus clock.

DDR’s use of Stub Series Terminated Logic (SSTL) topology improves noise immunity and power-supply rejection, while reducing power dissipation. To achieve this performance improvement, DDR requires more complex power management architecture than previous RAM technology.

Unlike the conventional DRAM technology, DDR SDRAM uses differential inputs and a reference voltage for all interface signals. This increases the data bus bandwidth, and lowers the system power consumption. Power consumption is reduced by lower operating voltage, a lower signal voltage swing associated with Stub Series Terminated Logic (SSTL_2), and by the use of a termination voltage, VTT. SSTL_2 is an industry standard defined in JEDEC document JESD8-9. SSTL_2 maintains high-speed data bus signal integrity by reducing transmission reflections. JEDEC further defines the DDR SDRAM specification in JESD79C.

DDR memory requires three tightly regulated voltages: VDDQ, VTT, and VREF (see Typical DDR terminations, Class II). In a typical SSTL_2 receiver, the higher current VDDQ supply voltage is normally 2.5 V with a tolerance of ±200 mV. The active bus termination voltage, VTT, is half of VDDQ. VREF is a reference voltage that tracks half of VDDQ, ±1%, and is compared with the VTT terminated signal at the receiver. VTT must be within ±40 mV of VREF.
The VTT power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2 mA to achieve the 405 mV minimum over VTT needed at the receiver:

\[ I_{\text{termination}} = \frac{405 \text{ mV}}{R_t(25 \Omega)} = 16.2 \text{ mA} \]

A typical 64 Mbyte SSTL–2 memory system, with 128 terminated lines, has a worst–case maximum VTT supply current up to ±2.07 A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the VTT external capacitor. In a real memory system, the continuous average VTT current level in normal operation is less than ±200 mA.

The VDDQ power supply, in addition to supplying current to the memory banks, could also supply current to controllers and other circuitry. The current level typically stays within a range of 0.5 A to 1 A, with peaks up to 2 A or more, depending on memory size and the computing operations being performed.

The tight tracking requirements and the need for VTT to sink, as well as source, current provide unique challenges for powering DDR SDRAM.

**CM3202–00 Regulator**

The CM3202–00 dual output linear regulator provides all of the power requirements of DDR memory by combining two linear regulators into a single TDFN–8 package. VDDQ regulator can supply up to 2 A current, and the two–quadrant VTT termination regulator has current sink and source capability to ±2 A. The VDDQ linear regulator uses a PMOS pass element for a very low dropout voltage, typically 500 mV at a 2 A output. The output voltage of VDDQ can be set by an external voltage divider. The use of regulators for both the upper and lower side of the VDDQ output allows a fast transient response to any change of the load, from high current to low current or inversely. The second output, VTT, is regulated at VDDQ/2 by an internal resistor divider. Same as VDDQ, VTT has the same fast transient response to load change in both directions. The VTT regulator can source, as well as sink, up to 2 A current. The CM3202–00 is designed for optimal operation from a nominal 3.3 V DC bus, but can work with VIN as high as 5 V. When operating at higher VIN voltages, attention must be given to the increased package power dissipation and proportionally increased heat generation.

VREF is typically routed to inputs with high impedance, such as a comparator, with little current draw. An adequate VREF can be created with a simple voltage divider of precision, matched resistors from VDDQ to ground. A small ceramic bypass capacitor can also be added for improved noise performance.

**Input and Output Capacitors**

The CM3202–00 requires that at least a 220 µF electrolytic capacitor be located near the VIN pin for stability and to maintain the input bus voltage during load transients. An additional 4.7 µF ceramic capacitor between the VIN and the GND, located as close as possible to those pins, is recommended to ensure stability.

At a minimum of a 220 µF electrolytic capacitor is recommended for the VDDQ output. An additional 4.7 µF ceramic capacitor between the VDDQ and GND, located very close to those pins, is recommended.

At a minimum of a 220 µF electrolytic capacitor is recommended for the VTT output. This capacitor should have low ESR to achieve best output transient response. SP or OSCON capacitors provide low ESR at high frequency, and thus are a good choice. In addition, place a 4.7 µF ceramic capacitor between the VTT pin and GND, located very close to those pins. The total ESR must be low enough to keep the transient within the VTT window of 40 mV during the transition for source to sink. An average current step of ±0.5 A requires:

\[ ESR < \frac{40 \text{ mV}}{1 \text{ A}} = 40 \text{ mΩ} \]

Both outputs will remain stable and in regulation even during light or no load conditions.
Adjusting VDDQ Output Voltage

The CM3202–00 internal bandgap reference is set at 1.25 V. The VDDQ voltage is adjustable by using a resistor divider, R1 and R2:

\[ V_{DDQ} = V_{ADJ} \times \frac{R_1 + R_2}{R_2} \]

where \( V_{ADJ} = 1.25 \) V. For best regulator stability, we recommend that R1 and R2 not exceed 10 kΩ each.

Shutdown

ADJSD also serves as a shutdown pin. When this is pulled high (SHDN_H), both the VDDQ and the VTT outputs tri–state and could sink/source less than 10 μA. During shutdown, the quiescent current is reduced to less than 0.5 mA, independent of output load.

It is recommended that a low leakage Schottky diode be placed between the ADJSD Pin and an external shutdown signal to prevent interference with the ADJ pin’s normal operation. When the diode anode is pulled low, or left open, the CM3202–00 is again enabled.

Current Limit, Foldback and Over–temperature Protection

The CM3202–00 features internal current limiting with thermal protection. During normal operation, VDDQ limits the output current to approximately 2 A and VTT limits the output current to approximately +2 A. When VTT is current limiting into a hard short circuit, the output current folds back to a lower level, about 1 A, until the over–current condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the junction temperature of the device exceeds 170°C (typical), the thermal protection circuitry triggers and tri–states both VDDQ and VTT outputs. Once the junction temperature has cooled to below about 120°C the CM3202–00 returns to normal operation.

Thermal Considerations

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (\( \theta_{JA} \)) for device power dissipation (\( P_D \)) primarily consists of two paths in the series. The first path is the junction to the case (\( \theta_{JC} \)) which is defined by the package style and the second path is case to ambient (\( \theta_{CA} \)) thermal resistance which is dependent on board layout. The final operating junction temperature for any condition can be estimated by the following thermal equation:

\[ T_{JUNC} = T_{AMB} + P_D \times (\theta_{JC}) + P_D \times (\theta_{CA}) \]

\[ = T_{AMB} + P_D \times (\theta_{CA}) \]

When a CM3202–00 using WDFN8 package is mounted on a double–sided printed circuit board with four square inches of copper allocated for “heat spreading,” the \( \theta_{JA} \) is approximately 55°C/W. Based on the over temperature limit of 170°C with an ambient temperature of 85°C, the available power of the package will be:

\[ P_D = \frac{170^\circ C - 85^\circ C}{55^\circ C/W} = 1.5 \text{ W} \]
PCB Layout Considerations
The CM3202–00 has a heat spreader attached to the bottom of the WDFN8 package in order for the heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during the manufacturing, the heat will be transferred between the two pads. See the Thermal Layout, the CM3202–00 shows the recommended PCB layout. Please be noted that there are four vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can be resulted in blocking of the solder. The ground and power planes need to be at least 2 square inches of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and not near other heat-dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3202–00 to ambient, $\theta_{JA}$, of approximately 55°C/W.

![Figure 2. Thermal Layout for WDFN8 Package](image-url)
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 2:1

WDFN8 3x3, 0.65P
CASE 511BH–01
ISSUE O

DATE 21 JUL 2010

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIMENSIONS: MILLIMETERS

DIM
MIN
MAX
A
0.70
0.80
A1
0.00
0.05
A3
0.20 REF
b
0.25
0.35
D
3.00 BSC
D2
2.20
2.40
E
3.00 BSC
E2
1.40
1.60
e
0.65 BSC
L
0.20
0.40
L1
—
0.15

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

DIM
MIN
MAX
A
0.70
0.80
A1
0.00
0.05
A3
0.20 REF
b
0.25
0.35
D
3.00 BSC
D2
2.20
2.40
E
3.00 BSC
E2
1.40
1.60
e
0.65 BSC
L
0.20
0.40
L1
—
0.15

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