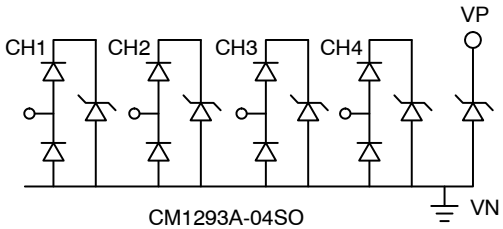
4-Channel Low Capacitance ESD Protection Array

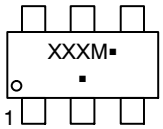
CM1293A-04SO

SC-74
SO SUFFIX
CASE 318F

BLOCK DIAGRAM



MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
CM1293A-04SO	SC-74 (Pb-Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

CM1293A-04SO has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. This device is ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series that steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N which helps protect the V_{CC} rail against ESD strikes. This device protects against ESD pulses up to ±8 kV contact discharge) per the IEC 61000-4-2 Level 4 standard.

This device is particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (FireWire®, i.LINK™), Serial ATA, DVI, HDMI, and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

Features

- Four Channels of ESD Protection
- Provides ESD Protection to IEC61000-4-2
  - ♦ ±8 kV Contact Discharge
- Low Loading Capacitance of 2.0 pF Max
- Low Clamping Voltage
- Channel I/O to I/O Capacitance 1.5 pF Typical
- Zener Diode Protects Supply Rail and Eliminates the Need for External By-Pass Capacitors
- Each I/O Pin Can Withstand over 1000 ESD Strikes*
- This Device is Pb-Free and is RoHS Compliant**

Applications

- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High-Speed Data Line ESD Protection

* Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

* For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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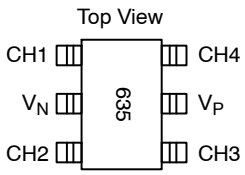
Table 1. PIN DESCRIPTIONS

Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	V_N	GND	Negative Voltage Supply Rail
3	CH2	I/O	ESD Channel
4	CH3	I/O	ESD Channel
5	V_P	PWR	Positive Voltage Supply Rail
6	CH4	I/O	ESD Channel

PACKAGE/PINOUT DIAGRAM



4-Channel SC-74

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Operating Supply Voltage (V_P – V_N)	6.0	V
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–65 to +150	°C
DC Voltage at any Channel Input	(V_N – 0.5) to (V_P + 0.5)	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Unit
Operating Temperature Range	–40 to +85	°C
Package Power Rating	225	mW

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_P	Operating Supply Voltage (V_P–V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P–V_N) = 3.3 V			8.0	μA
V_F	Diode Forward Voltage	I_F = 8 mA, T_A = 25 °C		0.90		V
I_{LEAK}	Channel Leakage Current	T_A = 25°C, V_P = 5 V, V_N = 0 V		±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P = 3.3 V, V_N = 0 V, V_{IN} = 1.65 V			2.0	pF
ΔC_{IO}	Channel I/O to I/O Capacitance			1.5		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any Channel Input, in System Contact Discharge per IEC 61000-4-2 Standard	T_A = 25°C (Notes 2 and 3)	±8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A = 25 °C, I_{PP} = 1 A, t_P = 8/20 μS (Note 3)		 +9.9 –1.6		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	T_A = 25 °C, I_{PP} = 1A, t_P = 8/20 μS (Note 3)		 0.96 0.5		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. All parameters specified at T_A = –40 °C to +85 °C unless otherwise noted.
2. Standard IEC 61000-4-2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω, V_P = 3.3 V, V_N grounded.
3. These measurements performed with no external capacitor on V_P.

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PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

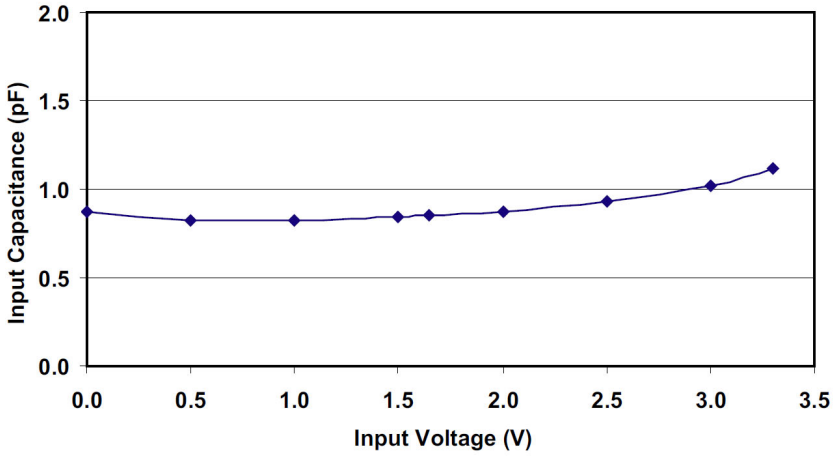

Figure 1. Typical Variation of C_{IN} vs. V_{IN}
(f = 1 MHz, V_P = 3.3 V, V_N = 0 V, 0.1 μF Chip Capacitor between V_P and V_N, 25°C)

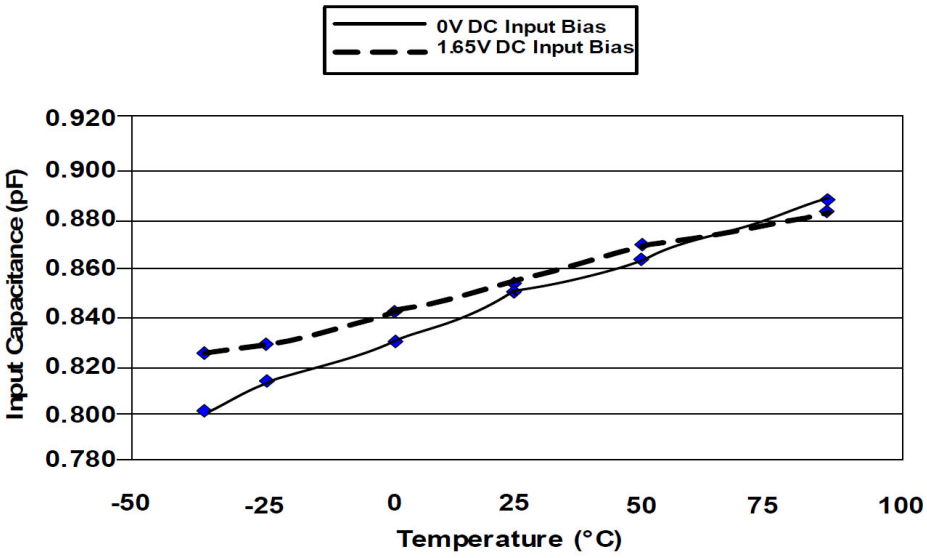

Figure 2. Typical Variation of C_{IN} vs. Temp
(f = 1 MHz, V_{IN} = 30 mV, V_P = 3.3 V, V_N = 0 V, 0.1 μF Chip Capacitor between V_P and V_N)

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PERFORMANCE INFORMATION (CONTINUED)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ω Environment)

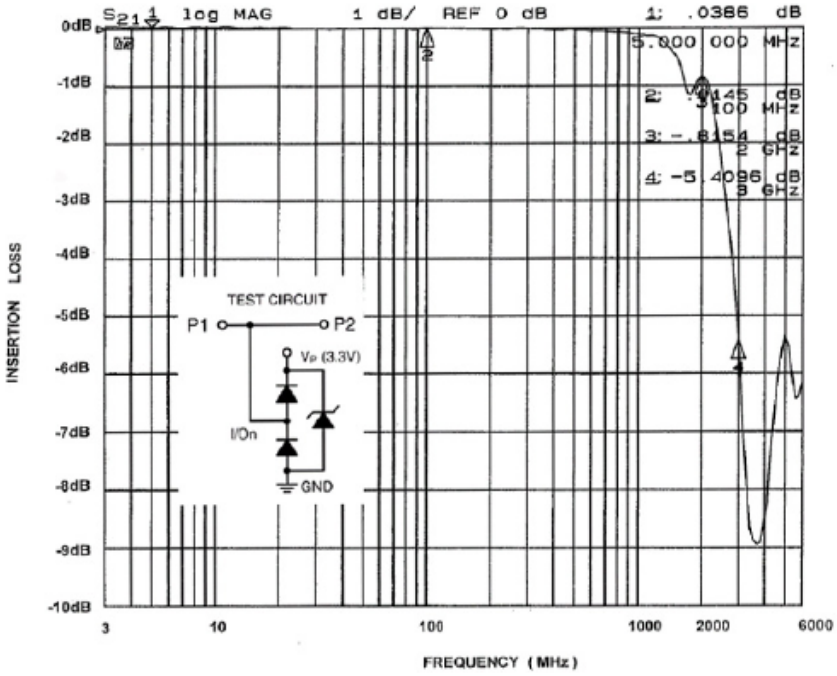

Figure 3. Insertion Loss (S21) vs. Frequency (0 V DC Bias, V_P = 3.3 V)

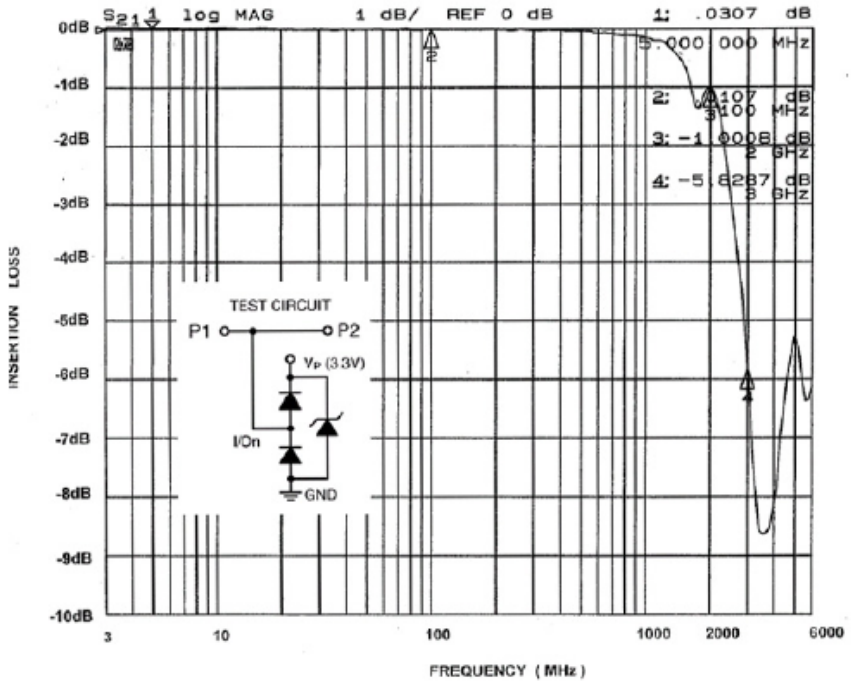

Figure 4. Insertion Loss (S21) vs. Frequency (2.5 V DC Bias, V_P = 3.3 V)

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APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Figure 5, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$\mathbf{V_{CL} = Fwd\ voltage\ drop\ of\ D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt}$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10 nH of series inductance (L_1 and L_2 combined) will lead to a 300 V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1293 has an integrated Zener diode between V_P and V_N. This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22 μF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

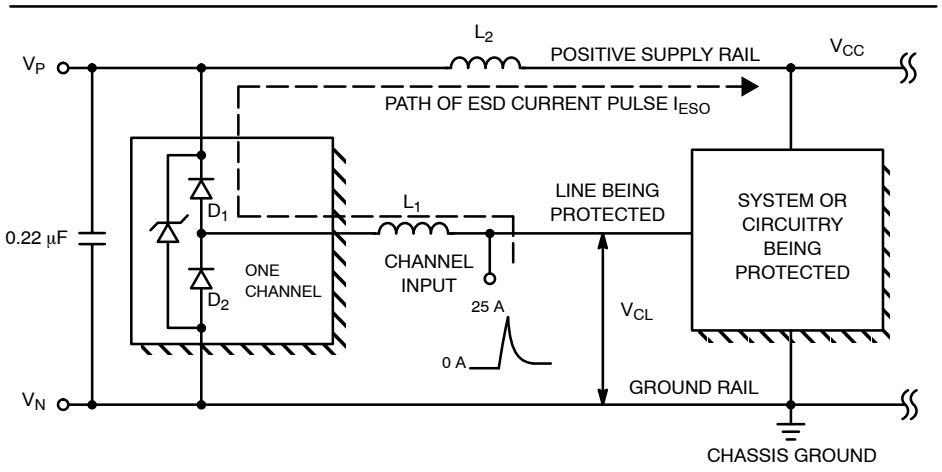

Figure 5. Application of Positive ESD Pulse between Input Channel and Ground

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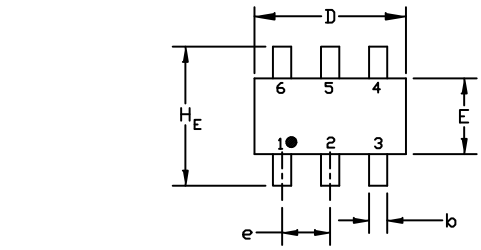
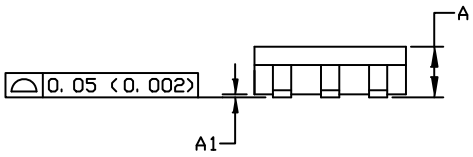
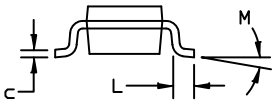


TOP VIEW



SIDE VIEW

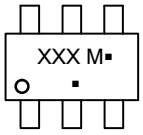


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. CONTROLLING DIMENSION: INCHES
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
H_E	2.50	2.75	3.00	0.099	0.108	0.118
L	0.20	0.40	0.60	0.008	0.016	0.024
M	0°	---	10°	0°	---	10°

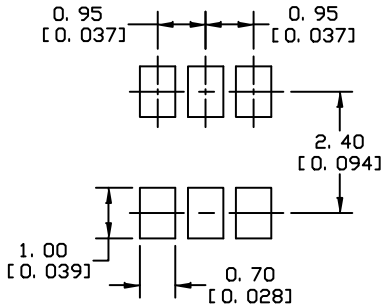
GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1

STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 10:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 11:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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