CM1240

Dual-Voltage ESD Protection Array for USB Ports

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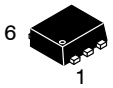
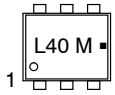


SOT−563
SE SUFFIX
CASE 463A

MARKING DIAGRAM



L40 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
CM1240−F4SE	SOT−563 (Pb−Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

The CM1240 is a 4−channel ESD protection array. Three channels of the CM1240 are low voltage (LV) diodes, which have a capacitance of 7 pF enabling them to protect high speed I/O ports while providing robust ESD protection. The other channel of the CM1240 is a high voltage (HV) diode which has a capacitance of 25 pF enabling it to protect power supply inputs or OLED power rails, etc.

The parts integrate avalanche−type ESD diodes, which provide a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The ESD protection diodes are designed and characterized to safely dissipate ESD strikes of ±8 kV, the maximum requirement of the IEC61000−4−2 international standard. Using the MIL−STD−883 (Method 3015) specification for Human Body Model (HBM) ESD, the pins are protected for contact discharges of greater than ±16 kV.

This device is particularly well suited for portable electronics (e.g. wireless handsets, PDAs, notebook computers) because of its small package format and easy−to−use pin assignments. In particular, the CM1240 is ideal for protecting USB or mini−USB ports operating at full speed (12 Mbps).

Features

- Four Channels of ESD Protection
- ±8 kV ESD Protection (IEC61000−4−2, Contact Discharge)
- ±16 kV ESD Protection (HBM)
- SOT−563 Space−saving Package
- 16 V Clamp on V_{CC}
- These Devices are Pb−Free and are RoHS Compliant

Applications

- USB and Mini−USB Applications
- I/O Port Protection for Mobile Handsets
- Wireless Handsets

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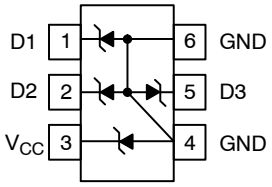
Table 1. PIN DESCRIPTIONS

6−pin SOT−563 Package		
Pin	**Name**	**Description**
1	D1	Cathode Connection for Low Voltage ESD Diode
2	D2	Cathode Connection for Low Voltage ESD Diode
5	D3	Cathode Connection for Low Voltage ESD Diode
3	V_{CC}	Cathode Connection for High Voltage ESD Diode
−	NC	No Connect
−	NC	No Connect
−	NC	No Connect
−	NC	No Connect
4	GND	Anode−side Connection for All ESD Diodes
6	GND	Anode−side Connection for All ESD Diodes

PACKAGE / PINOUT DIAGRAMS



SOT−563

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
ESD Protection (HBM)	16	kV
Pin Voltages V_{CC} to GND All Other Pins to GND	 [GND − 0.3] to +13 [GND − 0.3] to +5.5	V
Storage Temperature Range	−65 to +150	°C
Lead Temperature (soldering, 10 sec)	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

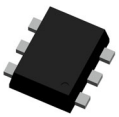
Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{LV}	LV Diode Capacitance at 3 Vdc; 1 MHz, 30 mVac			6		pF
C_{HV}	HV Diode Capacitance at 3 Vdc; 1 MHz, 30 mVac			25		pF
I_{LV}	LV Diode Leakage at +3.3 V reverse bias voltage			0.01	0.4	μA
I_{HV}	HV Diode Leakage at +11 V reverse bias voltage			0.01	0.4	μA
$V_{CL(LV)}$	LV Diode Signal Clamp Voltage: Positive Clamp, 10 mA Negative Clamp, −10 mA		 5.6 −1.5	 6.8 −0.8	 9 −0.4	V
$V_{CL(HV)}$	HV Diode Signal Clamp Voltage: Positive Clamp, 10 mA Negative Clamp, −10 mA		 13 −1.5	 16 −0.8	 19 −0.4	V
V_{ESD}	In−system ESD withstand voltage: Human Body Model (MIL−STD−883, method 3015) IEC 61000−4−2, contact discharge method	(Note 2)	 ±25 ±12			kV
$R_{DYN(LV)}$	LV Diode Dynamic Resistance: Positive Negative			 2.8 1.2		Ω
$R_{DYN(HV)}$	HV Diode Dynamic Resistance: Positive Negative			 1.0 0.7		Ω

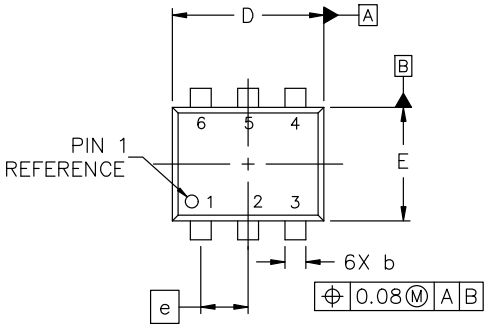
1. Guaranteed at 25°C only
2. ESD applied to input/output pins with respect to GND, one at a time. These parameters are guaranteed by design.



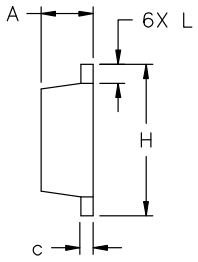
SOT−563−6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

DATE 15 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

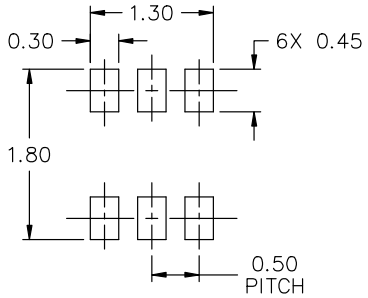


TOP VIEW



SIDE VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

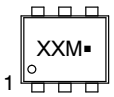
STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Month Code
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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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