CM1225

4-Channel Low Capacitance ESD Protection Arrays

ON Semiconductor®

http://onsemi.com

uUDFN−10
DE SUFFIX
CASE 517BB

Product Description

The CM1225 diode array has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. This device is ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to the ground pins (V_N). A Zener diode is embedded between the positive terminal of the diode pair to the ground. This eliminates the need for an external bypass capacitor to absorb positive ESD strikes to ground. The CM1225 protects against ESD pulses up to ±8 kV per the IEC 61000−4−2 standard.

The CM1225 is particularly well−suited for protecting systems using high−speed ports such as HDMI, DVI, display, MDDI, USB 2.0, Serial ATA, IEEE1394 (FireWire and i.LINK), corresponding ports in removable storage, digital camcorders, DVD−RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

The CM1225 is available in a RoHS−compliant, uUDFN 10−pin package.

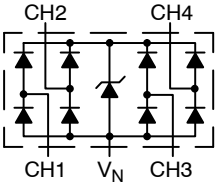
Features

- Four Channels of ESD Protection
- Provides ESD Protection to IEC61000−4−2 Level 4 ±8 kV Contact Discharge
- Low Channel Input Capacitance of 0.8 pF (Typically)
- Channel Input Capacitance Matching (I/O to I/O) of 0.02 pF (Typically) is Ideal for Differential Signals
- Minimal Capacitance Change for Temperature and Voltage
- Zener Diode Eliminates the Need for External By−pass Capacitors
- Each I/O Pin Can Withstand Over 1000 ESD Strikes*
- These Devices are Pb−Free and are RoHS Compliant

Applications

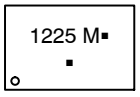
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Display and MDDI Ports
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- USB2.0 Ports at 480 Mbps in desktop PCs, Notebooks and Peripherals
- IEEE1394 FireWire Ports at 400 Mbps / 800 Mbps
- General Purpose High−speed Data Line ESD Protection
- Protection of Interface Ports or IC Pins which are Exposed to High ESD Levels

BLOCK DIAGRAM



CM1225−04DE

MARKING DIAGRAM



1225 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
CM1225−04DE	uUDFN−10 (Pb−Free)	3000/Tape & Reel

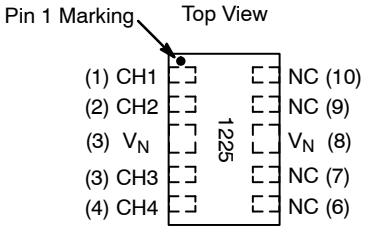
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*Standard test condition is IEC61000−4−2 level 4 test circuit with each pin subjected to ±8kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

Table 1. PIN DESCRIPTIONS

4−Channel, 10−Lead uUDFN−10 Package			
Pin	**Name**	**Type**	**Description**
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	V_N	GND	Ground
4	CH3	I/O	ESD Channel
5	CH4	I/O	ESD Channel
6	NC		No Connect
7	NC		No Connect
8	V_N	GND	Ground
9	NC		No Connect
10	NC		No Connect

PACKAGE / PINOUT DIAGRAMS



10−Lead uUDFN

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
DC Voltage at any Channel Input	− 0.5 to + 5.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 10 mA; T_A = 25°C; Note 2	 0.65 −1.20	 0.85 −0.85	 1.20 −0.65	V
I_{LEAK}	Channel Leakage Current	T_A = 25°C; V_{IN} = 3.3 V, V_N = 0 V		±0.1	±1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_N = 0 V, V_{IN} = 1.65 V		0.8	1.0	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, V_N = 0 V, V_{IN} = 1.65 V		0.02		pF
V_{ESD}	ESD Protection − Peak Discharge Voltage at any Channel Input, in system Contact discharge per IEC 61000−4−2 standard	 T_A = 25°C; (Notes 2 and 3)	 ±8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1 A, t_P = 8/20 μS; (Note 3)		 +10 −4.5		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1 A, t_P = 8/20 μS Any I/O pin to Ground; (Note 3)		 1.3 1.3		Ω

1. All parameters specified at T_A = −40°C to +85°C unless otherwise noted.
2. Standard IEC 61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω, V_P = 3.3 V, V_N grounded.
3. These measurements performed with no external capacitor.

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

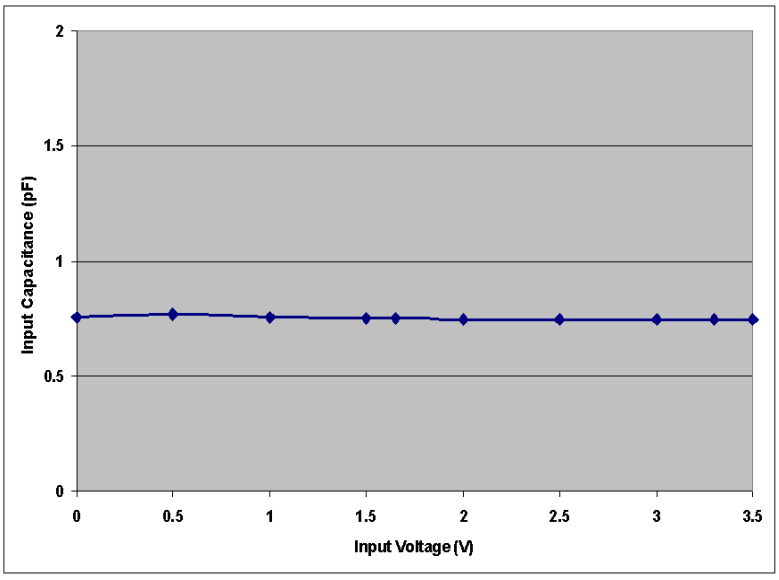


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
(f = 1 Mhz, V_N = 0 V, T = 25°C)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

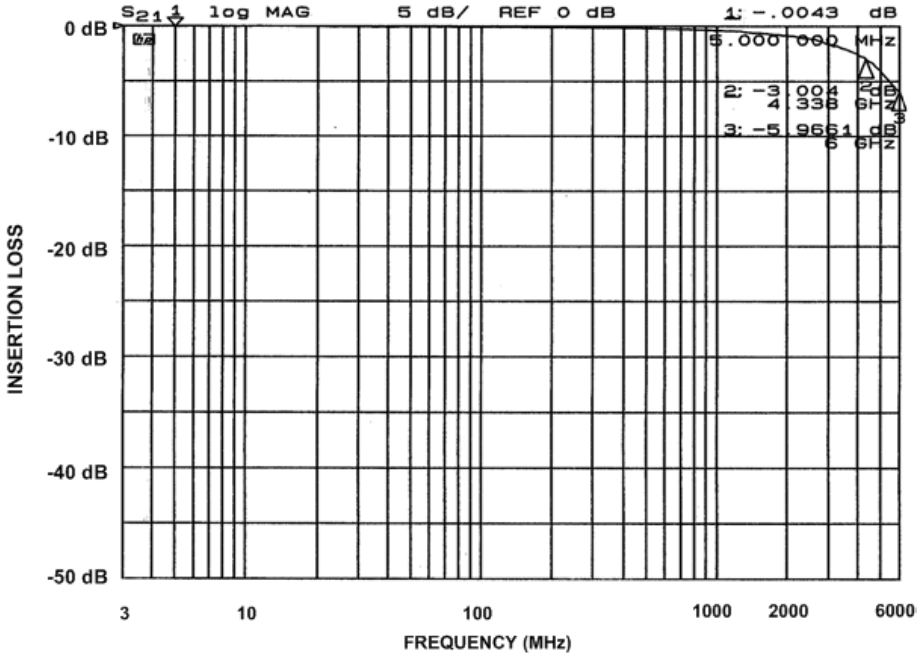


Figure 2. Insertion Loss (S21) vs. Frequency (0 V DC Bias)

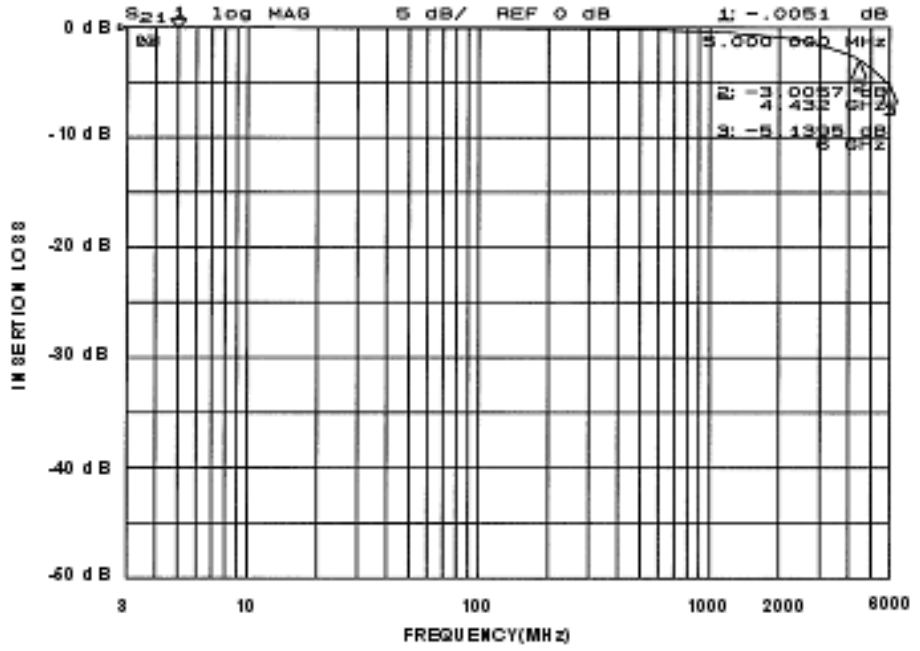


Figure 3. Insertion Loss (S21) vs. Frequency (2.5 V DC Bias)

APPLICATION INFORMATION

Design Considerations

As a general rule, the CM1225 ESD protection array should be located as close as possible to the point of entry of expected electrostatic discharges. Use minimum PCB trace lengths to ground planes and between the signal input and the ESD devices.

Additional Information

See also ON Semiconductor Application Note “Design Considerations for ESD Protection”.

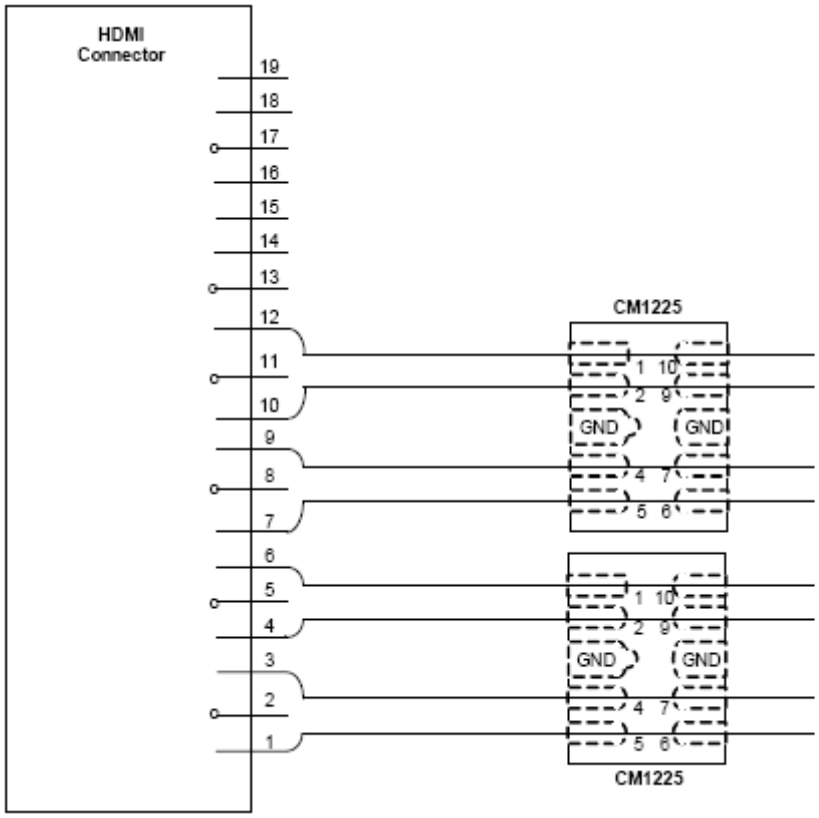


Figure 4. Typical HDMI ESD Protection with CM1225 Connection

APPLICATION INFORMATION (Cont'd)

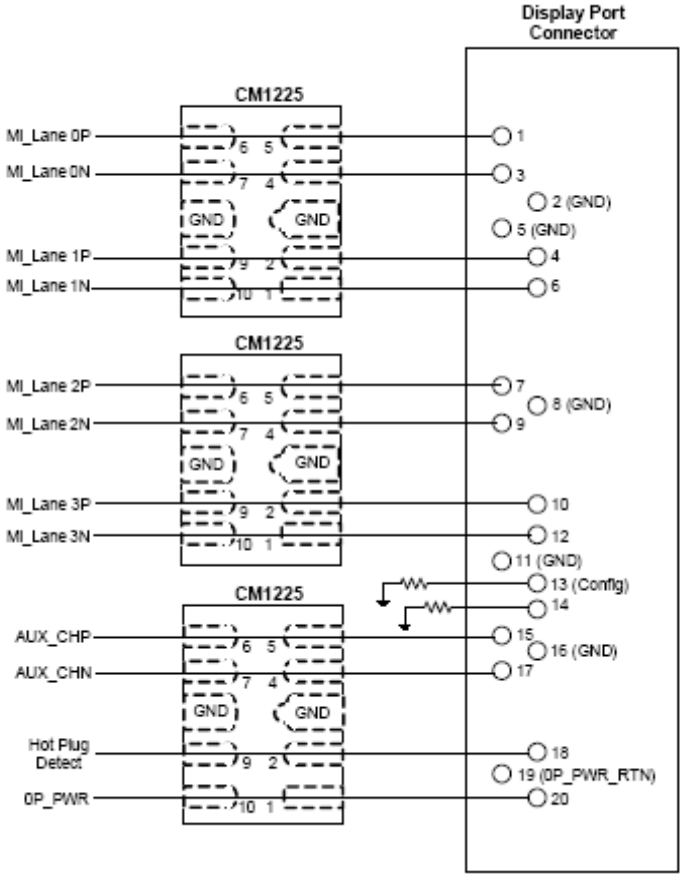


Figure 5. Display Port ESD Protection with CM1225 Connection

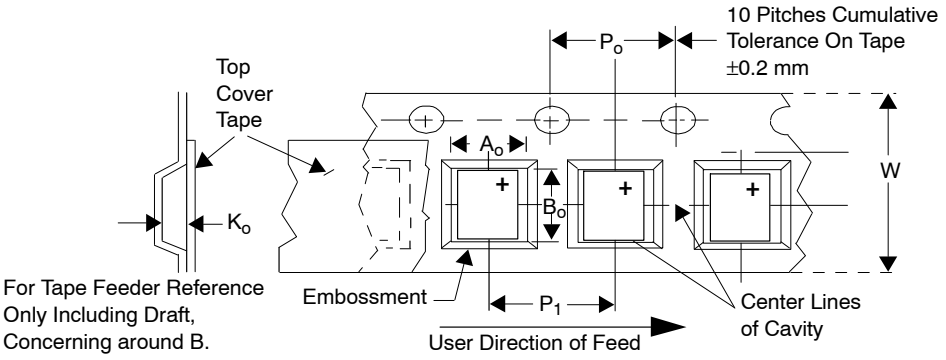
MECHANICAL DETAILS

uUDFN−10 Mechanical Specifications, 0.5 mm

The 10−lead, 0.5 mm pitch uUDFN package dimensions are presented below.

Table 5. TAPE AND REEL SPECIFICATIONS

Part Number	Chip Size (mm)	Pocket Size (mm) B_0 X A_0 X K_0	Tape Width W	Reel Diameter	Qty per Reel	P_0	P_1
CM1225	2.50 X 1.00 X 0.50	2.80 X 1.45 X 0.70	8 mm	178 mm (7”)	3000	4 mm	4 mm



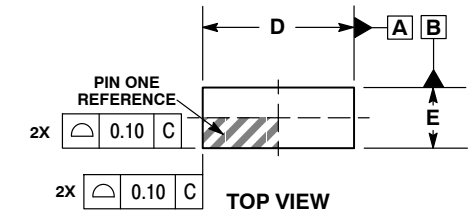
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

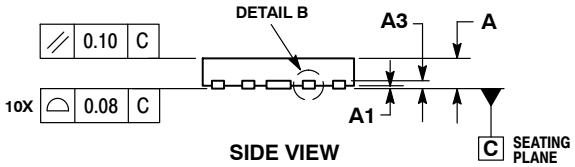
UDFN10 2.5x1, 0.5P
CASE 517BB−01
ISSUE O

DATE 17 NOV 2009

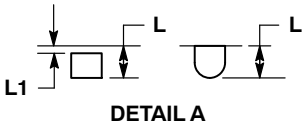
SCALE 4:1



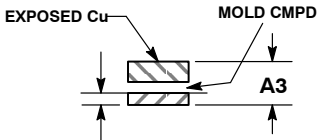
TOP VIEW



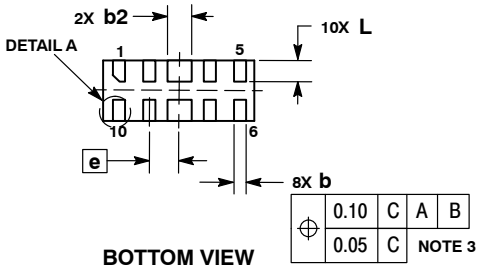
SIDE VIEW



DETAIL A
OPTIONAL CONSTRUCTIONS



DETAIL B
OPTIONAL CONSTRUCTION

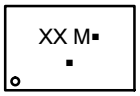


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
b2	0.35	0.45
D	2.50 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.05

GENERIC MARKING DIAGRAM*

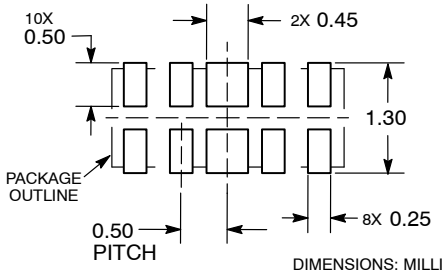


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**UDFN10 2.5X1, 0.5P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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