CM1225

4-Channel Low Capacitance ESD Protection Arrays

Product Description
The CM1225 diode array has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. This device is ideal for protecting systems with high data and clock rates or for systems requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to the ground pins (VN). A Zener diode is embedded between the positive terminal of the diode pair to the ground. This eliminates the need for an external bypass capacitor to absorb positive ESD strikes to ground. The CM1225 protects against ESD pulses up to ±8 kV per the IEC 61000−4−2 standard.

The CM1225 is particularly well−suited for protecting systems using high−speed ports such as HDMI, DVI, display, MDDI, USB 2.0, Serial ATA, IEEE1394 (FireWire and i.LINK), corresponding ports in removable storage, digital camcorders, DVD−RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

The CM1225 is available in a RoHS−compliant, uUDFN 10−pin package.

Features
• Four Channels of ESD Protection
• Provides ESD Protection to IEC61000−4−2 Level 4 ±8 kV Contact Discharge
• Low Channel Input Capacitance of 0.8 pF (Typically)
• Channel Input Capacitance Matching (I/O to I/O) of 0.02 pF (Typically) is Ideal for Differential Signals
• Minimal Capacitance Change for Temperature and Voltage
• Zener Diode Eliminates the Need for External By−pass Capacitors
• Each I/O Pin Can Withstand Over 1000 ESD Strikes*
• These Devices are Pb−Free and are RoHS Compliant

Applications
• DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
• Display and MDDI Ports
• Serial ATA Ports in Desktop PCs and Hard Disk Drives
• PCI Express Ports
• USB2.0 Ports at 480 Mbps in desktop PCs, Notebooks and Peripherals
• IEEE1394 FireWire Ports at 400 Mbps / 800 Mbps
• General Purpose High−speed Data Line ESD Protection
• Protection of Interface Ports or IC Pins which are Exposed to High ESD Levels

*Standard test condition is IEC61000−4−2 level 4 test circuit with each pin subjected to ±8kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

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Publication Order Number: CM1225/D
Table 1. PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CH1</td>
<td>I/O</td>
<td>ESD Channel</td>
</tr>
<tr>
<td>2</td>
<td>CH2</td>
<td>I/O</td>
<td>ESD Channel</td>
</tr>
<tr>
<td>3</td>
<td>VN</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>4</td>
<td>CH3</td>
<td>I/O</td>
<td>ESD Channel</td>
</tr>
<tr>
<td>5</td>
<td>CH4</td>
<td>I/O</td>
<td>ESD Channel</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td></td>
<td>No Connect</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td></td>
<td>No Connect</td>
</tr>
<tr>
<td>8</td>
<td>VN</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td></td>
<td>No Connect</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td></td>
<td>No Connect</td>
</tr>
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</table>

Table 2. ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature Range</td>
<td>–40 to +85°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>–65 to +150°C</td>
<td></td>
</tr>
<tr>
<td>DC Voltage at any Channel Input</td>
<td>–0.5 to +5.5 V</td>
<td></td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature Range</td>
<td>–40 to +85°C</td>
<td></td>
</tr>
</tbody>
</table>

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note1)

Symbol | Parameter | Conditions | Min | Typ | Max | Units |
--------|-----------|------------|-----|-----|-----|-------|
VF      | Diode Forward Voltage Top Diode Bottom Diode | If = 10 mA; TA = 25°C; Note 2 | 0.65 | 0.85 | 1.20 | V |
|        |          |            | –1.20 | –0.85 | –0.65 | |
ILEAK   | Channel Leakage Current | TA = 25°C; VN = 3.3 V; VN = 0 V | ±0.1 | ±1.0 | μA |
CIN     | Channel Input Capacitance | At 1 MHz, VN = 0 V, VIIN = 1.65 V | 0.8 | 1.0 | pF |
ΔCIN    | Channel Input Capacitance Matching | At 1 MHz, VN = 0 V, VIIN = 1.65 V | 0.02 | | pF |
VESD    | ESD Protection – Peak Discharge Voltage at any Channel Input, in system Contact discharge per IEC 61000–4–2 standard | TA = 25°C; (Notes 2 and 3) | ±8 | | kV |
VCL     | Channel Clamp Voltage Positive Transients Negative Transients | TA = 25°C, IPP = 1 A, | ±10 | –4.5 | |
|        |          | tP = 8/20 μS; (Note 3) | | | |
Rdyn    | Dynamic Resistance Positive Transients Negative Transients | IPP = 1 A, IP = 8/20 μS; Any I/O pin to Ground; (Note 3) | 1.3 | 1.3 | Ω |

1. All parameters specified at TA = –40°C to +85°C unless otherwise noted.
3. These measurements performed with no external capacitor.

http://onsemi.com
Input Channel Capacitance Performance Curves

Figure 1. Typical Variation of $C_{IN}$ vs. $V_{IN}$
(f = 1 Mhz, $V_N = 0$ V, $T = 25^\circ$C)
Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

Figure 2. Insertion Loss (S21) vs. Frequency (0 V DC Bias)

Figure 3. Insertion Loss (S21) vs. Frequency (2.5 V DC Bias)
Design Considerations
As a general rule, the CM1225 ESD protection array should be located as close as possible to the point of entry of expected electrostatic discharges. Use minimum PCB trace lengths to ground planes and between the signal input and the ESD devices.

Additional Information
See also ON Semiconductor Application Note “Design Considerations for ESD Protection”.

Figure 4. Typical HDMI ESD Protection with CM1225 Connection
Figure 5. Display Port ESD Protection with CM1225 Connection
uUDFN−10 Mechanical Specifications, 0.5 mm
The 10−lead, 0.5 mm pitch uUDFN package dimensions are presented below.

**Table 5. TAPE AND REEL SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Chip Size (mm)</th>
<th>Pocket Size (mm)</th>
<th>Tape Width (mm)</th>
<th>Reel Diameter</th>
<th>Qty per Reel</th>
<th>P₀</th>
<th>P₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM1225</td>
<td>2.50 X 1.00 X 0.50</td>
<td>2.80 X 1.45 X 0.70</td>
<td>8</td>
<td>178 mm (7&quot;)</td>
<td>3000</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

For Tape Feeder Reference
Only Including Draft,
Concerning around B.

Embossment
User Direction of Feed

10 Pitches Cumulative Tolerance On Tape
±0.2 mm
UDFN10 2.5x1, 0.5P
CASE 517BB–01
ISSUE O

DATE 17 NOV 2009

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.