CM1214A

1 and 2-Channel AC Signal ESD Protector

ON Semiconductor®

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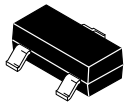
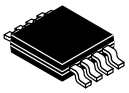


SOT23−3
SO SUFFIX
CASE 318



MSOP−8
MR SUFFIX
CASE 846AD

Product Description

The CM1214A ESD protector is used to protect bipolar signal lines against electrostatic discharge (ESD). The CM1214A allows operation in high−speed environments with signals levels up to ±5 V.

The CM1214A comes in two versions:

- The CM1214A−01SO is a single channel ESD protector and is available in a 3−lead SOT23−3 package.
- The CM1214A−02MR is a dual channel ESD protector and is available in an 8−lead MSOP−8 package.

The low sub−1 pF loading capacitance makes the CM1214A−01SO ideal for protecting high−speed interfaces including RF switches and amplifiers.

The CM1214A−02MR is ideal for dual high−speed signal pairs used in Gigabit Ethernet, ADSL, etc. The CM1214A−02MR can also be used for higher transmit voltage applications by connecting the two channels in series.

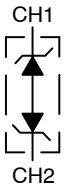
Features

- Single Channel ESD Protection for an AC Signal Up To ±5 V for 0.25 W Transmit Power
- Connects Two Channels in Series for Signals Up To ±10 V (1 W transmit power)
- ±8 kV ESD Protection Per IEC 61000−4−2 Contact Discharge
- Sub−1pF Loading Capacitance
- Minimal Variation with Voltage and Temperature
- Each I/O Pin Can Withstand Over 1000 ESD Strikes*
- SOT23−3 and MSOP−8 Packages
- These Devices are Pb−Free and are RoHS Compliant

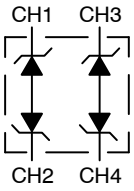
Applications

- RF Switch and Amplifier Protection
- RF Modules and RF IC Protection
- Wireless Handsets and WLAN
- High−Speed AC Signals for Gbit Ethernet, etc.

BLOCK DIAGRAM

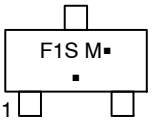


CM1214A−01SO

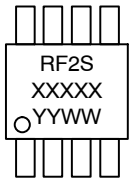


CM1214A−02MR

MARKING DIAGRAMS



M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)



XXXXX = Last 5 Digits of Lot#
YYWW = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
CM1214A−01SO	SOT23 (Pb−Free)	3000/Tape & Reel
CM1214A−02MR	MSOP (Pb−Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

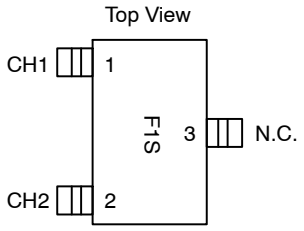
*Standard test condition is IEC61000−4−2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

Table 1. PIN DESCRIPTIONS

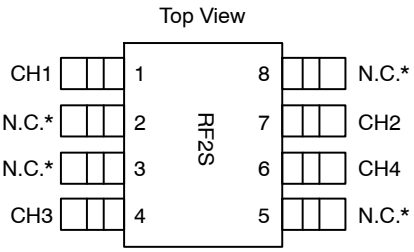
SOT23−3 Package		
Pin	**Name**	**Description**
1	CH1	ESD Channel
2	CH2	ESD Channel
3	N.C.	No connect

MSOP−8 Package		
Pin	**Name**	**Description**
1	CH1	ESD Channel
2	N.C.	No connect
3	N.C.	No connect
4	CH3	ESD Channel
5	N.C.	No connect
6	CH4	ESD Channel
7	CH2	ESD Channel
8	N.C.	No connect

PACKAGE / PINOUT DIAGRAMS



SOT23−3



MSOP−8

* All N.C. pins must be left floating (i.e., not connected to the PCB). See applications section for more information.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
DC Voltage between CH pins	7	V
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C
Package Power Rating SOT23−3 Package (CM1214A−01SO) MSOP8 Package (CM1214A−02MR)	 225 400	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ST}	Standoff Voltage	I = 10 μA		±7		V
V_{ESD}	ESD Voltage Protection Peak discharge voltage between CH pins a) Contact discharge per IEC 61000−4−2 standard	(Notes 2 and 3)	±8			kV
I_{LEAK}	Channel Leakage Current	T_A = 25°C, 5.5 V between CH pins		±0.1	±1.0	μA
R_{DYN}	Dynamic Resistance	T_A = 25°C, I_{PP} = 1 A, t_P = 8/20 μS Any I/O pin to Ground (Note 4)		1.36		Ω

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CL}	Channel Clamp Voltage	T_A = 25°C, I_{PP} = 1 A, t_P = 8/20 μS (Note 4)		11.3		V
C_{IN}	Channel Input Capacitance Voltage between CH pins = 0 V Voltage between CH pins = 5 V	Measured at 1 MHz between CH pins	 0.4 0.35	 0.6 0.54	 0.9 0.8	pF

1. All parameters specified at T_A = −40°C to +85°C unless otherwise noted.
2. Standard IEC 61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω.
3. From CH pin with other CH pin grounded.
4. No Connect pins are left open for all tests.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PERFORMANCE INFORMATION

Typical Capacitance Characteristics vs. Voltage

CM1214A illustrates how the loading capacitance remains mainly flat across the voltage range form 0 V to 5 V, the voltage between CH pins.

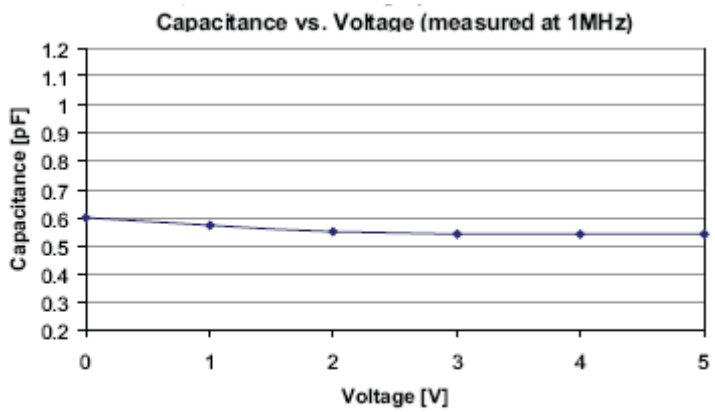


Figure 1. CM1214A Capacitance vs. Voltage

Typical Voltage Current (VI) Characteristics (low current)

CM1214A shows how the CM1214A experiences a symmetrical I/V curve, without any snapback or trigger voltage. It gradually starts tu turn on at about 6 V and clamps above 7 V.

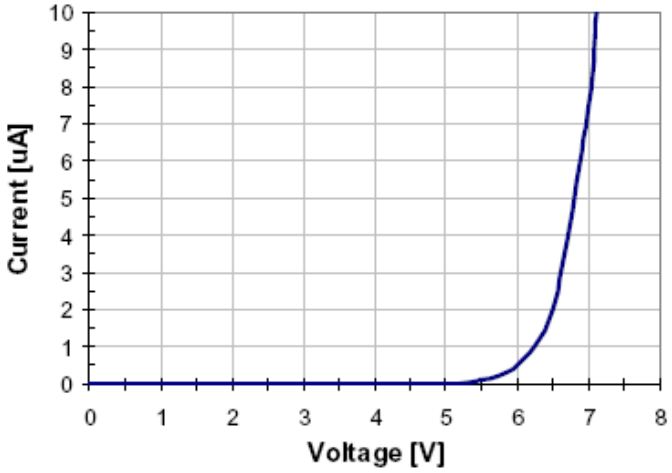


Figure 2. CM1214A VI Characteristics, Low Current

PERFORMANCE INFORMATION (Cont'd)

Typical Voltage−Current (VI) Characteristics (high current, pulse condition)

CM1214A shows how the CM1214A experiences a symmetrical I/V curve, without any snapback or trigger voltage. The curve shows only one polarity.

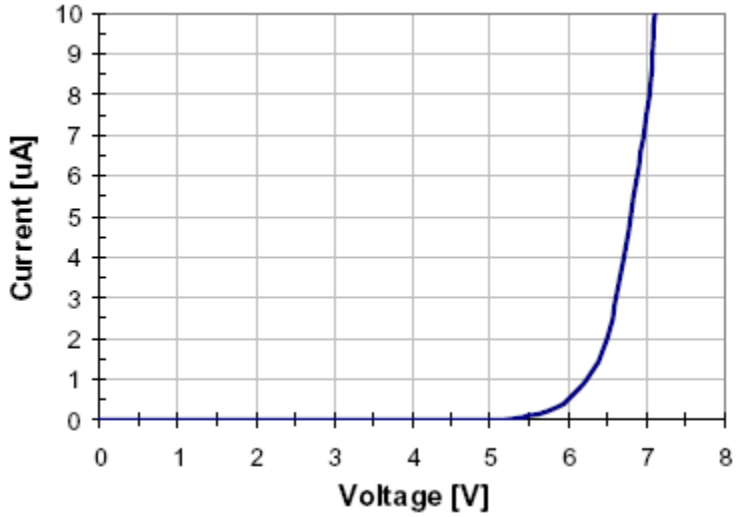


Figure 3. CM1214A VI Characteristics, High Current, Pulse (clamping) Condition

Typical Capacitance Characteristics vs. Temperature

CM1214A illustrates the loading capacitance for both 0 VDC and 1.65 VDC input across the −40 to 85°C temperature range.

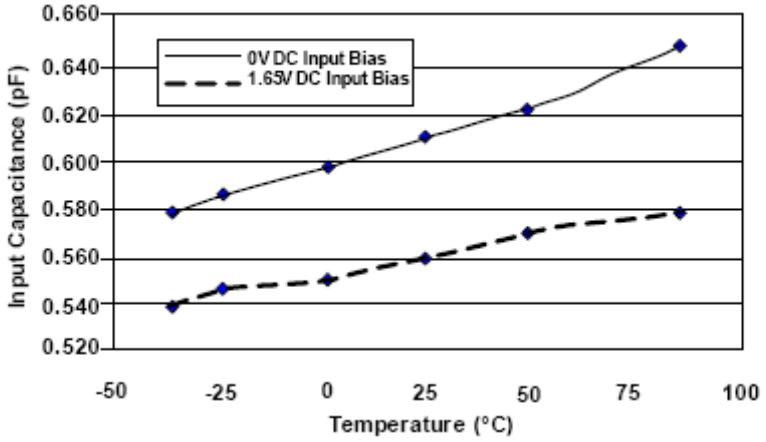


Figure 4. CM1214A Capacitance vs. Temperature

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

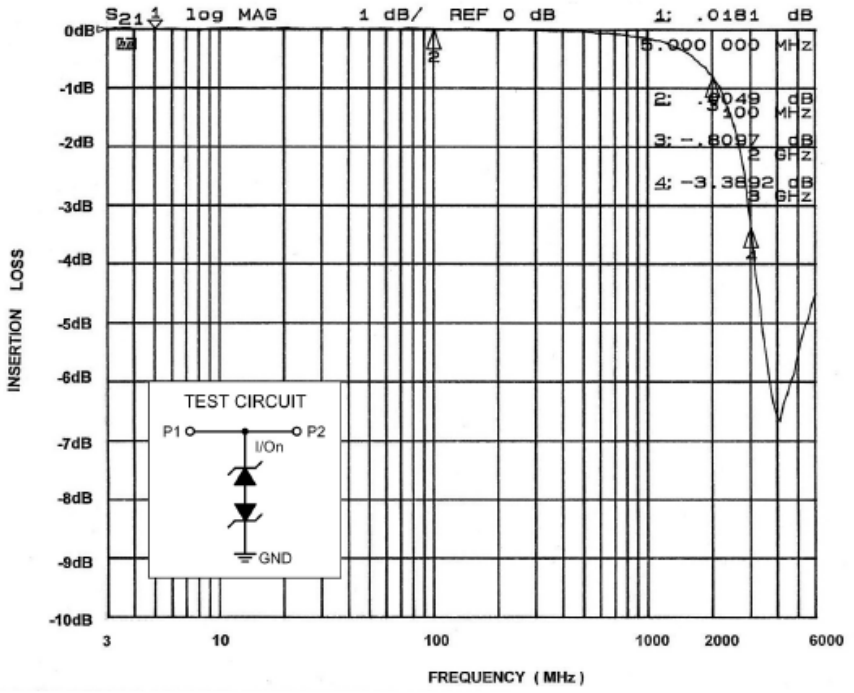


Figure 5. Insertion Loss vs. Frequency (0 V DC Bias)

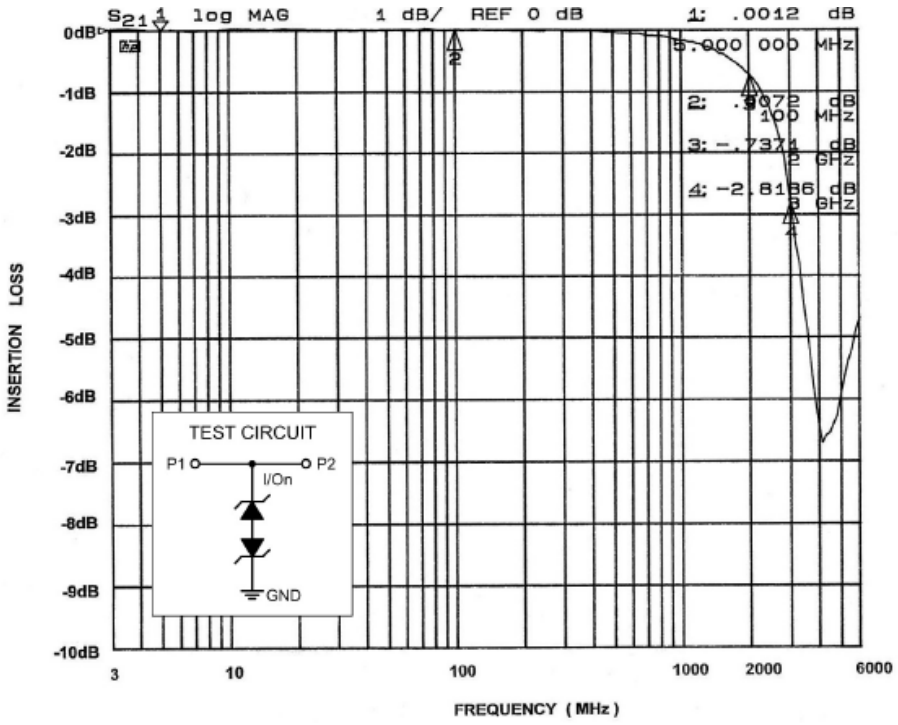


Figure 6. Insertion Loss vs. Frequency (2.5 V DC Bias)

APPLICATION INFORMATION

CM1214A−01SO

The CM1214A−01SO protects a single bipolar signal line often found in RF circuits. One I/O pin (pin 1 for example) is connected to the signal line for protection, and the other I/O pin is tied to GND. It is important to have a solid ground connection to reduce the clamping voltage. *Pin 3 of the 3−lead SOT23 must be left open (and not connected on the PCB)*.

CM1214A−02MR

The CM1214A−02MR protects two bipolar lines, such as for Gbit Ethernet. The PCB traces underneath the package connect across to the corresponding pins (Pins 1, 4, 6 and 7). *Pins 2, 3, 5 and 8 of the MSOP−8 package must be left open (and not connected on the PCB)*.

Any disturbance on the line above or below the standoff voltage is clamped.

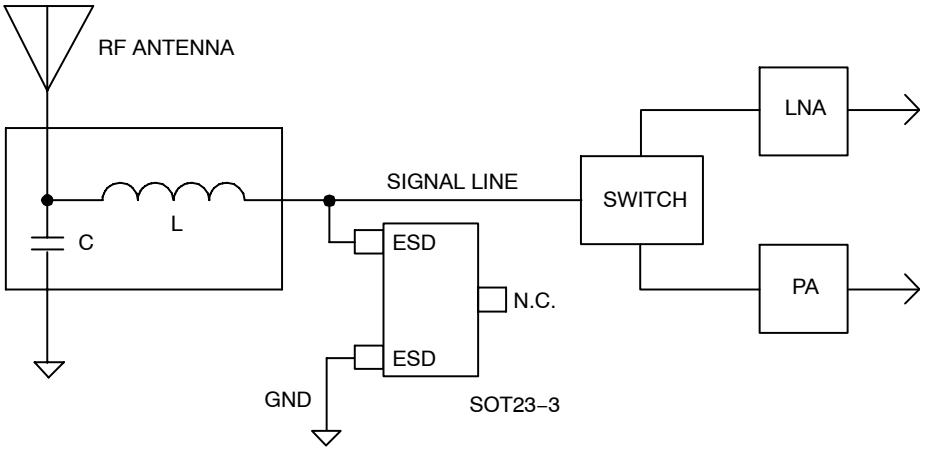


Figure 7. Typical Application − RF Switch and Amplifier Protection, CM1214A−01SO in 3−lead SOT23

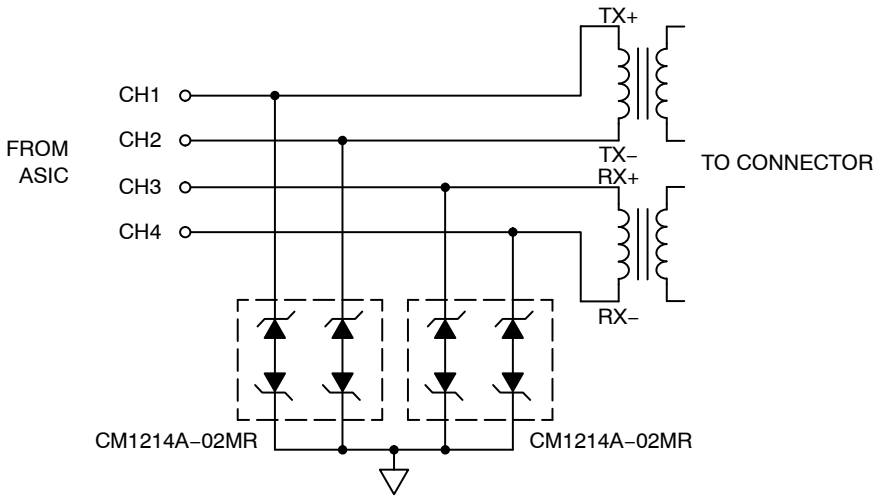
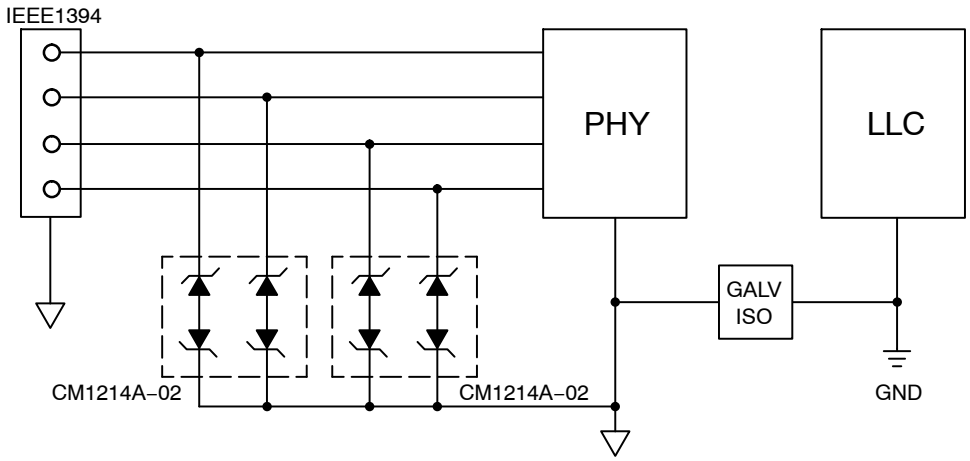


Figure 8. Typical Application − Ethernet Protection, CM1214A−02MR in 8−lead MSOP

APPLICATION INFORMATION (Cont'd)

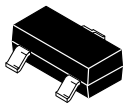


Keep the ESD devices on the PHY side of the galvanic isolation and inside the V_{CC} domain of the PHY controller

Figure 9. Typical Application − IEEE1394 Protection, CM1214A−02MR in 8−lead MSOP

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

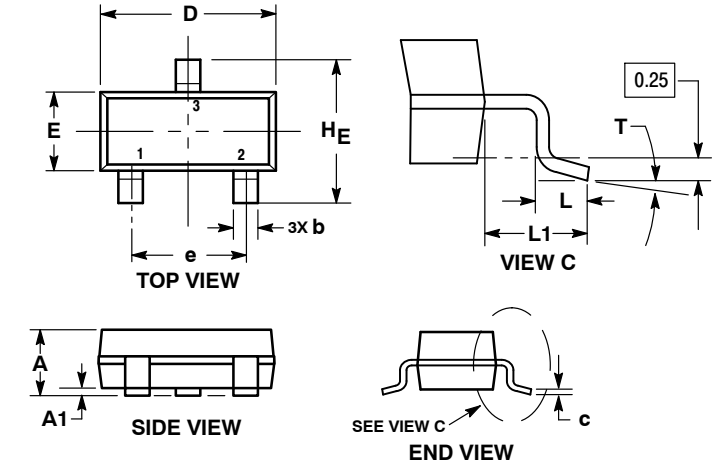
ON Semiconductor®



SOT−23 (TO−236)
CASE 318−08
ISSUE AS

DATE 30 JAN 2018

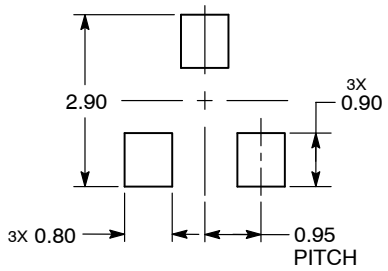
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

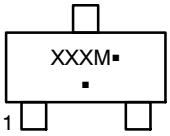
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	−−−	10°	0°	−−−	10°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

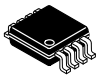
STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

DOCUMENT NUMBER:	98ASB42226B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOT−23 (TO−236)	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

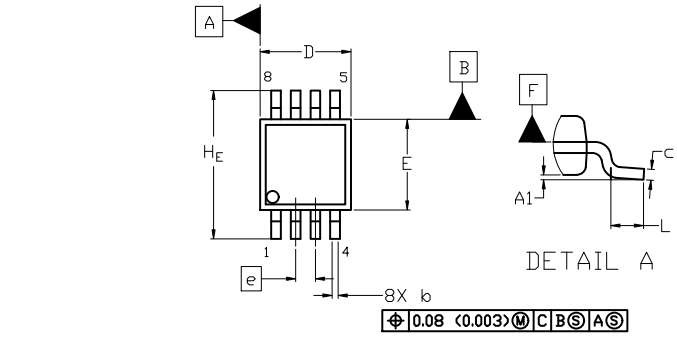
ON Semiconductor®

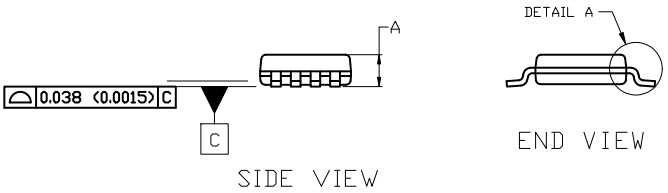


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

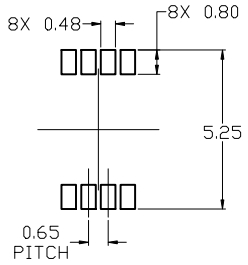
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

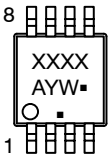


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

DOCUMENT NUMBER:	**98ASB14087C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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