

# EEPROM Serial 1-Kb Microwire - Automotive Grade 1

## CAV93C46



**TSSOP-8**  
**Y SUFFIX**  
**CASE 948AL**



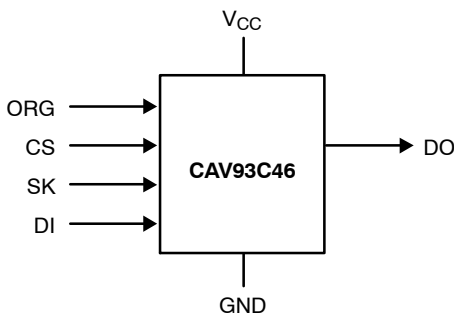
**SOIC-8**  
**V SUFFIX**  
**CASE 751BD**

### Description

The CAV93C46 is an EEPROM Serial 1-Kb Microwire Automotive Grade 1 device, which is configured as either 64 registers of 16 bits (ORG pin at  $V_{CC}$ ) or 128 registers of 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAV93C46 features a self-timed internal write with auto-clear. On-chip Power-On Reset circuit protects the internal logic against powering up in the wrong state.

### Features

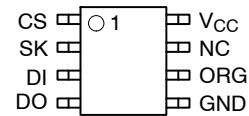
- Automotive AEC-Q100 Grade 1 ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) Qualified
- High Speed Operation: 2 MHz
- 2.5 V to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read
- Software Write Protection
- Power-up Inadvertant Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-pin SOIC and TSSOP Packages
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant†



**Figure 1. Functional Symbol**

†For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### PIN CONFIGURATIONS



SOIC (V), TSSOP (Y)  
(Top View)

### PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
$V_{CC}$	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

Note: When the ORG pin is connected to  $V_{CC}$ , the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameter	Value	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	-0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than -0.5 V or higher than  $V_{CC} + 0.5$  V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than  $V_{CC} + 1.5$  V, for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS** (Note 2)

Symbol	Parameter	Min	Units
$N_{END}$ (Note 3)	Endurance	1,000,000	Program / Erase Cycles
$T_{DR}$	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Block Mode,  $V_{CC} = 5$  V, 25°C

**Table 3. D.C. OPERATING CHARACTERISTICS**

( $V_{CC} = +2.5$  V to +5.5 V,  $T_A = -40^\circ\text{C}$  to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
$I_{CC1}$	Supply Current (Write)	Write, $V_{CC} = 5.0$ V		1	mA
$I_{CC2}$	Supply Current (Read)	Read, DO open, $f_{SK} = 2$ MHz, $V_{CC} = 5.0$ V		500	μA
$I_{SB1}$	Standby Current (x8 Mode)	$V_{IN} = \text{GND or } V_{CC}$ $CS = \text{GND, ORG} = \text{GND}$		5	μA
$I_{SB2}$	Standby Current (x16 Mode)	$V_{IN} = \text{GND or } V_{CC}$ $CS = \text{GND, ORG} = \text{Float or } V_{CC}$		3	μA
$I_{LI}$	Input Leakage Current	$V_{IN} = \text{GND to } V_{CC}$		2	μA
$I_{LO}$	Output Leakage Current	$V_{OUT} = \text{GND to } V_{CC}$ $CS = \text{GND}$		2	μA
$V_{IL1}$	Input Low Voltage	$4.5 \text{ V} \leq V_{CC} < 5.5 \text{ V}$	-0.1	0.8	V
$V_{IH1}$	Input High Voltage	$4.5 \text{ V} \leq V_{CC} < 5.5 \text{ V}$	2	$V_{CC} + 1$	V
$V_{IL2}$	Input Low Voltage	$2.5 \text{ V} \leq V_{CC} < 4.5 \text{ V}$	0	$V_{CC} \times 0.2$	V
$V_{IH2}$	Input High Voltage	$2.5 \text{ V} \leq V_{CC} < 4.5 \text{ V}$	$V_{CC} \times 0.7$	$V_{CC} + 1$	V
$V_{OL1}$	Output Low Voltage	$4.5 \text{ V} \leq V_{CC} < 5.5 \text{ V}$ , $I_{OL} = 3$ mA		0.4	V
$V_{OH1}$	Output High Voltage	$4.5 \text{ V} \leq V_{CC} < 5.5 \text{ V}$ , $I_{OH} = -400$ μA	2.4		V
$V_{OL2}$	Output Low Voltage	$2.5 \text{ V} \leq V_{CC} < 4.5 \text{ V}$ , $I_{OL} = 1$ mA		0.2	V
$V_{OH2}$	Output High Voltage	$2.5 \text{ V} \leq V_{CC} < 4.5 \text{ V}$ , $I_{OH} = -100$ μA	$V_{CC} - 0.2$		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 4. PIN CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz,  $V_{CC} = 5$  V)

Symbol	Test	Conditions	Min	Typ	Max	Units
$C_{OUT}$ (Note 4)	Output Capacitance (DO)	$V_{OUT} = 0$ V			5	pF
$C_{IN}$ (Note 4)	Input Capacitance (CS, SK, DI, ORG)	$V_{IN} = 0$ V			5	pF

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

**Table 5. A.C. CHARACTERISTICS**(V<sub>CC</sub> = +2.5 V to +5.5 V, T<sub>A</sub> = -40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
t <sub>CSS</sub>	CS Setup Time	50		ns
t <sub>CSH</sub>	CS Hold Time	0		ns
t <sub>DIS</sub>	DI Setup Time	100		ns
t <sub>DIH</sub>	DI Hold Time	100		ns
t <sub>PD1</sub>	Output Delay to 1		0.25	μs
t <sub>PD0</sub>	Output Delay to 0		0.25	μs
t <sub>HZ</sub> (Note 5)	Output Delay to High-Z		100	ns
t <sub>EW</sub>	Program/Erase Pulse Width		5	ms
t <sub>CSSMIN</sub>	Minimum CS Low Time	0.25		μs
t <sub>SKHI</sub>	Minimum SK High Time	0.25		μs
t <sub>SKLOW</sub>	Minimum SK Low Time	0.25		μs
t <sub>SV</sub>	Output Delay to Status Valid		0.25	μs
SK <sub>MAX</sub>	Maximum Clock Frequency	DC	2000	kHz

5. This parameter is tested initially and after a design or process change that affects the parameter.

**Table 6. POWER-UP TIMING** (Notes 6 and 7)

Symbol	Parameter	Max	Units
t <sub>PUR</sub>	Power-up to Read Operation	1	ms
t <sub>PUW</sub>	Power-up to Write Operation	1	ms

6. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

7. t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated.

**Table 7. A.C. TEST CONDITIONS**

Input Rise and Fall Times	≤ 50 ns	
Input Pulse Voltages	0.4 V to 2.4 V	4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V
Timing Reference Voltages	0.8 V, 2.0 V	4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V
Input Pulse Voltages	0.2 V <sub>CC</sub> to 0.7 V <sub>CC</sub>	2.5 V ≤ V <sub>CC</sub> ≤ 4.5 V
Timing Reference Voltages	0.5 V <sub>CC</sub>	2.5 V ≤ V <sub>CC</sub> ≤ 4.5 V
Output Load	Current Source I <sub>OLmax</sub> /I <sub>OHmax</sub> ; C <sub>L</sub> = 100 pF	

## DEVICE OPERATION

The CAV93C46 is a 1024-bit nonvolatile memory intended for use with industry standard microprocessors. The CAV93C46 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 10-bit instructions control the reading, writing and erase operations of the device. The CAV93C46 operates on a single power supply and will generate on chip the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status during a write operation. The serial communication protocol follows the timing shown in Figure 2.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The Ready/Busy flag can be disabled only in Ready state; no change is allowed in Busy state.

The format for all instructions sent to the device is a logical “1” start bit, a 2-bit (or 4-bit) opcode, 6-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organization).

## Read

Upon receiving a READ command (Figure 3) and an address (clocked into the DI pin), the DO pin of the CAV93C46 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

After the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

## Erase/Write Enable and Disable

The CAV93C46 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAV93C46 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 4.

**Table 8. INSTRUCTION SET**

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6-A0	A5-A0			Read Address AN-A0
ERASE	1	11	A6-A0	A5-A0			Clear Address AN-A0
WRITE	1	01	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN-A0
EWEN	1	00	11XXXXX	11XXXX			Write Enable
EWDS	1	00	00XXXXX	00XXXX			Write Disable
ERAL	1	00	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	00	01XXXXX	01XXXX	D7-D0	D15-D0	Write All Addresses

# CAV93C46

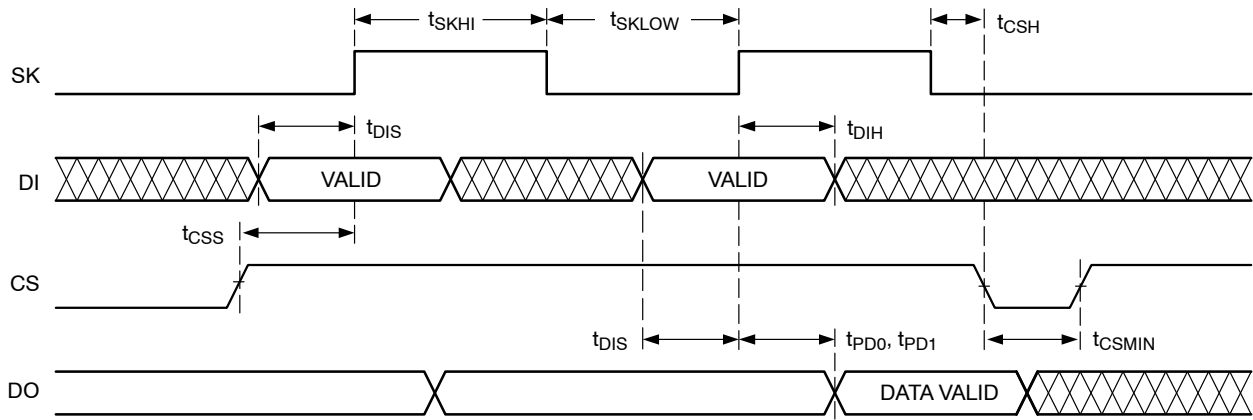


Figure 2. Synchronous Data Timing

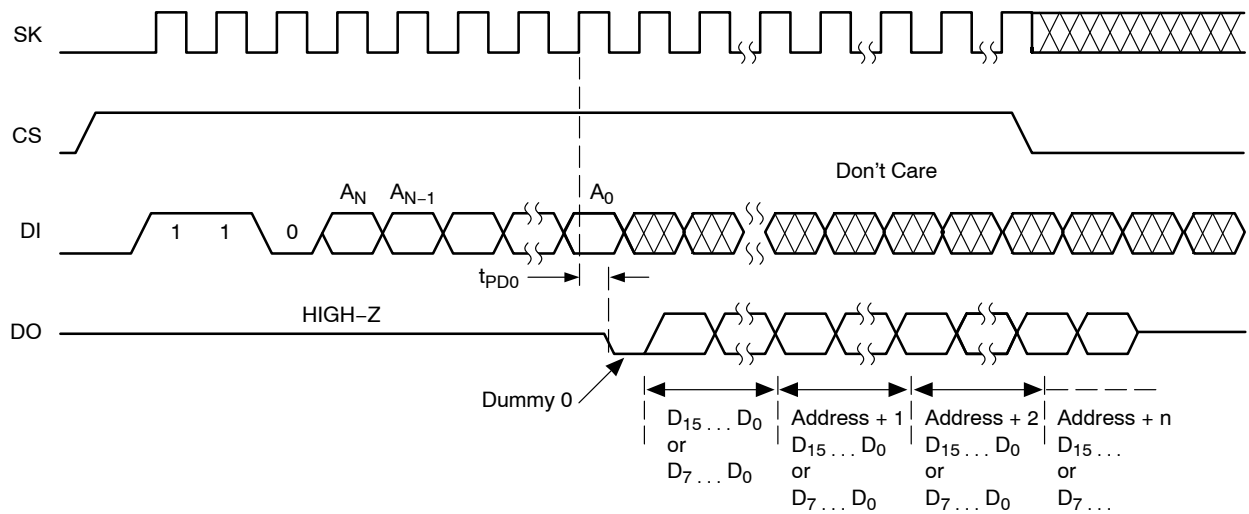


Figure 3. Read Instruction Timing

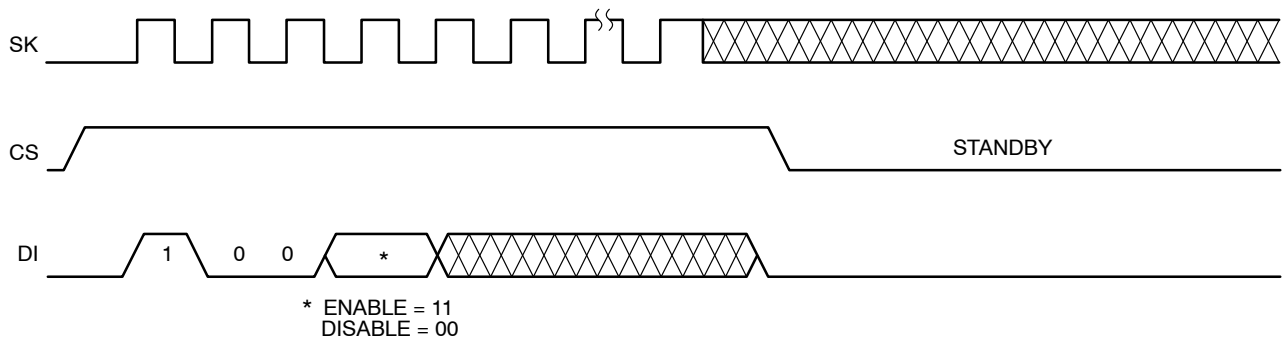


Figure 4. EWEN/EWDS Instruction Timing



# CAV93C46

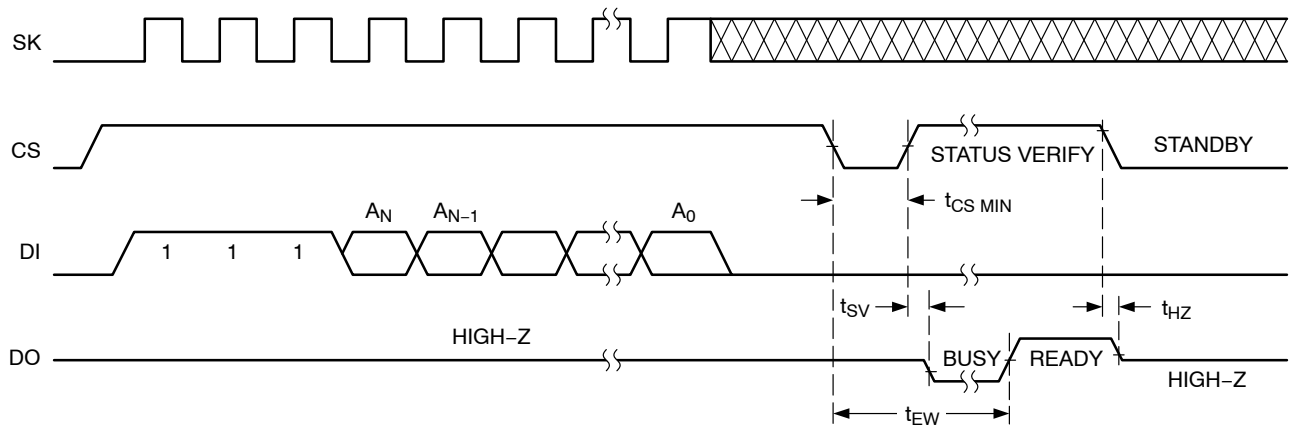


Figure 6. Erase Instruction Timing

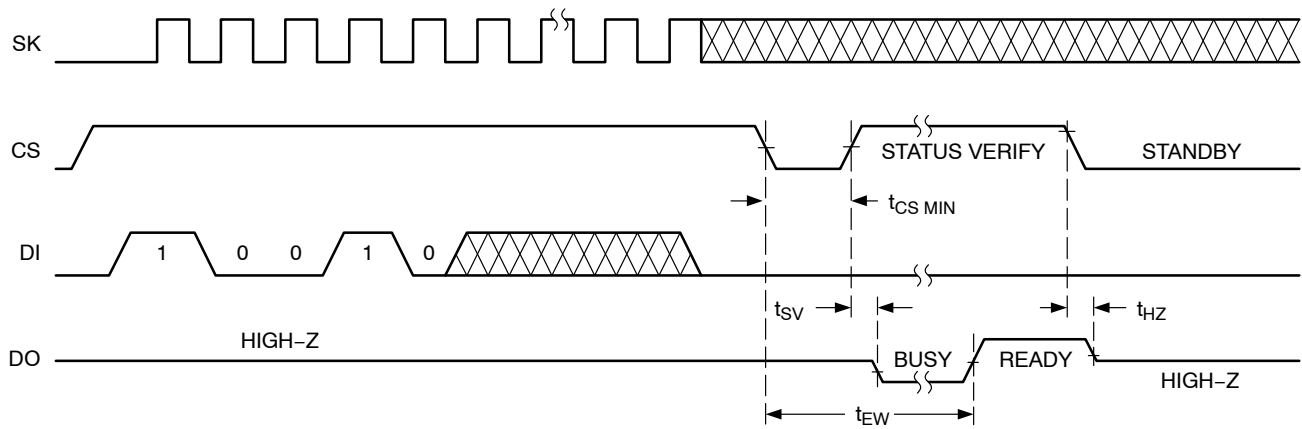


Figure 7. ERAL Instruction Timing

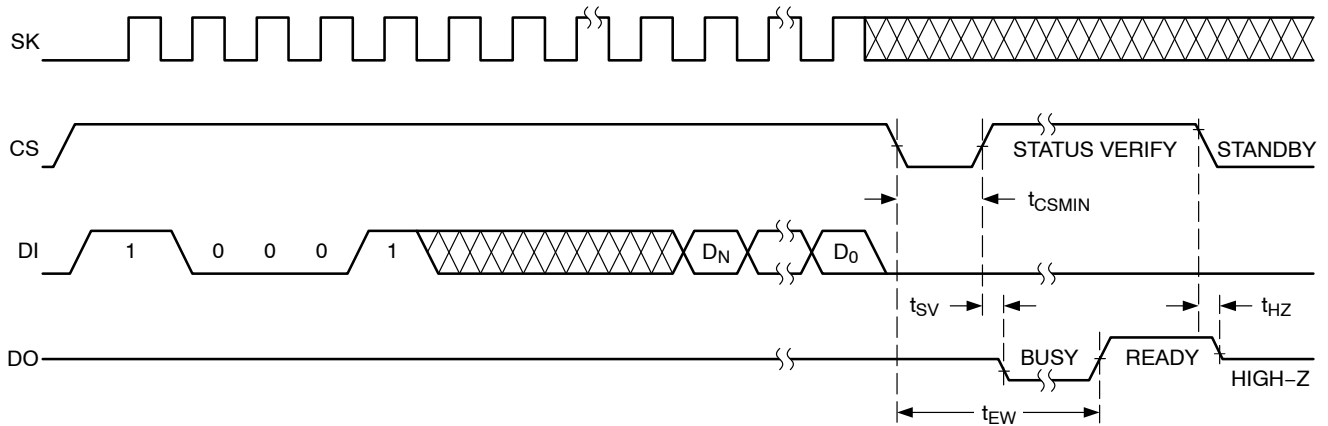


Figure 8. WRAL Instruction Timing

## CAV93C46

### ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping <sup>†</sup>
CAV93C46VE-GT3	93C46P	SOIC-8, JEDEC	-40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAV93C46YE-GT3	M46P	TSSOP-8	-40°C to +125°C	NiPdAu	Tape & Reel, 3,000 Units / Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

8. All packages are RoHS-compliant (Lead-free, Halogen-free).

9. The standard lead finish is NiPdAu.

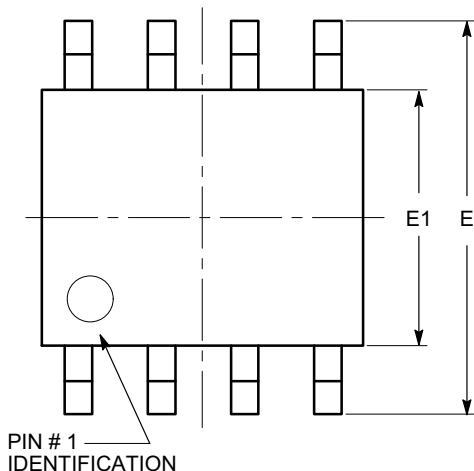
10. For additional package and temperature options, please contact your nearest **onsemi** Sales office.

11. For detailed information and a breakdown of device nomenclature and numbering systems, please see the **onsemi** Device Nomenclature document, TND310/D, available at [www.onsemi.com](http://www.onsemi.com)



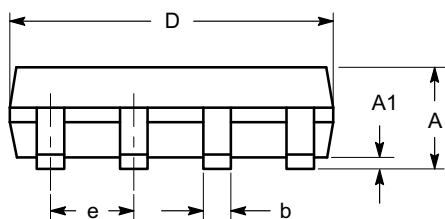
**SOIC-8, 150 mils**  
**CASE 751BD**  
**ISSUE O**

DATE 19 DEC 2008

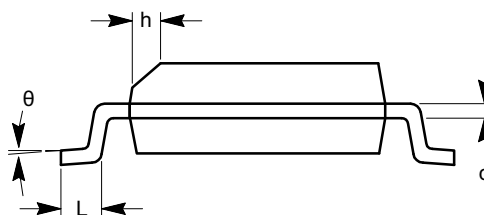


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



**SIDE VIEW**



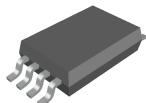
**END VIEW**

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

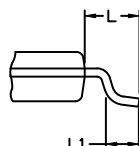
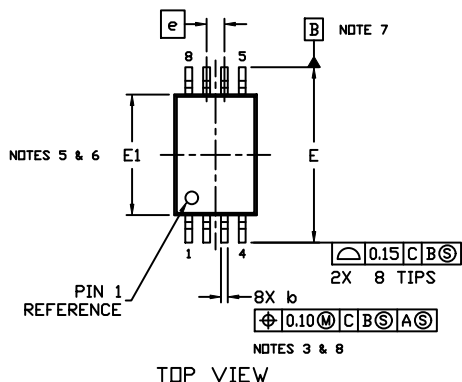
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TSSOP8, 4.4x3.0, 0.65P  
CASE 948AL  
ISSUE A

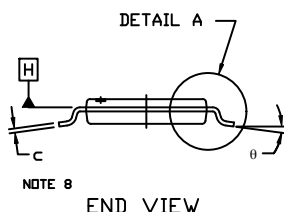
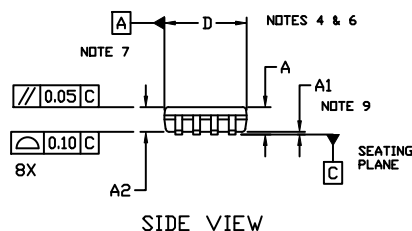
DATE 20 MAY 2022



DETAIL A

NOTES:

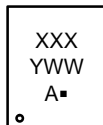
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM PLANE H.
7. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
8. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
9. A1 IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



END VIEW

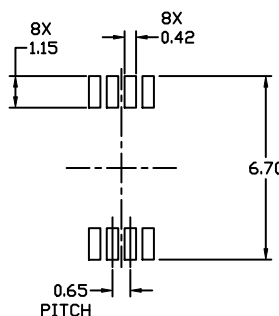
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

GENERIC  
MARKING DIAGRAM\*



XXX = Specific Device Code  
Y = Year  
WW = Work Week  
A = Assembly Location  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED  
MOUNTING FOOTPRINT\*

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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DESCRIPTION:	TSSOP8, 4.4X3.0, 0.65P	PAGE 1 OF 1

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