256-position SPI Compatible Digital Potentiometer (POT)

CAT5172

The CAT5172 is a 256-position digital linear taper potentiometer ideally suited for replacing mechanical potentiometers and variable resistors. Like mechanical potentiometers, the CAT5172 has a resistive element, which can span V_{CC} to Ground or float anywhere between the power supply rails.

Wiper settings are controlled through an SPI-compatible digital interface. Upon power-up, the wiper assumes a mid-span position and may be repositioned anytime after the power is stable.

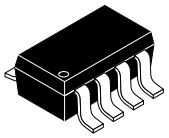
The CAT5172 operates from 2.7 V to 5.5 V, while consuming less than 2 μA. This low operating current, combined with a small package footprint, make the CAT5172 ideal for battery-powered portable appliance.

Features

- 256-position
- End-to-End Resistance: 50 kΩ, 100 kΩ
- SPI Compatible Interface
- Power-on Preset to Midscale
- Single Supply 2.7 V to 5.5 V
- Low Temperature Coefficient 100 ppm/°C
- Low Power, I_{DD} 2 μA max
- Wide Operating Temperature −40°C to +85°C
- SOT−23 8-lead (2.9 mm × 3 mm) Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Potentiometer Replacement
- Transducer Adjustment of Pressure, Temperature, Position, Chemical, and Optical Sensors
- RF Amplifier Biasing
- Gain Control and Offset Adjustment



SOT23−8
TB SUFFIX
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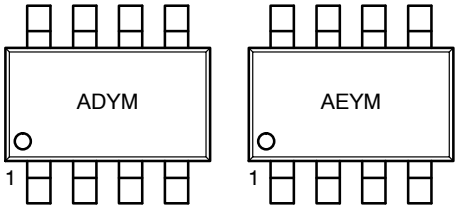
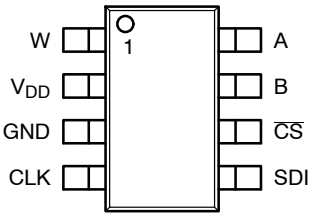
MARKING DIAGRAM



AD = 50 kΩ
AE = 100 kΩ
Y = Production Year (Last Digit)
M = Production Month (1 − 9, A, B, C)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

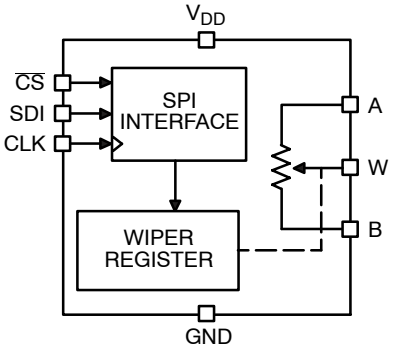


Figure 1. Functional Block Diagram

Table 1. ORDERING INFORMATION

Part Number	Resistance	Temperature Range	Package	Shipping†
CAT5172TBI−00GT3	100 kΩ	−40°C to 85°C	SOT−23−8 (Pb−Free)	3,000/Tape & Reel

DISCONTINUED (Note 1)

CAT5172TBI−50GT3	50 kΩ	−40°C to 85°C	SOT−23−8 (Pb−Free)	3,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.
2. For detailed information and a breakdown of device nomenclature and numbering systems, please see the **onsemi** Device Nomenclature document, TND310/D, available at www.onsemi.com.

Table 2. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	W	Resistor's Wiper Terminal.
2	V_{DD}	Positive Power Supply.
3	GND	Digital Ground.
4	CLK	Serial Clock Input. Positive edge triggered.
5	SDI	Serial Data Input.
6	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data will be loaded into the DAC register.
7	B	Bottom Terminal of resistive element.
8	A	Top Terminal of resistive element.

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 3)

Rating	Value	Unit
V_{DD} to GND	−0.3 to 6.5	V
V_A, V_B, V_W to GND	V_{DD}	
I_{MAX}	±20	mA
Digital Inputs and Output Voltage to GND	0 to 6.5	V
Operating Temperature Range	−40 to +85	°C
Maximum Junction Temperature (T_{JMAX})	150	°C
Storage Temperature	−65 to +150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

Table 4. ELECTRICAL CHARACTERISTICS: 50 kΩ and 100 kΩ Versions

V_{DD} = 5 V ±10%, or 3 V ±10%; $V_A = V_{DD}$; V_B = 0 V; –40°C < T_A < +85°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Unit
DC CHARACTERISTICS – RHEOSTAT MODE						
R–DNL	Resistor Differential Nonlinearity (Note 5)	R_{WB}, V_A = no connection	–1	±0.1	+1	LSB
R–INL	Resistor Integral Nonlinearity (Note 5)	R_{WB}, V_A = no connection	–2	±0.4	+2	LSB
ΔR_{AB}	Nominal Resistor Tolerance (Note 6)	T_A = 25°C	–20		+20	%
$\Delta R_{AB}/\Delta T$	Resistance Temperature Coefficient	$V_{AB} = V_{DD}$, Wiper = no connection		100		ppm/°C
R_W	Wiper Resistance	V_{DD} = 5 V		50	120	Ω
		V_{DD} = 3 V		100	250	
DC CHARACTERISTICS – POTENTIOMETER DIVIDER MODE						
N	Resolution				8	Bits
DNL	Differential Nonlinearity (Note 7)		–1	±0.1	+1	LSB
INL	Integral Nonlinearity (Note 7)		–1	±0.4	+1	LSB
$\Delta V_W/\Delta T$	Voltage Divider Temperature Coefficient	Code = 0x80		100		ppm/°C
V_{WFSE}	Full-Scale Error	Code = 0xFF	–3	–1	0	LSB
V_{WZSE}	Zero-Scale Error	Code = 0x00	0	1	3	LSB
RESISTOR TERMINALS						
$V_{A,B,W}$	Voltage Range (Note 8)		GND		V_{DD}	V
$C_{A,B}$	Capacitance (Note 9) A, B	f = 1 MHz, measured to GND, Code = 0 x 80		45		pF
C_W	Capacitance (Note 9) W	f = 1 MHz, measured to GND, Code = 0 x 80		60		pF
I_{CM}	Common-Mode Leakage (Note 9)	$V_A = V_B = V_{DD}/2$		1		nA
DIGITAL INPUTS						
V_{IH}	Input Logic High	V_{DD} = 5 V	0.7 x V_{DD}			V
V_{IL}	Input Logic Low	V_{DD} = 5 V			0.3V_{DD}	V
V_{IH}	Input Logic High	V_{DD} = 3 V	0.7 x V_{DD}			V
V_{IL}	Input Logic Low	V_{DD} = 3 V			0.3V_{DD}	V
I_{IL}	Input Current	V_{IN} = 0 V or 5 V			±1	μA
C_{IL}	Input Capacitance (Note 9)			5		pF
POWER SUPPLIES						
$V_{DD\ RANGE}$	Power Supply Range		2.7		5.5	V
I_{DD}	Supply Current	V_{IH} = 5 V or V_{IL} = 0 V		0.3	2	μA
P_{DISS}	Power Dissipation (Note 10)	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
PSS	Power Supply Sensitivity	ΔV_{DD} = +5 V ±10%, Code = Midscale			±0.05	%/%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
5. Resistor position nonlinearity error R–INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R–DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
6. $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.
7. INL and DNL are measured at VW with the digital POT configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
8. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
9. Guaranteed by design and not subject to production test.
10. PDISS is calculated from (I_{DD} x V_{DD}). CMOS logic level inputs result in minimum power dissipation.
11. All dynamic characteristics use V_{DD} = 5 V.

Table 4. ELECTRICAL CHARACTERISTICS: 50 kΩ and 100 kΩ Versions (continued)
V_{DD} = 5 V ±10%, or 3 V ±10%; $V_A = V_{DD}$; V_B = 0 V; –40°C < T_A < +85°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Unit
DYNAMIC CHARACTERISTICS (Notes 9 and 11)						
BW	Bandwidth –3 dB	R_{AB} = 50 kΩ / 100 kΩ, Code = 0x80		100/40		kHz
THD_W	Total Harmonic Distortion	V_A =1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
t_S	V_W Settling Time (50 kΩ/100 kΩ)	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
5. Resistor position nonlinearity error R–INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R–DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
6. $V_{AB} = V_{DD}$, Wiper (V_W) = no connect.
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8. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
9. Guaranteed by design and not subject to production test.
10. PDISS is calculated from (I_{DD} x V_{DD}). CMOS logic level inputs result in minimum power dissipation.
11. All dynamic characteristics use V_{DD} = 5 V.

Table 5. TIMING CHARACTERISTICS: 50 kΩ and 100 kΩ Versions
V_{DD} = 5 V ± 10%, or 3 V ± 10%; $V_A = V_{DD}$; V_B = 0 V; –40°C < T_A < +85°C; unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ (Note 12)	Max	Unit
SPI INTERFACE TIMING CHARACTERISTICS (Notes 13 and 14) **(Specifications Apply to All Parts)**						
f_{CLK}	Clock Frequency				25	MHz
t_{CH}, t_{CL}	Input Clock Pulse width	Clock level high or low	20			ns
t_{DS}	Data Setup Time		5			ns
t_{DH}	Data Hold Time		5			ns
T_{CSS}	$\overline{CS}$ Setup Time		15			ns
T_{CSW}	$\overline{CS}$ High Pulse Width		40			ns
T_{CSH0}	CLK Fall to $\overline{CS}$ Fall Hold Time		0			ns
T_{CSH1}	CLK Fall to $\overline{CS}$ Rise Hold Time		0			ns
T_{CS1}	$\overline{CS}$ Rise to Clock Rise Setup		10			ns

12. Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
13. Guaranteed by design and not subject to production test.
14. See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

SPI INTERFACE

Table 6. CAT5172 SERIAL DATA−WORD FORMAT

B7	B6	B5	B4	B3	B2	B1	B0
D7 MSB 2^7	D6	D5	D4	D3	D2	D1	D0 LSB 2^0

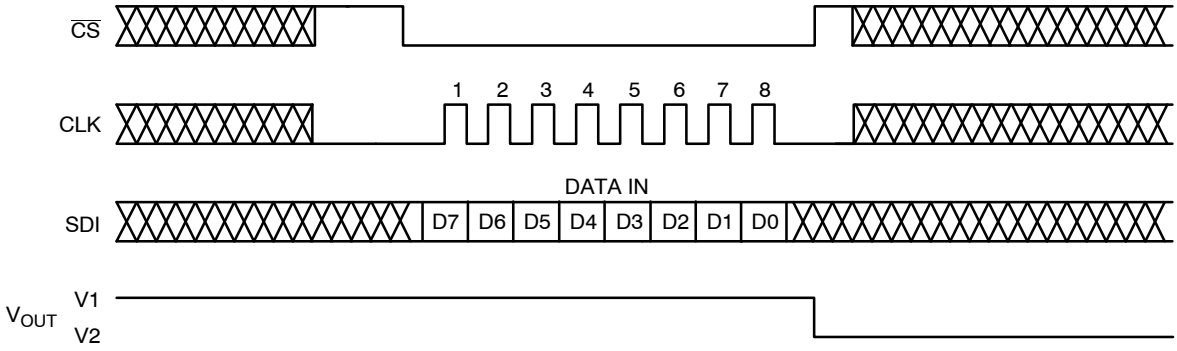


Figure 2. CAT5172 SPI Interface Timing Diagram (V_A = 5 V, V_B = 0 V, V_W = V_{OUT})

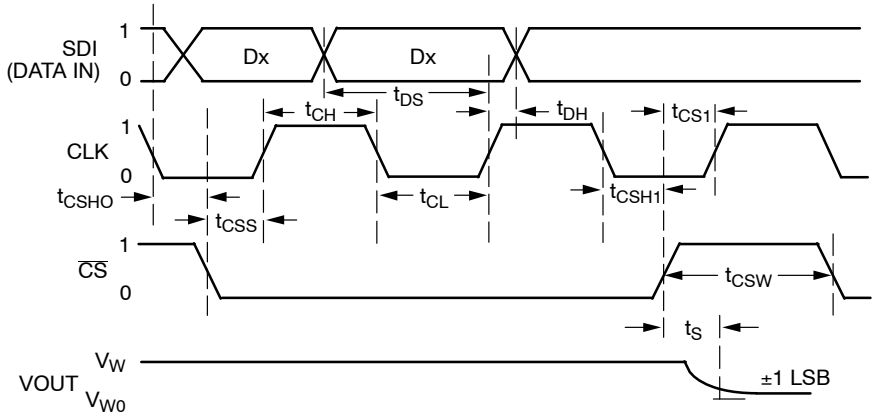


Figure 3. SPI Interface Detailed Timing Diagram (V_A = 5 V, V_B = 0 V, V_W = V_{OUT})

TYPICAL CHARACTERISTICS

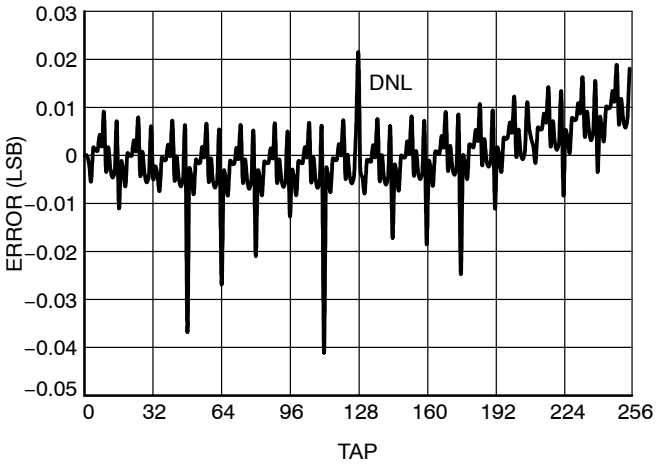


Figure 4. Differential Non−Linearity, V_{CC} = 5.6 V

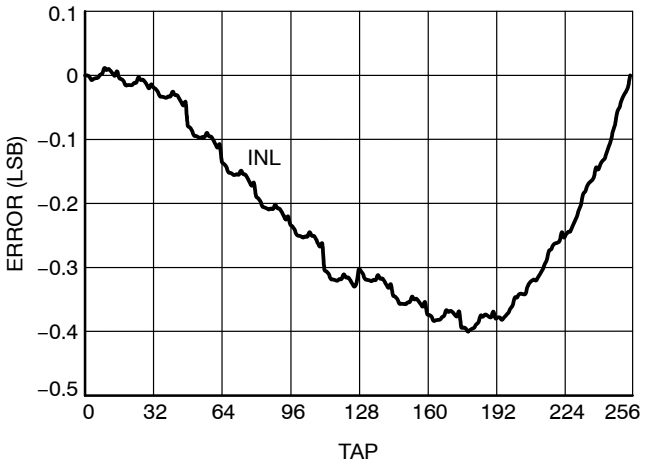


Figure 5. Integral Non−Linearity, V_{CC} = 5.6 V

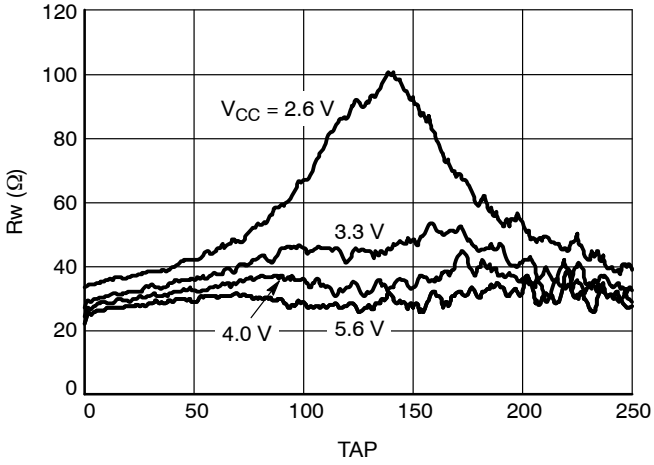


Figure 6. Wiper Resistance at Room Temperature

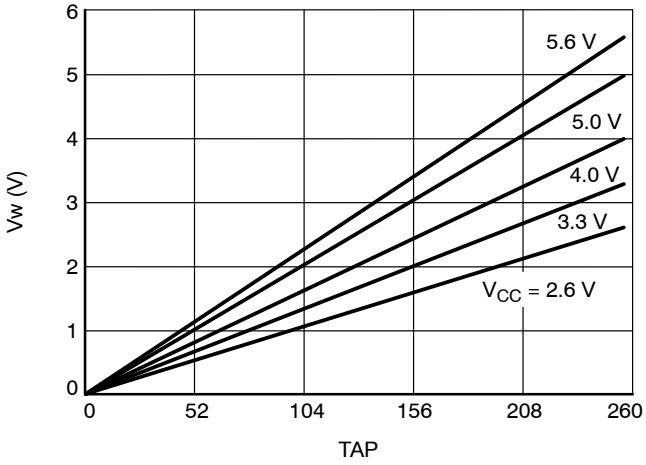


Figure 7. Wiper Voltage

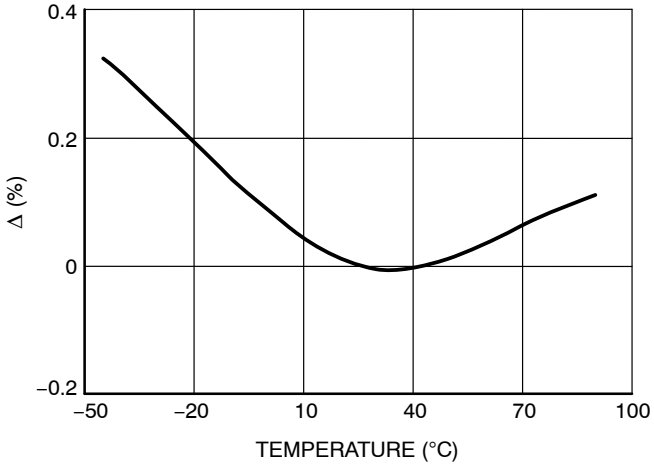


Figure 8. Change in End−to−End Resistance

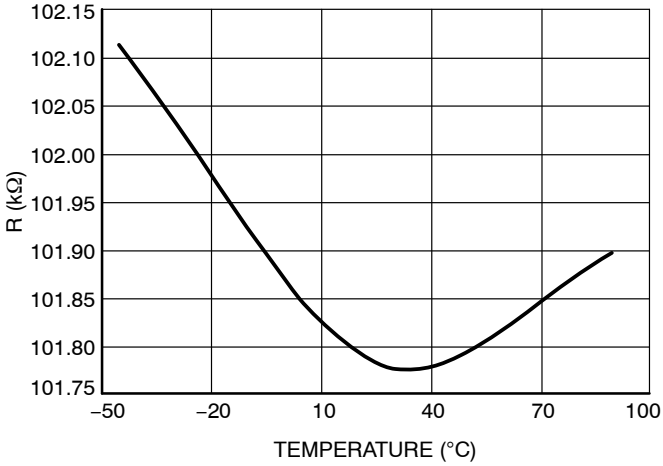


Figure 9. End−to−End Resistance vs. Temperature

TYPICAL CHARACTERISTICS (continued)

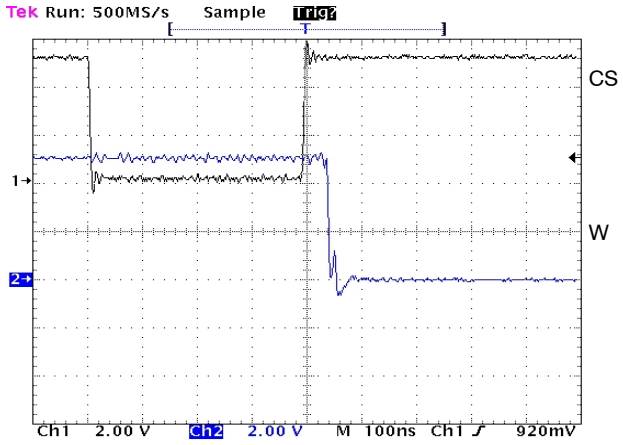


Figure 10. Wiper's Transition from Position 0xFF to Position 0x00 Relative to the CS Disable, V_{CC} = 5 V

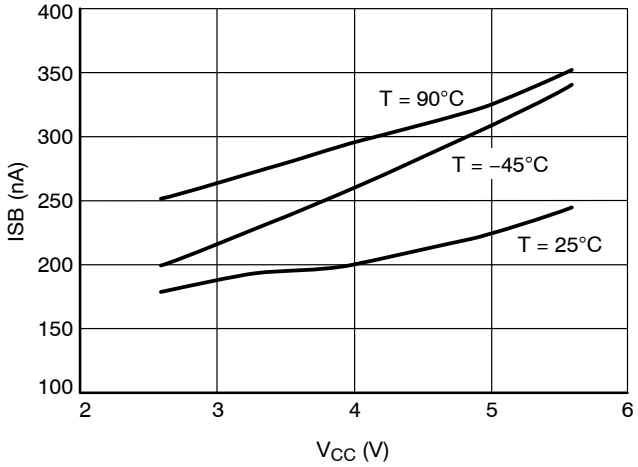


Figure 11. Standby Current

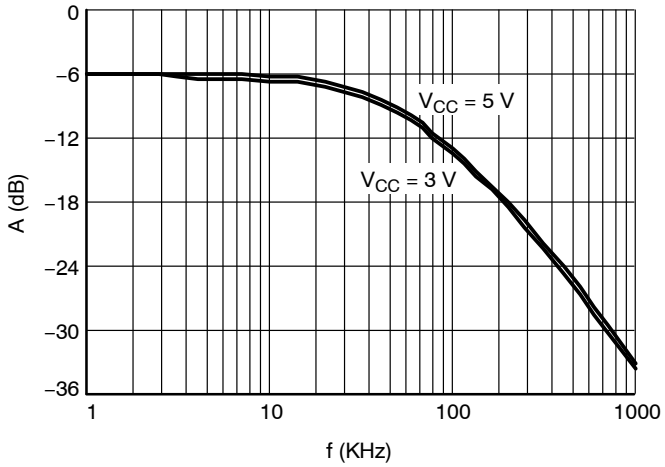


Figure 12. Gain vs. Bandwidth (Tap 0x80)

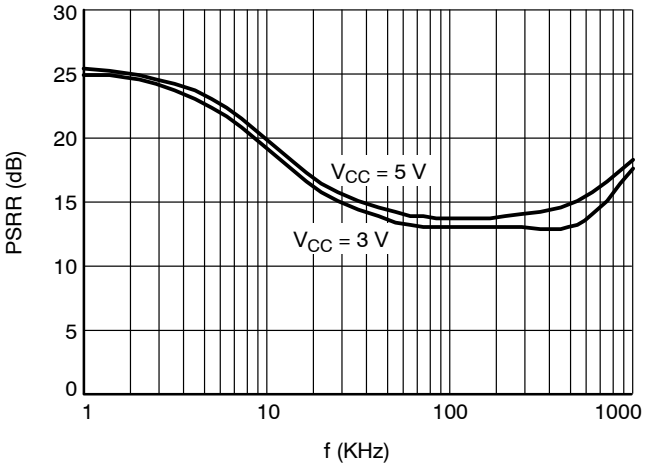


Figure 13. PSRR

BASIC OPERATION

The CAT5172 is a 256-position digitally controlled potentiometer. When power is first applied the wiper assumes a mid-scale position and will remain there as long as $\overline{CS}$ remians high. Once the power supply is stable the wiper may be repositioned via the SPI compatible interface. The rising edge of the $\overline{CS}$ signal acts as the transfer command and each time $\overline{CS}$ transitions from LOW to HIGH the contents of the input register are loaded into the wiper register.

In the power-up cycle, the input data register is cleared, setting all bits to 0 and the wiper register is loaded with 0x80 (128 Decimal) which moves the wiper to its midscale position. If $\overline{CS}$ is toggled CAT5172 transfers the contents of the input data register (0x00) to the wiper register moving the wiper to the bottom-most position (W = terminal B). This transfer is independent of whether new data has been input or not because $\overline{CS}$ acts as the transfer command.

PROGRAMMING: VARIABLE RESISTOR

Rheostat Mode

The resistance between terminals A and B, R_{AB}, has a nominal value of 50 kΩ or 100 kΩ and has 256 contact points accessed by the wiper terminal, plus the B terminal contact. Data in the 8-bit Wiper register is decoded to select one of these 256 possible settings.

The wiper's first connection is at the B terminal, corresponding to control position 0x00. Ideally this would present a 0 Ω between the Wiper and B, but just as with a mechanical rheostat there is a small amount of contact resistance to be considered, there is a wiper resistance comprised of the R_{ON} of the FET switch connecting the wiper output with its respective contact point. In CAT5172 this 'contact' resistance is typically 50 Ω. Thus a connection setting of 0x00 yields a minimum resistance of 50 Ω between terminals W and B.

For a 100 kΩ device, the second connection, or the first tap point, corresponds to 441 Ω ($R_{WB} = R_{AB}/256 + R_W$ = 390.6 + 50 Ω) for data 0x01. The third connection is the next tap point, is 831 Ω (2 × 390.6 + 50 Ω) for data 0x02, and so on. Figure 14 shows a simplified equivalent circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

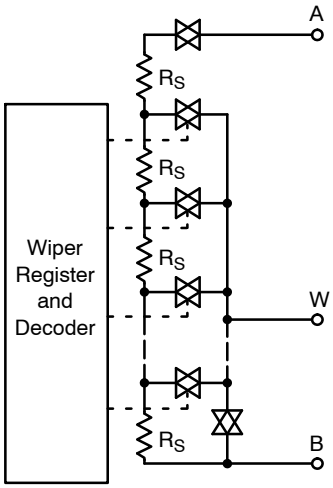


Figure 14. CAT5172 Equivalent Digital POT Circuit

The equation for determining the digitally programmed output resistance between W and B is

$$R_{WB} = \frac{D}{256} R_{AB} + R_W \qquad \text{(eq. 1)}$$

where D is the decimal equivalent of the binary code loaded in the 8-bit Wiper register, R_{AB} is the end-to-end resistance, and R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 100 kΩ and the A terminal is open circuited, the following output resistance R_{WB} will be set for the indicated Wiper register codes:

Table 7. CODES AND CORRESPONDING R_{WB} RESISTANCE FOR R_{AB} = 100 kΩ, V_{DD} = 5 V

D (Dec.)	R_{WB} (Ω)	Output State
255	99,559	Full Scale (R_{AB} – 1 LSB + R_W)
128	50,050	Midscale
1	441	1 LSB
0	50	Zero Scale (Wiper Contact Resistance)

Be aware that in the zero-scale position, the wiper resistance of 50 Ω is still present. Current flow between W and B in this condition should be limited to a maximum pulsed current of no more than 20 mA. Failure to heed this restriction can cause degradation or possible destruction of the internal switch contact.

Similar to the mechanical potentiometer, the resistance of the digital POT between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} R_{AB} + R_W \qquad \text{(eq. 2)}$$

For R_{AB} = 100 kΩ and the B terminal open circuited, the following output resistance R_{WA} will be set for the indicated Wiper register codes.

Table 8. CODES AND CORRESPONDING R_{WA} RESISTANCE FOR R_{AB} = 100 kΩ, V_{DD} = 5 V

D (Dec.)	R_{WA} (Ω)	Output State
255	441	Full Scale
128	50,050	Midscale
1	99,659	1 LSB
0	100,050	Zero Scale

Typical device to device resistance matching is lot dependent and may vary by up to ±20%.

SPI Compatible 3-wire Serial Bus

Control of CAT5172 is through a 3-wire SPI compatible digital interface (SDI, $\overline{CS}$, and CLK).

The CLK input is rising-edge sensitive and requires crisp transitions to avoid clocking incorrect data into the serial input register. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (Figure 1). Each 8-bit serial word must be loaded starting with the MSB. The format of the word is shown in Table 6.

Data loaded into CAT5172's 8-bit serial input register is transferred to the internal Wiper register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

ESD Protection

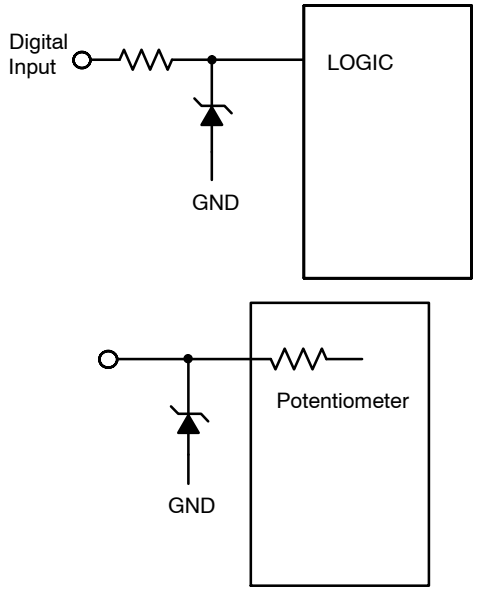


Figure 15. ESD Protection Networks

Terminal Voltage Operating Range

The CAT5172 V_{DD} and GND power supply define the limits for proper 3-terminal digital potentiometer operation. Signals or potentials applied to terminals A, B or the wiper must remain inside the span of V_{DD} and GND. Signals which attempt to go outside these boundaries will be clamped by the internal forward biased diodes.

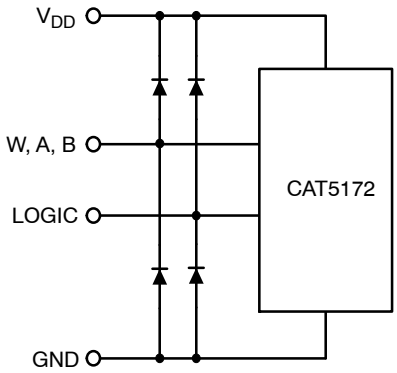


Figure 16.

Power-up Sequence

Because ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 15), it is recommended that V_{DD}/GND be powered before applying any voltage to terminals A, B, and W. The ideal power-up sequence is: GND, V_{DD}, digital inputs, and then $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

Power Supply Bypassing

Good design practice employs compact, minimum lead length layout design. Leads should be as direct as possible. It is also recommended to bypass the power supplies with quality low ESR Ceramic chip capacitors of 0.01 μF to 0.1 μF. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors can also be applied at the supplies to suppress transient disturbances and low frequency ripple. As a further precaution digital ground should be joined remotely to the analog ground at one point to minimize the ground bounce.

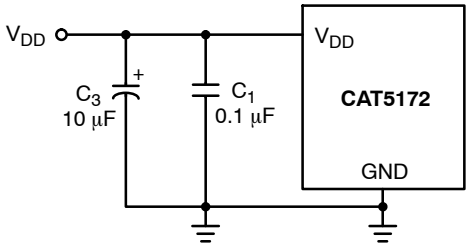
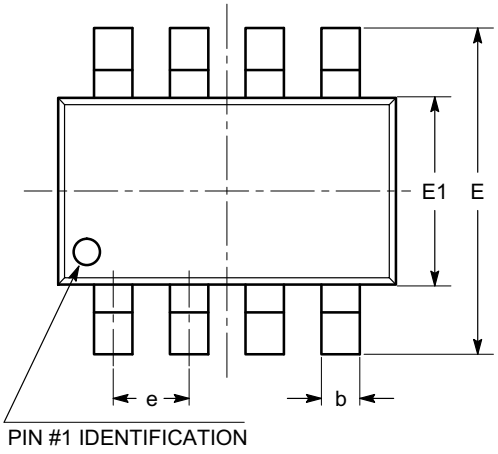


Figure 17. Power Supply Bypassing

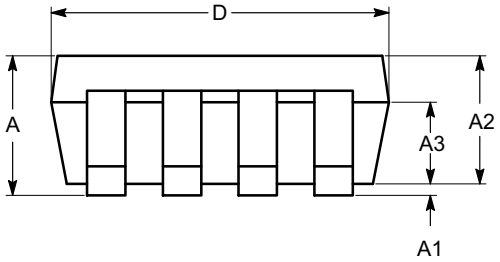
SOT−23, 8 Lead
CASE 527AK
ISSUE A

DATE 18 MAR 2009

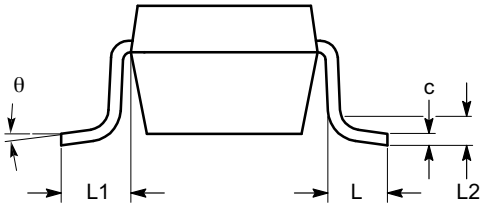


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.10	1.30
A3	0.60		0.80
b	0.28		0.38
c	0.08		0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.65 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

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