CAT5120, CAT5121, CAT5122

16-tap Digital Potentiometers (POTs) with 2-wire Interface

ON Semiconductor®

http://onsemi.com

SC−70
SD SUFFIX
CASE 419AD

SOT−23
TB SUFFIX
CASE 527AJ

SC−70
SD SUFFIX
CASE 419AC

SOT−23
TB SUFFIX
CASE 527AH

Description

CAT5120/5121/5122 linear-taper digital POTs perform the same function as a mechanical potentiometer or a variable resistor. These devices consist of a fixed resistor and a wiper contact with 16-tap points that are digitally controlled through a 2-wire up/down serial interface.

The CAT5120 is configured as a potentiometer. The CAT5121 and CAT5122 are configured as variable resistors. See *Pin Configurations* for part functionality.

Two resistance values are available: 10 kΩ and 50 kΩ. These are available in space-saving 5-pin and 6-pin SC−70 and SOT−23 packages.

Features

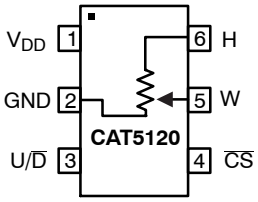
- 0.3 μA Ultra-low Standby Current
- Single-supply Operation: 2.7 V to 5.5 V
- Glitchless Switching between Resistor Taps
- Power-on Reset to Midscale
- 2-wire Up/Down Serial Interface
- Resistance Values: 10 kΩ, 50 kΩ
- Available in SC−70 and SOT−23 Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

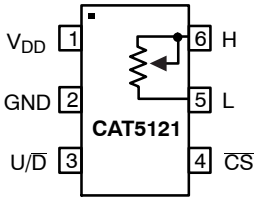
- LCD Screen Adjustment
- Volume Control
- Mechanical Potentiometer Replacement
- Gain Adjustment
- Line Impedance Matching

PIN CONFIGURATIONS

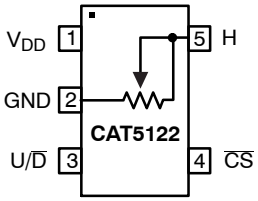
SC−70
SOT−23



SC−70
SOT−23



SC−70
SOT−23



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

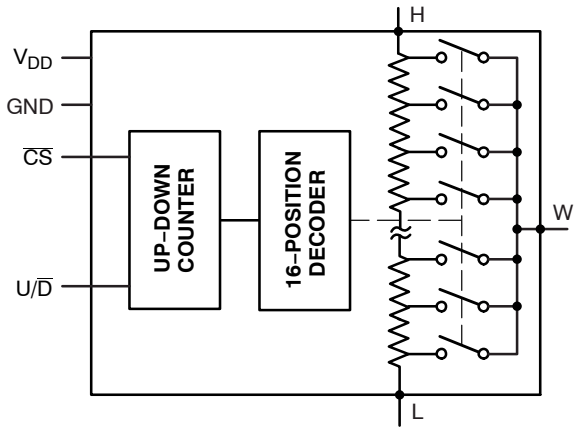


Figure 1. Functional Diagram

Table 1. PIN DESCRIPTIONS

Name	Description
V_{DD}	Power Supply
GND	Ground
U/$\overline{D}$	Up/$\overline{Down}$ Control Input. With $\overline{CS}$ low, a low-to-high transition increments or decrements the wiper position.
$\overline{CS}$	Chip Select Input. A high-to-low $\overline{CS}$ transition determines the mode: increment if U/$\overline{D}$ is high, or decrement if U/$\overline{D}$ is low.
L	Low Terminal of Resistor
W	Wiper Terminal of Resistor
H	High Terminal of Resistor

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{DD} to GND	−0.3 to +6	V
All Other Pins to GND	−0.3 to (V_{DD} + 0.3)	V
Input and Output Latch-up Immunity	±200	mA
Maximum Continuous Current into H, L and W 50 kΩ 10 kΩ	 ±1.3 ±1.3	mA
Continuous Power Dissipation (T_A = +70°C) 5-pin SC−70 (Note 1) 6-pin SC−70 (Note 1)	 247 245	mW
Operating Temperature Range	−40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature Range	−65 to +150	°C
Soldering Temperature (soldering, 10 s)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Derate 3.1 mW/°C above T_A = +70°C

Table 3. ELECTRICAL CHARACTERISTICS
(V_{DD} = 2.7 V to 5.5 V, $V_H = V_{DD}$, V_L = 0, T_A = −40°C to +85°C. Typical values are at V_{DD} = 2.7 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DC PERFORMANCE						
Resolution			16			Taps
End-to-End Resistance (−50)			37.5	50	62.5	kΩ
End-to-End Resistance (−10)			7.5	10	12.5	
End-to-End Resistance Tempco	TC_R			200		ppm/°C
Ratiometric Resistance Tempco				5		ppm/°C
Integral Non-linearity	INL				±0.5	LSB
Differential Non-linearity	DNL				±0.5	LSB
Zero/Full-Scale Error				±0.1	±0.5	LSB
Wiper Resistance	R_W			200	600	Ω
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
TIMING CHARACTERISTICS (Figures 7, 8)						
U/$\overline{D}$ Mode to $\overline{CS}$ Setup	t_{CU}		25			ns
$\overline{CS}$ to U/$\overline{D}$ Step Setup	t_{CI}		50			ns
$\overline{CS}$ to U/$\overline{D}$ Step Hold	t_{IC}		25			ns
U/$\overline{D}$ Step Low Period	t_{IL}		25			ns
U/$\overline{D}$ Step High Period	t_{IH}		25			ns
Up/$\overline{Down}$ Toggle Rate (Note 2)	f_{TOGGLE}			1		MHz
Output Settling Time (Note 3)	t_{SETTLE}	50 kΩ variable resistor configuration, C_L = 10 pF		1		μs
		50 kΩ potentiometer configuration, C_L = 10 pF		0.25		
POWER SUPPLY						
Supply Voltage	V_{DD}		2.7		5.5	V
Active Supply Current (Note 4)	I_{DD}				25	μA
Standby Supply Current (Note 5)	I_{SB}	V_{DD} = +5 V		0.3	1	μA

2. Up/Down Toggle Rate: $f_{TOGGLE} = 1 / t_{SETTLE}$
3. Typical settling times are dependent on end-to-end resistance.
4. Supply current measured while changing wiper tap, f_{TOGGLE} = 1 MHz.
5. Supply current measured while wiper position is fixed.

TYPICAL OPERATING CHARACTERISTICS

(T_A = 25°C, unless otherwise noted.)

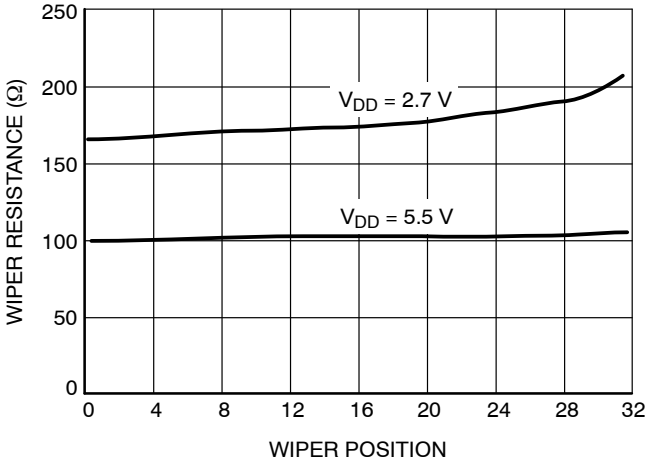


Figure 2. Wiper Resistance vs. Tap Position

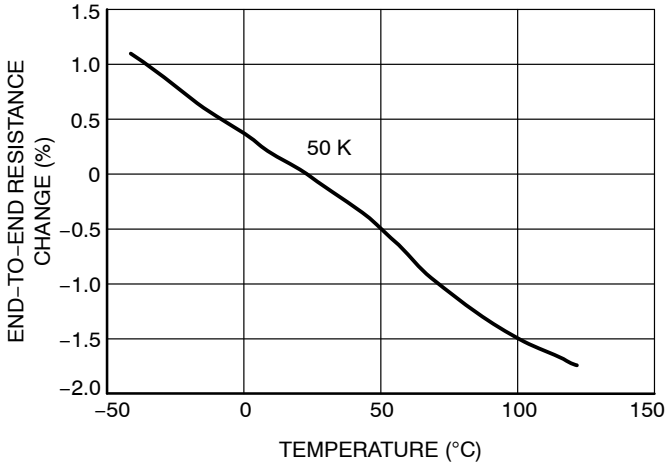


Figure 3. Change in End-to-End Resistance vs. Temperature

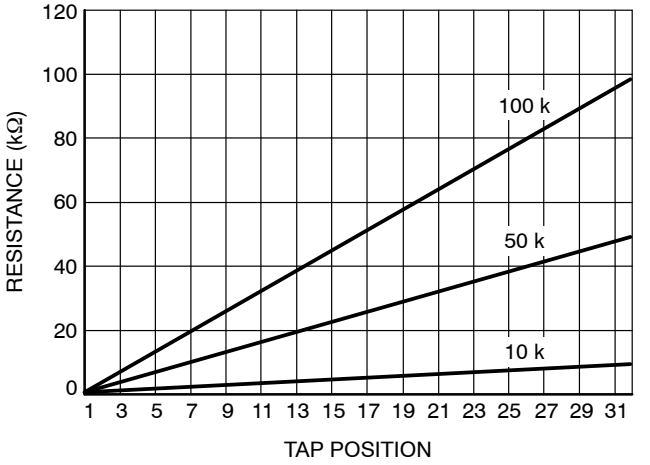


Figure 4. W-to-L Resistance vs. Tap Position

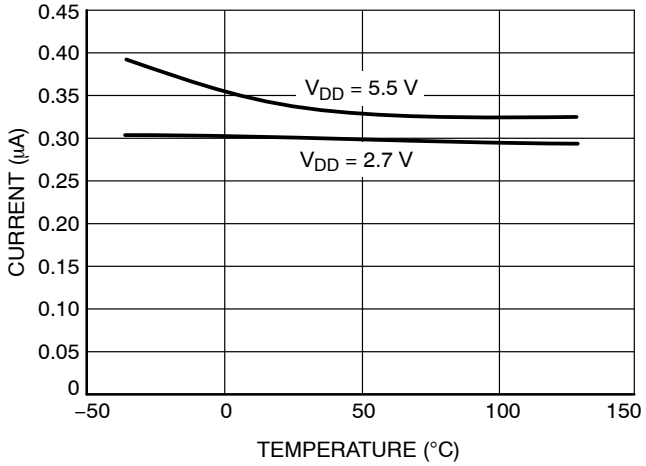


Figure 5. Supply Current vs. Temperature

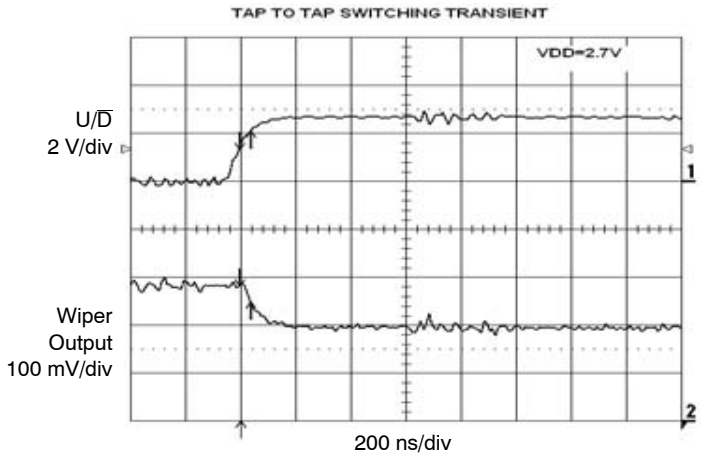


Figure 6. Tap-to-Tap Switching Transient

FUNCTIONAL DESCRIPTION

The CAT5120/5121/5122 consist of a fixed resistor and a wiper contact with 16-tap points that are digitally controlled through a 2-wire up/down serial interface. Two end-to-end resistance values are available: 10 kΩ and 50 kΩ.

The CAT5120 is designed to operate as a potentiometer. In this configuration, the low terminal of the resistor array is connected to ground (pin 2).

The CAT5122 performs as a variable resistor. In this device, the wiper terminal and high terminal of the resistor array is connected at pin 5. The CAT5121 is a similar variable resistor, except the low terminal is connected to pin 5.

Digital Interface Operation

The devices have two modes of operation when the serial interface is active: increment and decrement mode. The serial interface is only active when $\overline{CS}$ is low.

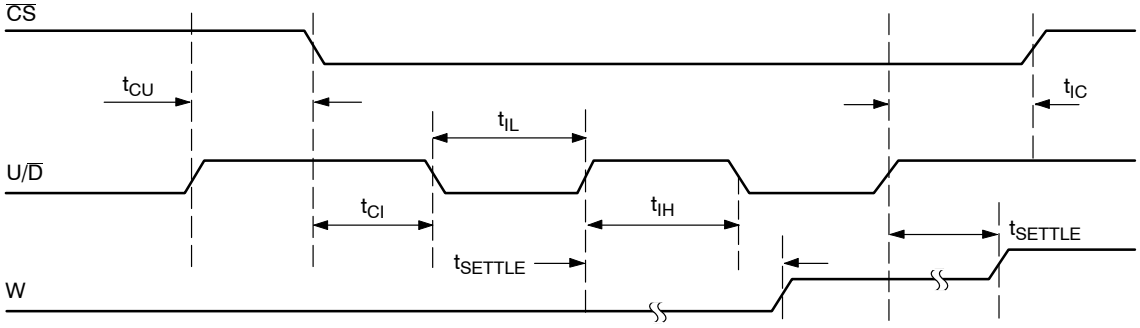
The $\overline{CS}$ and U/$\overline{D}$ inputs control the position of the wiper along the resistor array. When $\overline{CS}$ transitions from high to low, the part will go into increment mode if U/$\overline{D}$ input is high, and into decrement mode when U/$\overline{D}$ input is low. Once the mode is set, the device will remain in that mode until $\overline{CS}$ goes high again. A low-to-high transition at the U/$\overline{D}$ pin will increment or decrement the wiper position depending on the current mode (Figures 7 and 8).

When the $\overline{CS}$ input transitions to high (serial interface inactive), the value of the counter is stored and the wiper position is maintained.

Note that when the wiper reaches the maximum (or minimum) tap position, the wiper will not wrap around to the minimum (or maximum) position.

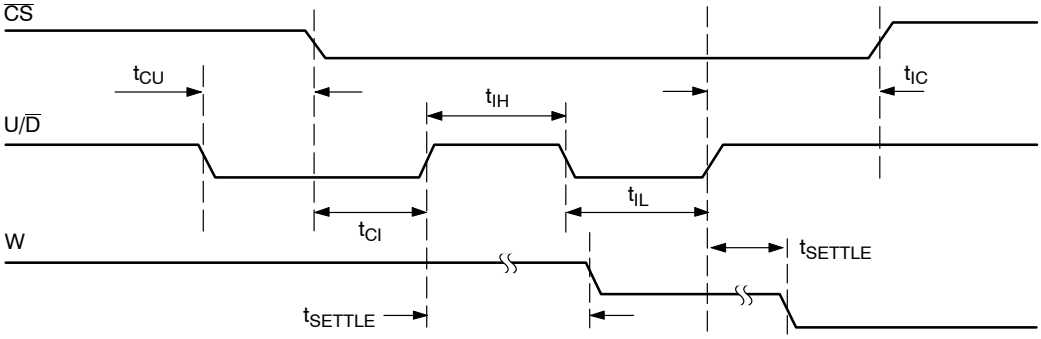
Power-on Reset

All parts in this family feature power-on reset (POR) circuitry that sets the wiper position to midscale at power-up. By default, the chip is in the increment mode.



Note: “W” is not a digital signal. It represents wiper transitions.

Figure 7. Serial Interface Timing Diagram, Increment Mode



Note: “W” is not a digital signal. It represents wiper transitions.

Figure 8. Serial Interface Timing Diagram, Decrement Mode

APPLICATIONS INFORMATION

The devices are intended for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control, where voltage biasing adjusts the display contrast.

Alternative Positive LCD Bias Control

Use an op amp to provide buffering and gain on the output of the CAT5120. Connect the mechanical potentiometer to the positive input of a noninverting op amp (Figure 9) to select a portion of the input signal by digitally controlling the wiper terminal. Figure 10 shows a similar circuit for the CAT5121.

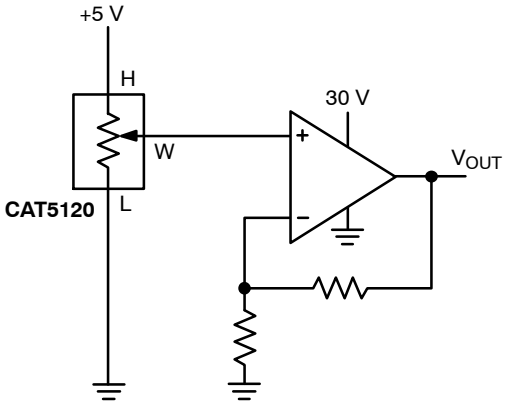


Figure 9. Positive LCD Bias Control

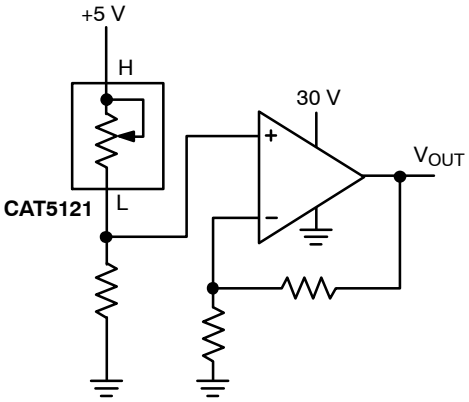


Figure 10. Positive LCD Bias Control

Adjustable Gain

Figures 11 and 12 show how to use the variable resistor to digitally adjust the gain of a noninverting op amp configuration. Connect the CAT5121 in series with a resistor to ground to form the adjustable gain control of a noninverting amplifier. The devices have a low 5 ppm/°C ratiometric tempco that allows for a very stable adjustable gain configuration over temperature.

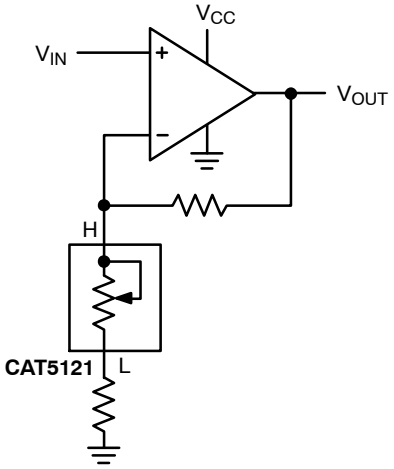


Figure 11. Adjustable Gain Circuit

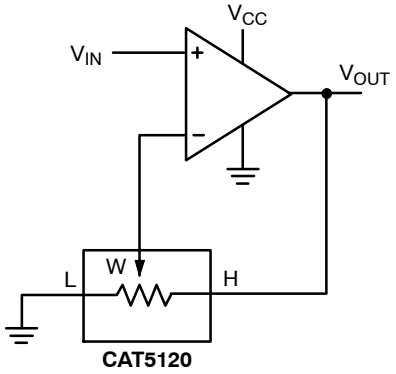


Figure 12. Adjustable Gain Circuit

Table 4. ORDERING INFORMATION

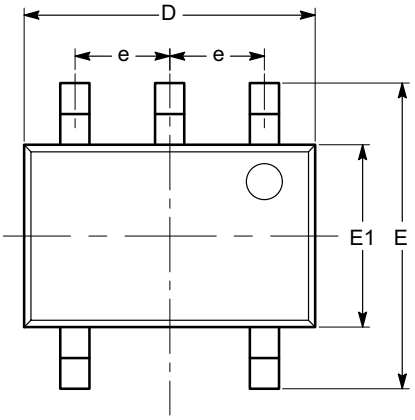
Orderable Part Number	Resistor [kΩ]	Package	Shipping†
CAT5120SDI−10GT3	10	SC70−6 (Pb−Free)	3000 / Tape & Reel
CAT5120TBI−10GT3	10	SOT23−6 (Pb−Free)	3000 / Tape & Reel
CAT5120SDI−50GT3	50	SC70−6 (Pb−Free)	3000 / Tape & Reel
CAT5120TBI−50GT3	50	SOT23−6 (Pb−Free)	3000 / Tape & Reel
CAT5121SDI−10GT3	10	SC70−6 (Pb−Free)	3000 / Tape & Reel
CAT5121TBI−10GT3	10	SOT23−6 (Pb−Free)	3000 / Tape & Reel
CAT5121SDI−50GT3	50	SC70−6 (Pb−Free)	3000 / Tape & Reel
CAT5121TBI−50GT3	50	SOT23−6 (Pb−Free)	3000 / Tape & Reel
CAT5122SDI−10GT3	10	SC70−5 (Pb−Free)	3000 / Tape & Reel
CAT5122TBI−10GT3	10	SOT23−5 (Pb−Free)	3000 / Tape & Reel
CAT5122SDI−50GT3	50	SC70−5 (Pb−Free)	3000 / Tape & Reel
CAT5122TBI−50GT3	50	SOT23−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.

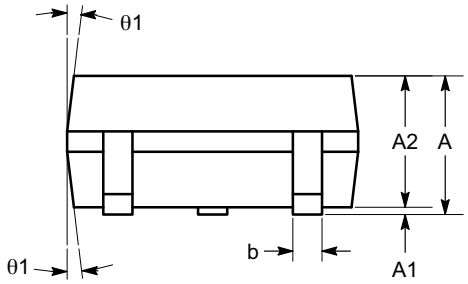
SC−88A (SC−70 5 Lead), 1.25x2
CASE 419AC−01
ISSUE A

DATE 29 JUN 2010

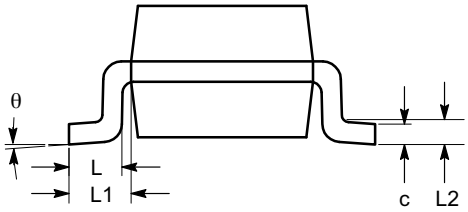


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

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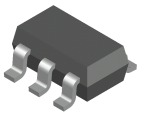
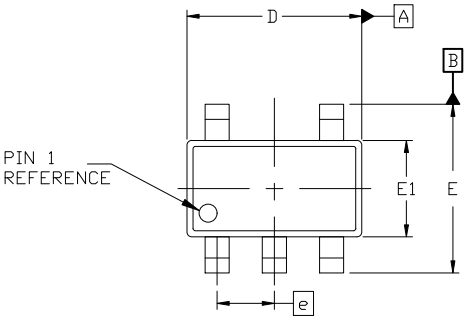
DESCRIPTION:	SC−88A (SC−70 5 LEAD), 1.25X2	PAGE 1 OF 1

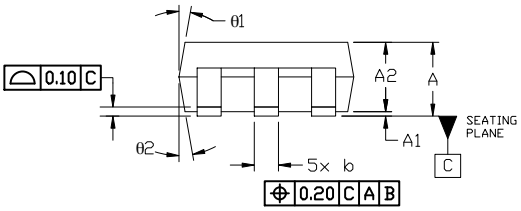


SOT−23, 5 Lead
CASE 527AH
ISSUE A

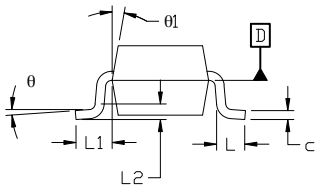
DATE 09 JUN 2021



TOP VIEW



SIDE VIEW

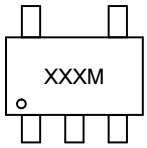


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

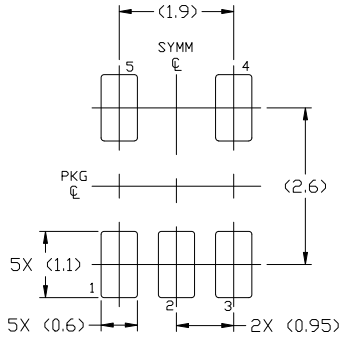
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON34320E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOT−23, 5 LEAD**	**PAGE 1 OF 1**

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