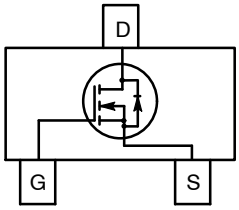
N-Channel Logic Level Enhancement Mode Field Effect Transistor

BSS138W

SOT−323, 3 Lead, 1.25X2
CASE 419AB



Description

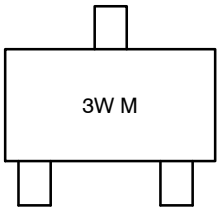
These N−Channel Enhancement Mode Field Effect Transistor. These products have been Designed to minimize on−state resistance while provide rugged, reliable, and fast switching performance.

These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- $R_{DS(on)}$ = 3.5 Ω @ V_{GS} = 10 V, I_D = 0.22 A
  $R_{DS(on)}$ = 6.0 Ω @ V_{GS} = 4.5 V, I_D = 0.22 A
- High Density Cell Design For Extremely Low $R_{DS(on)}$
- Rugged and Reliable
- Compact Industry Standard SOT−323 Surface Mount Package
- These Devices are Pb−Free and Halide Free

MARKING DIAGRAM



3W = Device Code
M = Date Code

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	50	V
V_{GSS}	Gate to Source Voltage	±20	V
I_D	Drain Current − Continuous (Note 1) − Pulsed	 0.21 0.84	A
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16” from Case for 10 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
BSS138W	SOT−323 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
P_D	Maximum Power Dissipation Derate Above 25°C (Note 1)	340 2.72	mW mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	367	°C/W

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	50	–	–	V
$\frac{\Delta BV_{DSS(th)}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	71	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V V_{DS} = 50 V, V_{GS} = 0 V, T_J = 125°C V_{DS} = 30 V, V_{GS} = 0 V	–	–	0.5 5 100	μA μA nA
I_{GSS}	Gate−Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
On Characteristics (Note2)						
$V_{GS(th)}$	Gate to Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	0.8	1.3	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	−3.9	–	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 0.22 A V_{GS} = 4.5 V, I_D = 0.22 A V_{GS} = 10 V, I_D = 0.22 A, T_J = 125°C	–	1.17 1.36 2.16	3.5 6.0 5.8	Ω Ω Ω
$I_{D(on)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	0.2		–	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.22 A	0.12		–	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	38	–	pF
C_{oss}	Output Capacitance		–	5.9	–	pF
C_{rss}	Reverse Transfer Capacitance		–	3.5	–	pF
R_g	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz	–	11	–	Ω
Switching Characteristics						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 30 V, I_D = 0.29 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	2.3	5	ns
t_r	Turn−On Rise Time		–	1.9	18	ns
$t_{d(off)}$	Turn−Off Delay Time		–	6.7	36	ns
t_f	Turn−Off Fall Time		–	6.5	14	ns
Q_g	Total Gate Change	V_{DS} = 25 V, I_D = 0.22 A, V_{GS} = 10 V	–	1.1	–	nC
Q_{gs}	Gate−Source Change		–	0.12	–	nC
Q_{gd}	Gate−Drain Change		–	0.22	–	nC
Drain−Source Diode Characteristics						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	0.22	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0 44 A (Note 2)	–	–	1.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. 367°C/W When Mounted on a minimum pad.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

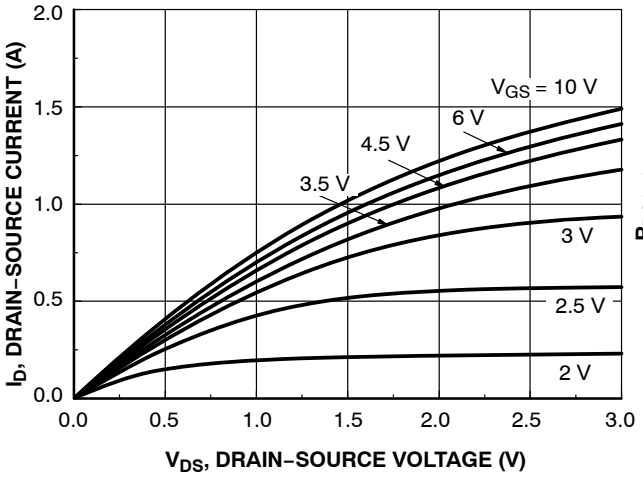


Figure 1. On−Region Characteristics

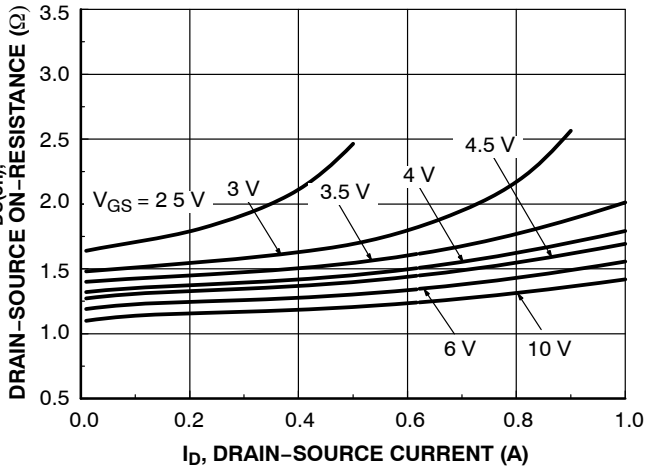


Figure 2. On−Resistance Variation With Drain Current and Gate Voltage

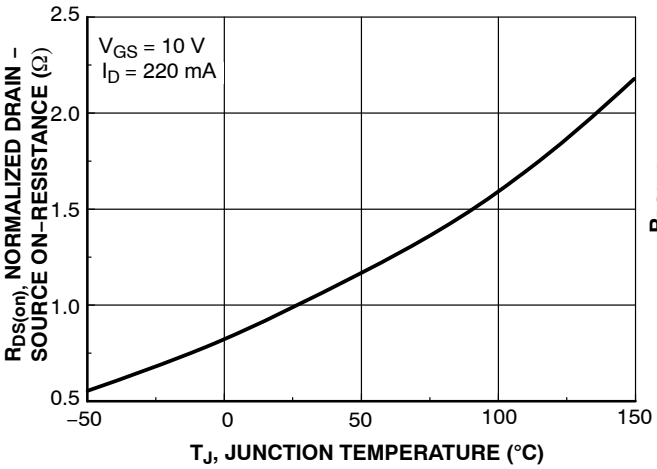


Figure 3. On−Resistance Variation with Temperature.

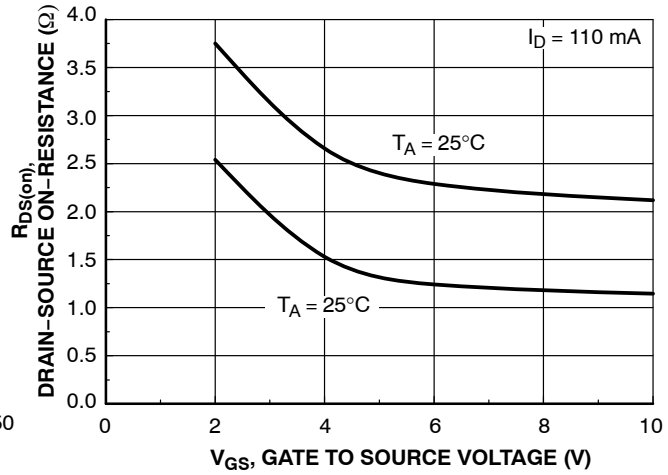


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

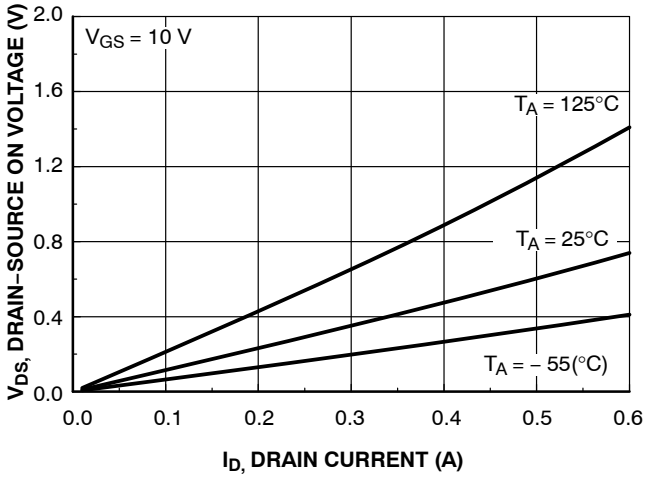


Figure 5. Drain−Source On Voltage with Temperature.

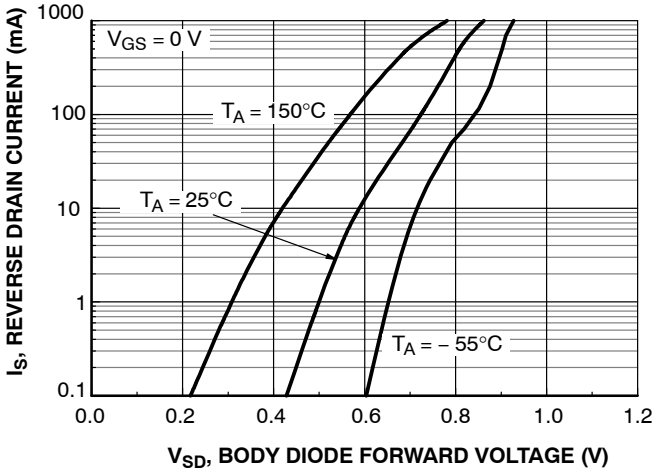


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

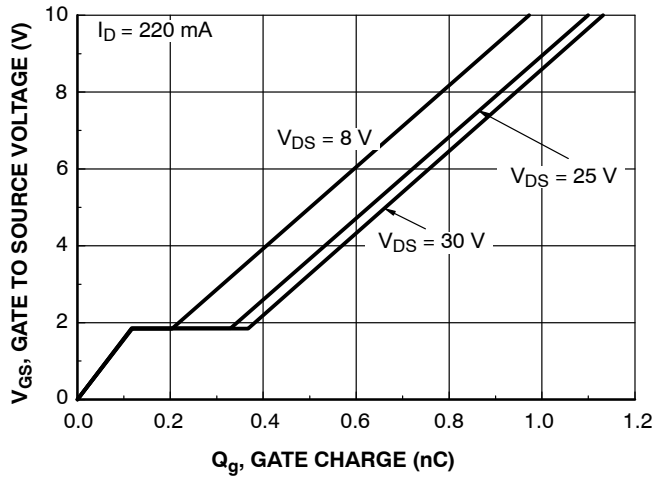


Figure 7. Gate Charge Characteristics

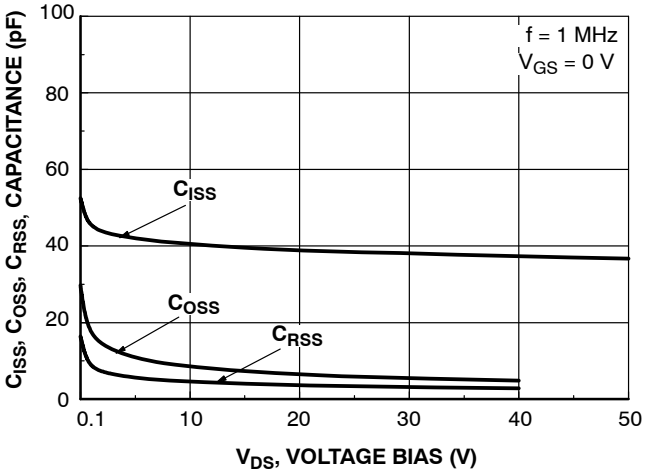


Figure 8. Capacitance Characteristics

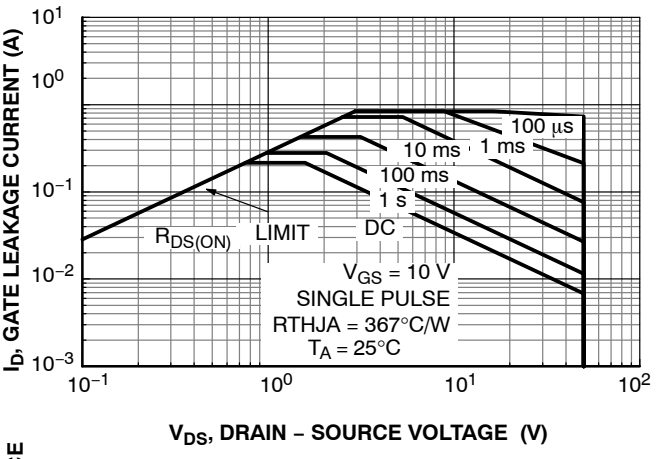


Figure 9. Maximum Safe Operating Area

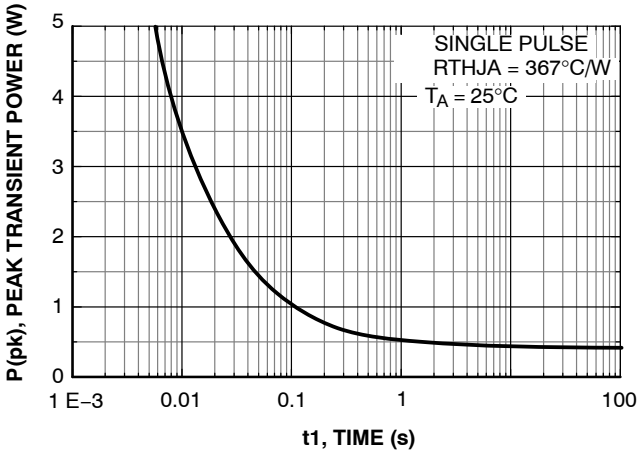


Figure 10. Single Pulse Maximum Power Dissipation

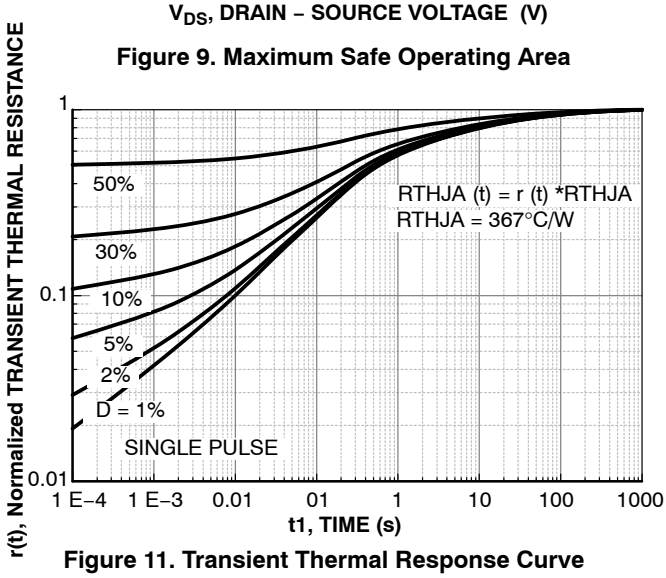
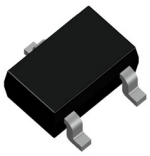
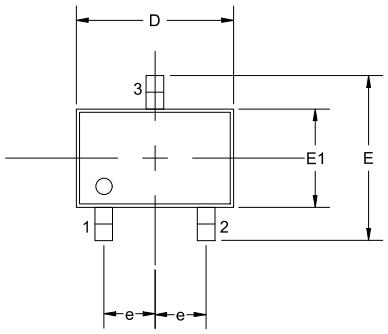


Figure 11. Transient Thermal Response Curve

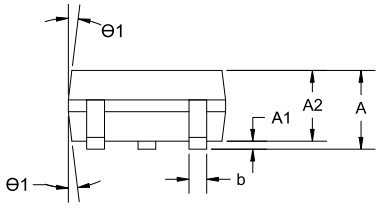


SC−70, 3 Lead, 1.25x2
CASE 419AB
ISSUE A

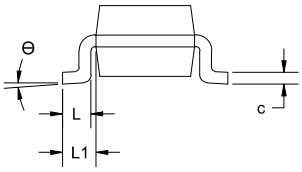
DATE 13 FEB 2023



TOP VIEW



SIDE VIEW

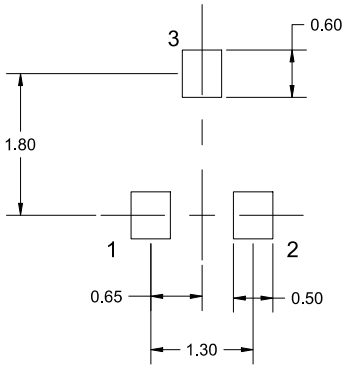


END VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. COMPLIES WITH JEDEC MO-203

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80		1.10
A1	0.00		0.10
A2	0.80	0.90	1.00
b	0.15		0.30
c	0.08		0.22
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
Θ	0°		8°
Θ1	4°		10°



SOLDERING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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