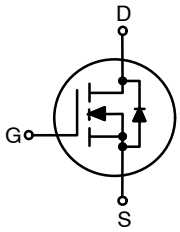
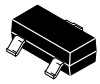
N-Channel Logic Level Enhancement Mode Field Effect Transistor

BSS123L



N−Channel



SOT−23−3
CASE 318−08

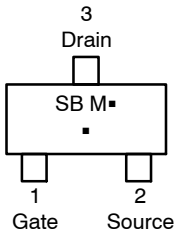
Description

This N−channel enhancement mode field effect transistor is produced using high cell density, trench MOSFET technology. This product minimizes on−state resistance while providing rugged, reliable and fast switching performance. This product is particularly suited for low−voltage, low−current applications such as small servo motor control, power MOSFET gate drivers, logic level transistor, high speed line drivers, power management/power supply and switching applications.

Features

- 0.17 A, 100 V
  - $R_{DS(on)}$ = 6 Ω @ V_{GS} = 10 V
  - $R_{DS(on)}$ = 10 Ω @ V_{GS} = 4.5 V
- High Density Cell Design for Low $R_{DS(ON)}$
- Rugged and Reliable
- Compact Industry Standard SOT−23 Surface Mount Package
- Very Low Capacitance
- Fast Switching Speed
- This Device is Pb−Free and Halogen Free

MARKING DIAGRAM



SB = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
BSS123L	SOT−23−3 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain–Source Voltage	100	V
V_{GSS}	Gate–Source Voltage	±20	V
I_D	Maximum Drain Current – Continuous	0.17	A
	Maximum Drain Current – Pulsed	0.68	
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16” from Case for 10 s	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
PD	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.8	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 1)	380	°C/W

ESD RATING (Note 2)

Symbol	Parameter	Value	Unit
HBM	Human Body Model per ANSI/ESDA/JEDEC JS–001–2012	50	V
CDM	Charged Device Model per JEDEC C101C	>2000	V

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	100	103	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	100	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 100 V, V_{GS} = 0 V	–	0.027	1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 125°C	–	0.159	60	
		V_{DS} = 20 V, V_{GS} = 0 V	–	0.07	10	nA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	0.036	50	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V, V_{DS} = 0 V	–	–0.019	–50	nA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.8	1.405	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	–2.82	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 0.17 A	–	2.98	6	Ω
		V_{GS} = 4.5 V, I_D = 0.17 A	–	3.17	10	
		V_{GS} = 10 V, I_D = 0.17 A, T_J = 125°C	–	5.63	12	
$I_{D(ON)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	0.680	0.735	–	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.17 A	0.08	2.13	–	S

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	21.5	–	pF
C_{oss}	Output Capacitance		–	3.52	–	
C_{rss}	Reverse Transfer Capacitance		–	1.67	–	
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz	–	7.18	–	Ω
SWITCHING CHARACTERISTICS (Note 3)						
$t_{d(on)}$	Turn–On Delay	V_{DD} = 30 V, I_D = 0.28 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	2.2	3.4	ns
t_r	Turn–On Rise Time		–	1.7	18	
$t_{d(off)}$	Turn–Off Delay		–	5.9	31	
t_f	Turn–Off Fall Time		–	5.6	5	
Q_g	Total Gate Charge	V_{DS} = 30 V, I_D = 0.22 A, V_{GS} = 10 V	–	0.793	2.5	nC
Q_{gs}	Gate–Source Charge		–	0.092	–	
Q_{gd}	Gate–Drain Charge		–	0.171	–	
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 440 mA (Note 1)	–	0.867	1.3	V
T_{rr}	Diode Reverse Recovery Time	I_F = 0.2 A, d_{if}/d_t = 100 A/μs	–	11.9	–	ns
Q_{rr}	Diode Reverse Recovery Charge		–	1.3	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 380°C/W when mounted on a minimum pad.

2. ESD values are in typical, no over–voltage rating is implied, ESD CDM zap voltage is 2000 V maximum.
3. Pulse test: pulse width ≤ 300 ms, duty cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

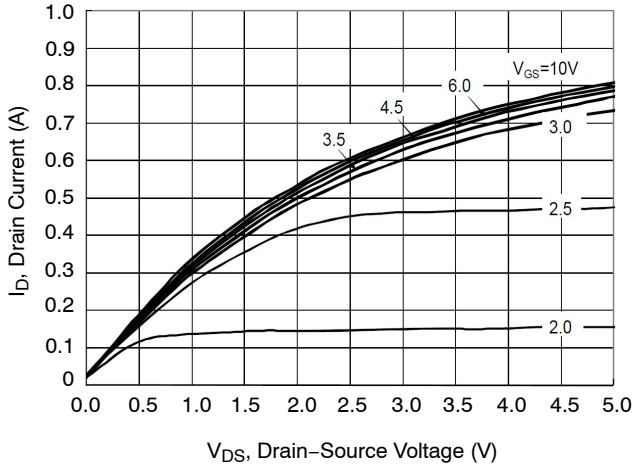


Figure 1. On−Region Characteristics

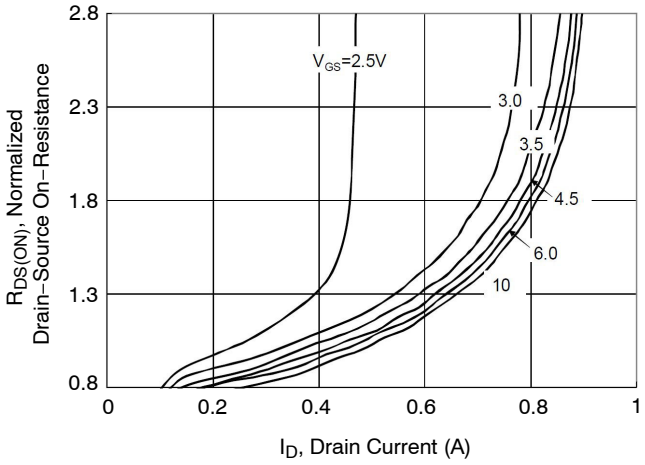


Figure 2. On−Resistance Variation with Gate Voltage and Drain Current

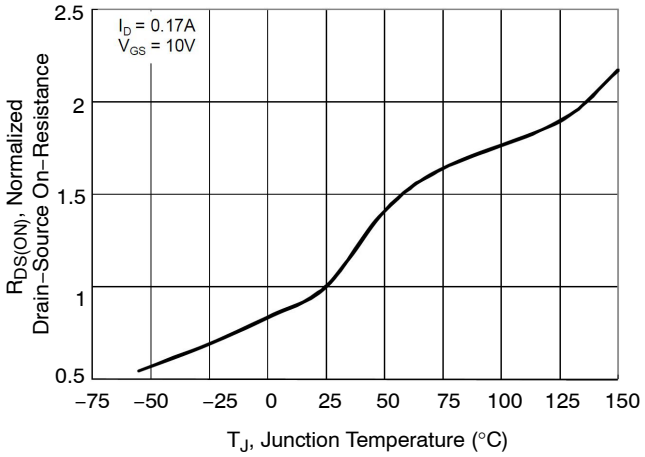


Figure 3. On−Resistance Variation with Temperature

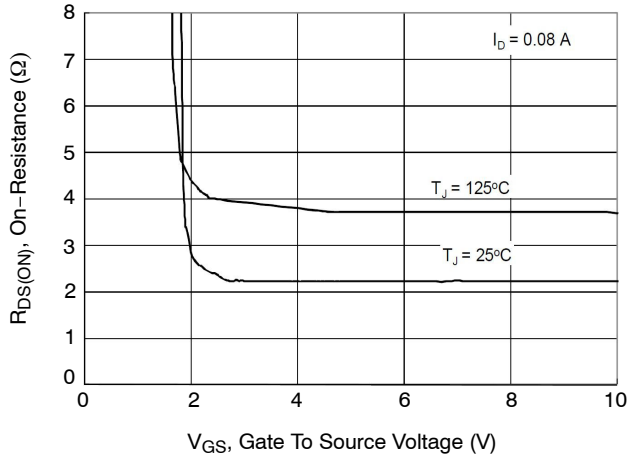


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

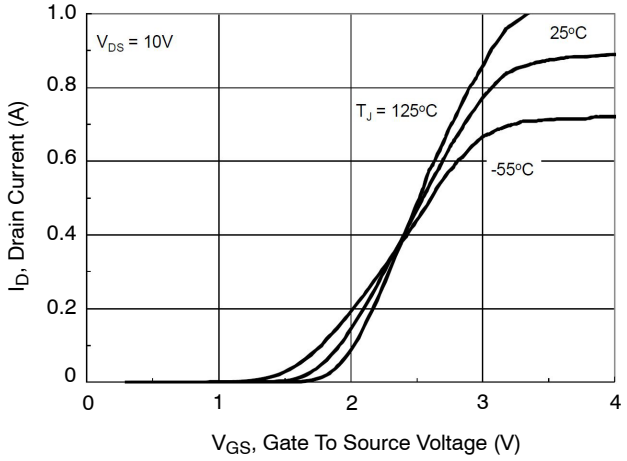


Figure 5. Transfer Characteristics

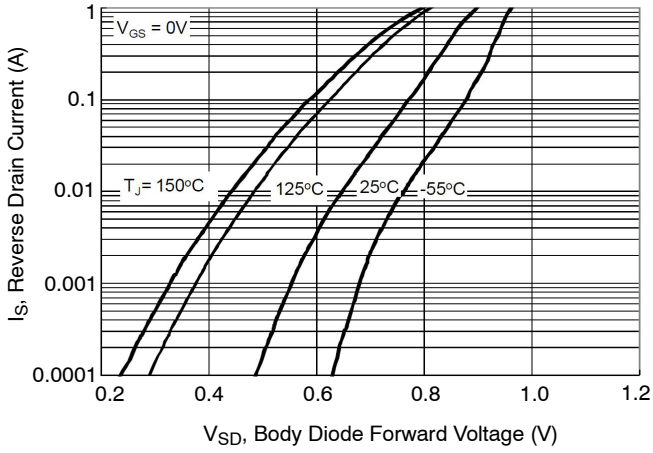


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

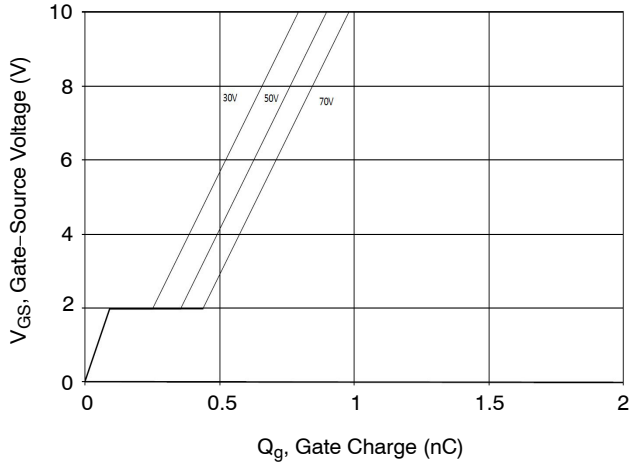


Figure 7. Gate Charge Characteristics

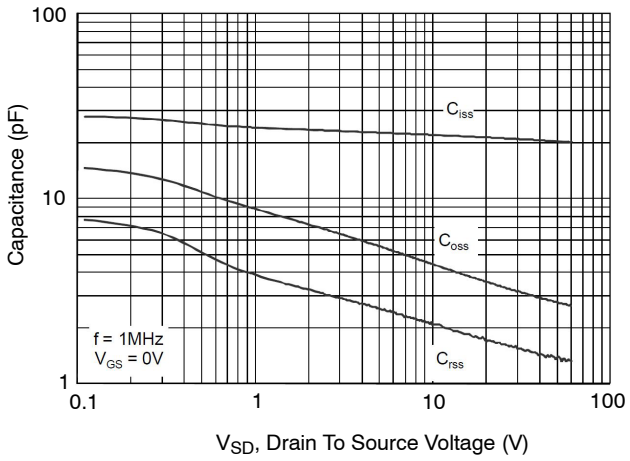


Figure 8. Capacitance Characteristics

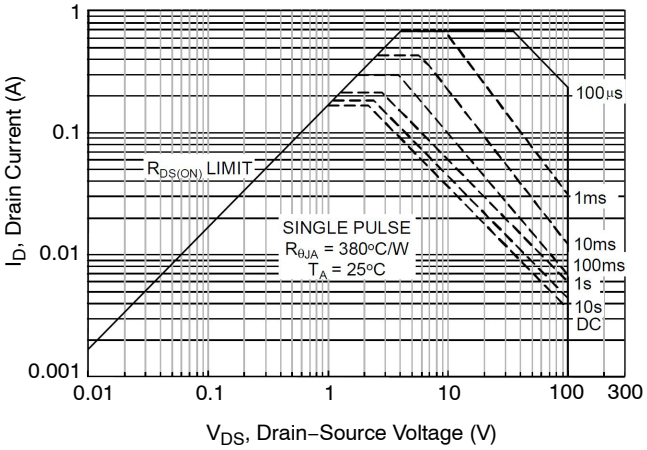


Figure 9. Maximum Safe Operating Area

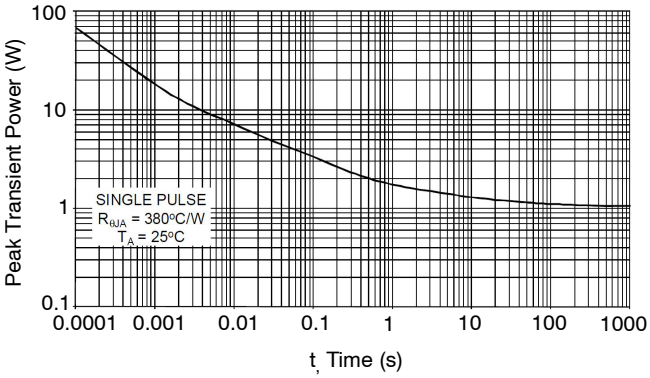


Figure 10. Single Pulse Maximum Power Dissipation

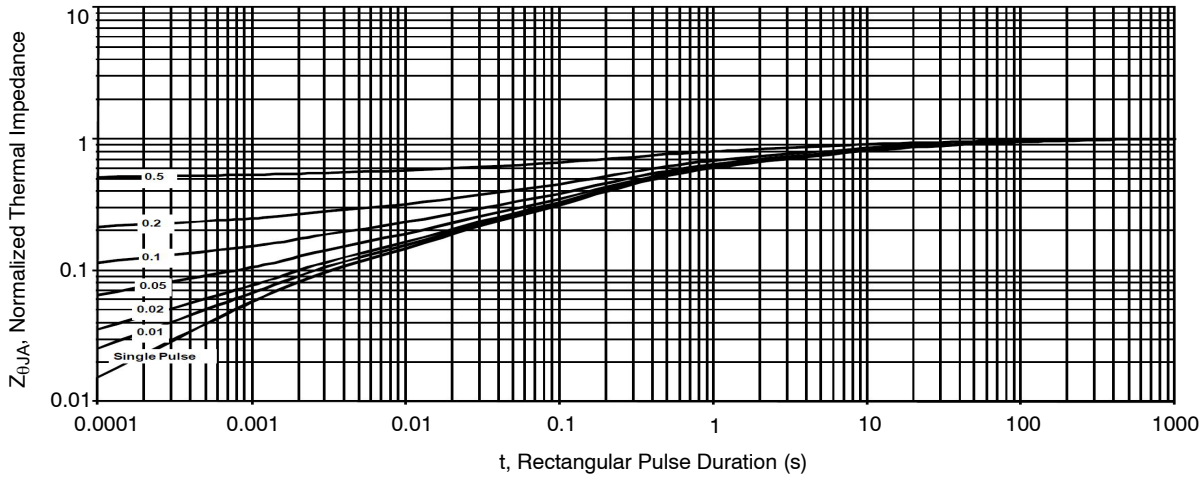


Figure 11. Transient Thermal Response Curve

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