ADP3212A, NCP3218A

7-Bit, Programmable, 3-Phase, Mobile CPU Synchronous Buck Controller

The APD3212A/NCP3218A is a highly efficient, multi−phase, synchronous buck switching regulator controller. With its integrated drivers, the APD3212A/NCP3218A is optimized for converting the notebook battery voltage into the core supply voltage required by high performance Intel processors. An internal 7−bit DAC is used to read a VID code directly from the processor and to set the CPU core voltage to a value within the range of 0.3 V to 1.5 V. The APD3212A/NCP3218A is programmable for 1−, 2−, or 3−phase operation. The output signals ensure interleaved 2− or 3−phase operation.

The APD3212A/NCP3218A uses a multimode architecture run at a programmable switching frequency and optimized for efficiency depending on the output current requirement. The APD3212A/NCP3218A switches between single− and multi−phase operation to maximize efficiency with all load conditions. The chip includes a programmable load line slope function to adjust the output voltage as a function of the load current so that the core voltage is always optimally positioned for a load transient. The APD3212A/NCP3218A also provides accurate and reliable short−circuit protection, adjustable current limiting, and a delayed power−good output. The IC supports On−The−Fly (OTF) output voltage changes requested by the CPU.

The APD3212A/NCP3218A are specified over the extended commercial temperature range of −40°C to 100°C. The ADP3212A is available in a 48−lead QFN 7x7mm 0.5mm pitch package. The NCP3218A is available in a 48−lead QFN 6x6mm 0.4mm pitch package. Except for the packages, the APD3212A/NCP3218A are identical. APD3212A/NCP3218A are Halogen−Free, Pb−Free and RoHS compliant.

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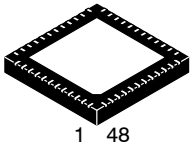
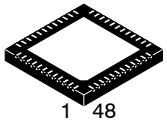


QFN48
CASE 485AJ



QFN48
CASE 485BA

MARKING DIAGRAM

xxx = Specific Device Code (ADP3212A or NCP3218A)
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

Features

- Single−Chip Solution
- Fully Compatible with the Intel® IMVP−6.5™ Specifications
- Selectable 1−, 2−, or 3−Phase Operation with Up to 1 MHz per Phase Switching Frequency
- Phase 1 and Phase 2 Integrated MOSFET Drivers
- Input Voltage Range of 3.3 V to 22 V
- Guaranteed ±8 mV Worst−Case Differentially Sensed Core Voltage Error Over Temperature
- Automatic Power−Saving Mode Maximizes Efficiency with Light Load During Deeper Sleep Operation
- Active Current Balancing Between Output Phases
- Independent Current Limit and Load Line Setting Inputs for Additional Design Flexibility
- Built−In Power−Good Blanking Supports Voltage Identification (VID) On−The−Fly (OTF) Transients
- 7−Bit, Digitally Programmable DAC with 0.3 V to 1.5 V Output
- Short−Circuit Protection with Programmable Latchoff Delay
- Clock Enable Output Delays the CPU Clock Until the Core
  Voltage is Stable
- Output Power or Current Monitor Options
- 48−Lead QFN 7x7mm (ADP3212A), 48−Lead QFN 6x6mm (NCP3218A)
- These are Pb−Free Devices
- Fully RoHS Compliant

Applications

- Notebook Power Supplies for Next−Generation Intel Processors

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 33 of this data sheet.

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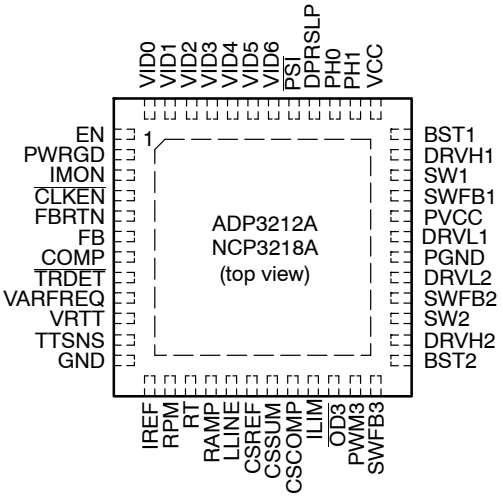
PIN ASSIGNMENT



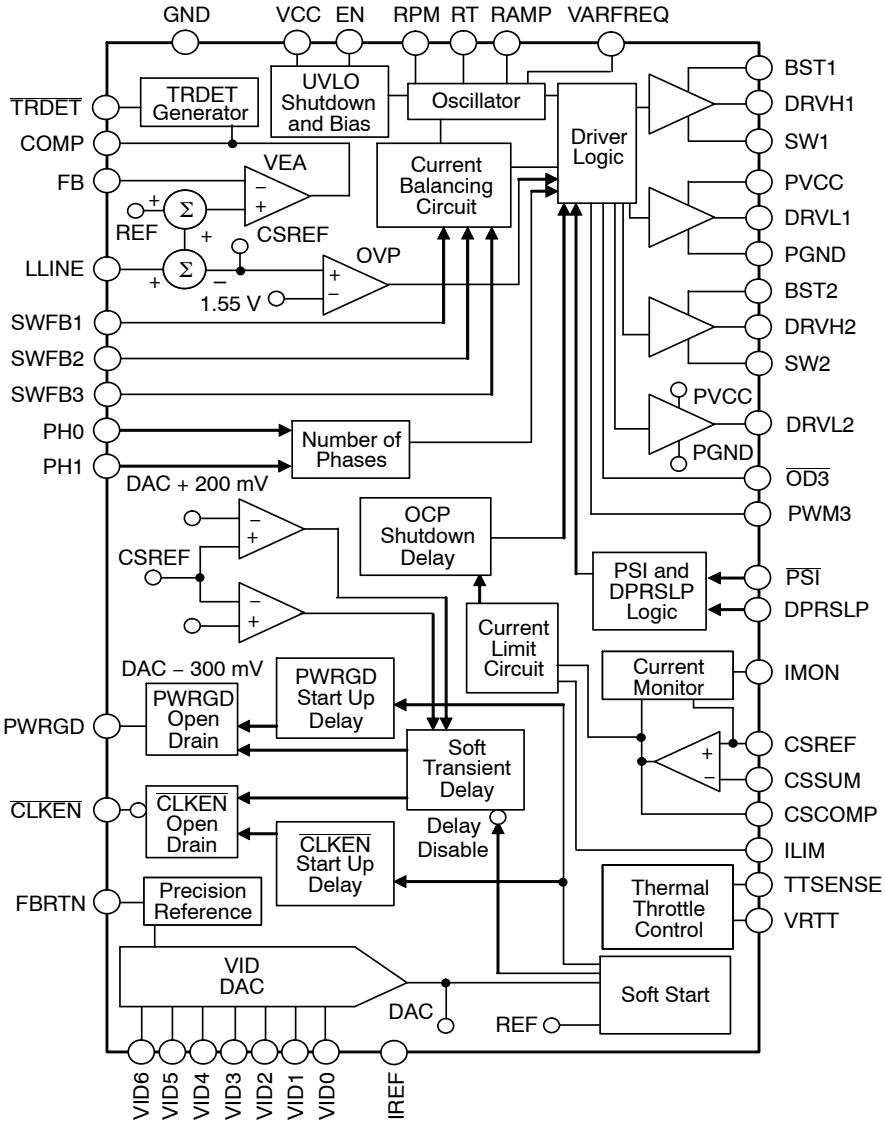


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{CC}, PV_{CC1}, PV_{CC2}	−0.3 to +6.0	V
FBRTN, PGND1, PGND2	−0.3 to +0.3	V
BST1, BST2, DRVH1, DRVH2 DC t < 200 ns	 −0.3 to +28 −0.3 to +33	V
BST1 to PV_{CC}, BST2 to PV_{CC} DC t < 200 ns	 −0.3 to +22 −0.3 to +28	V
BST1 to SW1, BST2 to SW2	−0.3 to +6.0	V
SW1, SW2 DC t < 200 ns	 −1.0 to +22 −6.0 to +28	V
DRVH1 to SW1, DRVH2 to SW2	−0.3 to +6.0	V
DRVL1 to PGND1, DRVL2 to PGND2 DC t < 200 ns	 −0.3 to +6.0 −5.0 to +6.0	V
RAMP (in Shutdown)	−0.3 to +22	V
All Other Inputs and Outputs	−0.3 to +6.0	V
Storage Temperature Range	−65 to +150	°C
Operating Ambient Temperature Range	−40 to +100	°C
Operating Junction Temperature	125	°C
Thermal Impedance (θ_{JA}) 2−Layer Board	30.5	°C/W
Lead Temperature Soldering (10 sec) Infrared (15 sec)	 300 260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	EN	Enable Input. Driving this pin low shuts down the chip, disables the driver outputs, pulls PWRGD and VRTT low, and pulls $\overline{\text{CLKEN}}$ high.
2	PWRGD	Power−Good Output. Open−drain output. A low logic state means that the output voltage is outside of the VID DAC defined range.
3	IMON	Current Monitor Output. This pin sources a current proportional to the output load current. A resistor to FBRTN sets the current monitor gain.
4	$\overline{\text{CLKEN}}$	Clock Enable Output. Open−drain output. A low logic state enables the CPU internal PLL clock to lock to the external clock.
5	FBRTN	Feedback Return Input/Output. This pin remotely senses the CPU core voltage. It is also used as the ground return for the VID DAC and the voltage error amplifier blocks.
6	FB	Voltage Error Amplifier Feedback Input. The inverting input of the voltage error amplifier.
7	COMP	Voltage Error Amplifier Output and Frequency Compensation Point.
8	$\overline{\text{TRDET}}$	Transient Detect Output. This pin is pulled low when a load release transient is detected. During repetitive load transients at high frequencies, this circuit optimally positions the maximum and minimum output voltage into a specified loadline window.
9	VARFREQ	Variable Frequency Enable Input. A high logic state enables the PWM clock frequency to vary with VID code.
10	VRTT	Voltage Regulator Thermal Throttling Output. Logic high state indicates that the voltage regulator temperature at the remote sensing point exceeded a set alarm threshold level.

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
11	TTSNS	Thermal Throttling Sense and Crowbar Disable Input. A resistor divider where the upper resistor is connected to VCC, the lower resistor (NTC thermistor) is connected to GND, and the center point is connected to this pin and acts as a temperature sensor half bridge. Connecting TTSNS to GND disables the thermal throttling function and disables the crowbar, or Overvoltage Protection (OVP), feature of the chip.
12	GND	Analog and Digital Signal Ground.
13	IREF	This pin sets the internal bias currents. A 80 kΩ resistor is connected from this pin to ground.
14	RPM	RPM Mode Timing Control Input. A resistor between this pin to ground sets the RPM mode turn−on threshold voltage.
15	RT	Multi−phase Frequency Setting Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device when operating in multi−phase PWM mode threshold of the converter.
16	RAMP	PWM Ramp Slope Setting Input. An external resistor from the converter input voltage node to this pin sets the slope of the internal PWM stabilizing ramp used for phase−current balancing.
17	LLINE	Output Load Line Programming Input. The center point of a resistor divider between CSREF and CSCOMP is connected to this pin to set the load line slope.
18	CSREF	Current Sense Reference Input. This pin must be connected to the common point of the output inductors. The node is shorted to GND through an internal switch when the chip is disabled to provide soft stop transient control of the converter output voltage.
19	CSSUM	Current Sense Summing Input. External resistors from each switch node to this pin sum the inductor currents to provide total current information.
20	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determine the gain of the current−sense amplifier and the positioning loop response time.
21	ILIM	Current Limit Setpoint. An external resistor from this pin to CSCOMP sets the current limit threshold of the converter.
22	$\overline{OD3}$	Multi−phase Output Disable Logic Output. This pin is actively pulled low when the APD3212A/NCP3218A enters single−phase mode or during shutdown. Connect this pin to the SD inputs of the Phase−3 MOSFET drivers.
23	PWM3	Logic−Level PWM Output for phase 3. Connect to the input of an external MOSFET driver such as the ADP3611.
24	SWFB3	Current Balance Input for phase 3. Input for measuring the current level in phase 3. SWFB3 should be left open for 1 or 2 phase configuration.
25	BST2	High−Side Bootstrap Supply for Phase 2. A capacitor from this pin to SW2 holds the bootstrapped voltage while the high−side MOSFET is on.
26	DRVH2	High−Side Gate Drive Output for Phase 2.
27	SW2	Current Return for High−Side Gate Drive for phase 2.
28	SWFB2	Current Balance Input for phase 2. Input for measuring the current level in phase 2. SWFB2 should be left open for 1 phase configuration.
29	DRVL2	Low−Side Gate Drive Output for Phase 2.
30	PGND	Low−Side Driver Power Ground
31	DRVL1	Low−Side Gate Drive Output for Phase 1.
32	PVCC	Power Supply Input/Output of Low−Side Gate Drivers.
33	SWFB1	Current Balance Input for phase 1. Input for measuring the current level in phase 1.
34	SW1	Current Return For High−Side Gate Drive for phase 1.
35	DRVH1	High−Side Gate Drive Output for Phase 1.
36	BST1	High−Side Bootstrap Supply for Phase 1. A capacitor from this pin to SW1 holds the bootstrapped voltage while the high−side MOSFET is on.
37	VCC	Power Supply Input/Output of the Controller.
38	PH1	Phase Number Configuration Input. Connect to VCC for 3 phase configuration.
39	PH0	Phase Number Configuration Input. Connect to GND for 1 phase configuration. Connect to VCC for multi−phase configuration.
40	DPRSLP	Deeper Sleep Control Input.
41	$\overline{PSI}$	Power State Indicator Input. Pulling this pin to GND forces the APD3212A/NCP3218A to operate in single−phase mode.
42 to 48	VID6 to VID0	Voltage Identification DAC Inputs. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.3 V to 1.5 V (see Table 3).

ELECTRICAL CHARACTERISTICS

V_{CC} = PV_{CC} = 5.0 V, FBRTN = PGND = GND = 0 V, H = 5.0 V, L = 0 V, EN = VARFREQ = H, DPRSLP = L, $\overline{PSI}$ = 1.05 V, V_{VID} = V_{DAC} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sink current) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOLTAGE CONTROL − VOLTAGE ERROR AMPLIFIER (VEAMP)						
FB, LLINE Voltage Range (Note 2)	V_{FB}, V_{LLINE}	Relative to CSREF = VDAC	−200		+200	mV
FB, LLINE Offset Voltage (Note 2)	V_{OSVEA}	Relative to CSREF = VDAC	−0.5		+0.5	mV
LLINE Bias Current	I_{LLINE}		−100		+100	nA
FB Bias Current	I_{FB}		−1.0		+1.0	μA
LLINE Positioning Accuracy	V_{FB} − V_{VID}	Measured on FB relative to V_{VID}, LLINE forced 80 mV below CSREF	−77.5	−80	−82.5	mV
COMP Voltage Range (Note 2)	V_{COMP}		0.85		4.0	V
COMP Current	I_{COMP}	COMP = 2.0 V, CSREF = VDAC FB forced 200 mV below CSREF FB forced 200 mV above CSREF		−0.75 6.0		mA
COMP Slew Rate	SR_{COMP}	C_{COMP} = 10 pF, CSREF = VDAC, Open loop configuration FB forced 200 mV below CSREF FB forced 200 mV above CSREF		15 −20		V/μs
Gain Bandwidth (Note 2)	GBW	Non−inverting unit gain configuration, R_{FB} = 1 kΩ		20		MHz
VID DAC VOLTAGE REFERENCE						
VDAC Voltage Range (Note 2)		See VID table	0		1.5	V
VDAC Accuracy	V_{FB} − V_{VID}	Measured on FB (includes offset), relative to V_{VID} V_{VID} = 0.5000 V to 1.5000 V, T = −10°C to 100°C V_{VID} = 0.5000 V to 1.5000 V, T = −40°C to 100°C V_{VID} = 0.3000 V to 0.4875 V, T = −10°C to 100°C V_{VID} = 0.3000 V to 0.4875 V, T = −40°C to 100°C	 −7.5 −9.0 −9.0 −10		 +7.5 +9.0 +9.0 +10	mV
VDAC Differential Non−linearity (Note 2)			−1.0		+1.0	LSB
VDAC Line Regulation	ΔV_{FB}	VCC = 4.75 V to 5.25 V		0.001		%
VDAC Boot Voltage	V_{BOOTFB}	Measured during boot delay period		1.100		V
Soft−Start Delay (Note 2)	t_{DSS}	Measured from EN pos edge to FB = 50 mV		200		μs
Soft−Start Time	t_{SS}	Measured from FB = 50 mV to FB settles to 1.1 V within 5%		1.4		ms
Boot Delay	t_{BOOT}	Measured from FB settling to 1.1 V within 5% to $\overline{CLKEN}$ neg edge		60		μs
VDAC Slew Rate (Note 2)		Soft−Start Non−LSB VID step, DPRSLP = H, Slow C4 Entry/Exit Non−LSB VID step, DPRSLP = L, Fast C4 Exit LSB VID step, DVID transition GPU Mode, Non−LSB VID step, Fast Entry/Exit		0.0625 0.25 1.0 0.4 1.0		LSB/μs
FBRTN Current	I_{FBRTN}			−90	−200	μA
VOLTAGE MONITORING and PROTECTION − POWER GOOD						
CSREF Undervoltage Threshold	$V_{UVCSREF}$	Relative to nominal VDAC voltage	−240	−300	−360	mV
CSREF Overvoltage Threshold	$V_{OVCSREF}$	Relative to nominal VDAC voltage, T = −10°C to 100°C T = −40°C to 100°C	 150 140	 200 200	 250 250	mV

1. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Based on bench characterization data.
4. Timing is referenced to the 90% and 10% points, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

V_{CC} = PV_{CC} = 5.0 V, FBRTN = PGND = GND = 0 V, H = 5.0 V, L = 0 V, EN = VARFREQ = H, DPRSLP = L, $\overline{PSI}$ = 1.05 V, V_{VID} = V_{DAC} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sink current) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VOLTAGE MONITORING and PROTECTION − POWER GOOD						
CSREF Crowbar Voltage Threshold	$V_{CBCSREF}$	Relative to FBRTN	1.5	1.55	1.6	V
CSREF Reverse Voltage Threshold	$V_{RVCSREF}$	Relative to FBRTN, latchoff mode CSREF is falling CSREF is rising	 −350	 −300 −75	 −10	mV
PWRGD Low Voltage	V_{PWRGD}	$I_{PWRGD(SINK)}$ = 4 mA		85	250	mV
PWRGD High, Leakage Current	I_{PWRGD}	V_{PWRDG} = 5.0 V			1.0	μA
PWRGD Startup Delay	$T_{SSPWRGD}$	Measured from $\overline{CLKEN}$ neg edge to PWRGD pos edge		9.0		ms
PWRGD Latchoff Delay	$T_{LOFFPWRGD}$	Measured from Out−off−Good−Window event to Latchoff (switching stops)		9.0		μs
PWRGD Propagation Delay (Note 3)	$T_{PDPWRGD}$	Measured from Out−off−Good−Window event to PWRGD neg edge		200		ns
Crowbar Latchoff Delay (Note 2)	T_{LOFFCB}	Measured from Crowbar event to latchoff (switching stops)		200		ns
PWRGD Masking Time		Triggered by any VID change or OCP event		100		μs
CSREF Soft−Stop Resistance		EN = L or latchoff condition		70		Ω
CURRENT CONTROL − CURRENT−SENSE AMPLIFIER (CSAMP)						
CSSUM, CSREF Common−Mode Range (Note 2)		Voltage range of interest	0		2.0	V
CSSUM, CSREF Offset Voltage	V_{OSCSA}	CSREF − CSSUM, T_A = 25°C T_A = −10°C to 85°C T_A = −40°C to 85°C	−0.5 −1.7 −1.9		+0.5 +1.7 +1.9	mV
CSSUM Bias Current	I_{BCSSUM}		−50		+50	nA
CSREF Bias Current	I_{BCSREF}		−2.0		+2.0	μA
CSCOMP Voltage Range (Note 2)		Voltage range of interest	0.05		2.0	V
CSCOMP Current	$I_{CSCOMPsource}$	CSSUM forced 200 mV below CSREF		−750		μA
	$I_{CSCOMPsink}$	CSSUM forced 200 mV above CSREF		1.0		mA
CSCOMP Slew Rate (Note 2)		C_{CSCOMP} = 10 pF, CSREF = VDAC, Open loop configuration CSSUM forced 200 mV below CSREF CSSUM forced 200 mV above CSREF		 20 −20		V/μs
Gain Bandwidth (Note 2)	GBW_{CSA}	Non−inverting unit gain configuration R_{FB} = 1 kΩ		20		MHz
CURRENT MONITORING and PROTECTION CURRENT REFERENCE						
I_{REF} Voltage	V_{REF}	R_{REF} = 80 kΩ to set I_{REF} = 20 μA	1.55	1.6	1.65	V
CURRENT LIMITER (OCP)						
Current Limit (OCP) Threshold	V_{LIMTH}	Measured from CSCOMP to CSREF, R_{LIM} = 1.5 kΩ, 3−ph configuration, $\overline{PSI}$ = H 3−ph configuration, $\overline{PSI}$ = L 2−ph configuration, $\overline{PSI}$ = H 2−ph configuration, $\overline{PSI}$ = L 1−ph configuration	 −80 −22 −80 −35 −75	 −90 −30 −90 −45 −90	 −100 −38 −100 −55 −105	mV
Current Limit Latchoff Delay		Measured from OCP event to PWRGD de−assertion		150		μs

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Parameter	Symbol	Conditions	Min	Typ	Max	Units
CURRENT MONITOR						
Current Gain Accuracy	I_{MON}/I_{LIM}	Measured from I_{LIM} to I_{MON} I_{LIM} = −20 μA I_{LIM} = −10 μA I_{LIM} = −5 μA	 3.7 3.6 3.5	 4.0 4.0 4.0	 4.3 4.4 4.5	–
I_{MON} Clamp Voltage	V_{MAXMON}	Relative to FBRTN, ILIMP = −30 μA	1.0		1.16	V
PULSE WIDTH MODULATOR – CLOCK OSCILLATOR						
RT Voltage	V_{RT}	VARFREQ = high, R_T = 125 kΩ, V_{VID} = 1.5000 V VARFREQ = low See also $V_{RT}(V_{VID})$ formula	 1.125 0.9	 1.25 1.0	 1.375 1.1	V
PWM Clock Frequency Range (Note 2)	f_{CLK}	Operation of interest	0.3		3.0	MHz
PWM Clock Frequency	f_{CLK}	T_A = +25°C, V_{VID} = 1.2000 V R_T = 72 kΩ R_T = 120 kΩ R_T = 180 kΩ	 900 700 300	 1200 800 400	 1500 900 500	kHz
RAMP GENERATOR						
RAMP Voltage	V_{RAMP}	EN = high, I_{RAMP} = 60 μA EN = low	0.9	1.0 V_{IN}	1.1	V
RAMP Current Range (Note 2)	I_{RAMP}	EN = high EN = low, RAMP = 19 V	1.0 −1.0		100 +1.0	μA
PWM COMPARATOR						
PWM Comparator Offset (Note 2)	V_{OSRPM}	V_{RAMP} − V_{COMP}		±3.0		mV
RPM COMPARATOR						
RPM Current	I_{RPM}	V_{VID} = 1.2 V, R_T = 215 kΩ See also $I_{RPM}(R_T)$ formula		−5.5		μA
RPM Comparator Offset (Note 2)	V_{OSRPM}	V_{COMP} − (1 + V_{RPMTH})		±3.0		mV
EPWM CLOCK SYNC						
Trigger Threshold (Note 2)		Relative to COMP sampled T_{CLK} time earlier 3−phase configuration 2−phase configuration 1−phase configuration	 	 350 400 450	 	mV
$\overline{TRDET}$						
Trigger Threshold (Note 2)		Relative to COMP sampled T_{CLK} time earlier 3−phase configuration 2−phase configuration 1−phase configuration	 	 −450 −500 −600	 	mV
$\overline{TRDET}$ Low Voltage (Note 2)	V_{LTRDET}	Logic low, $I_{\overline{TRDET}sink}$ = 4 mA		30	300	mV
$\overline{TRDET}$ Leakage Current	I_{HTRDET}	Logic high, $V_{\overline{TRDET}}$ = VCC			3.0	μA
SWITCH AMPLIFIER						
SW Common Mode Range (Note 2)	$V_{SW(X)CM}$	Operation of interest for current sensing	−600		+200	mV
SWFB Input Resistance	$R_{SW(X)}$	SW_X = 0 V, SWFB = 0 V	20	35	50	kΩ
ZERO CURRENT SWITCHING COMPARATOR						
SW ZCS Threshold	$V_{DCM(SW1)}$	DCM mode, DPRSLP = 3.3 V		−3.0		mV
Masked Off−Time	$t_{OFFMSKD}$	Measured from DRVH1 neg edge to DRVH1 pos edge at operation max frequency		600		ns

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Parameter	Symbol	Conditions	Min	Typ	Max	Units
SYSTEM I/O BUFFERS VID[6:0], DPRSLP, $\overline{PSI}$ INPUTS						
Input Voltage		Refers to driving signal level Logic low Logic high	 0.7		 0.3	V
Input Current		V = 0.2 V, VID[6:0], DPRSLP (active pulldown to GND) $\overline{PSI}$ (active pullup to VCC)		1.0 −2.0		μA
VID Delay Time (Note 2)		Any VID edge to FB change 10%	200			ns
VARFREQ						
Input Voltage		Refers to driving signal level Logic low Logic high	 4.0		 0.7	V
Input Current				1.0		μA
EN INPUT						
Input Voltage		Refers to driving signal level Logic low Logic high	 1.7		 0.5	V
Input Current		EN = L or EN = H (static) 0.8 V < EN < 1.6 V (during transition)		10 −70		nA μA
PH1, PH0 INPUTS						
Input Voltage		Refers to driving signal level Logic low Logic high	 2.0		 0.5	V
Input Current				1.0		μA
$\overline{CLKEN}$ OUTPUT						
Output Low Voltage		Logic low, I_{sink} = 4 mA		60	200	mV
Output High, Leakage Current		Logic high, V_{CLKEN} = VCC			0.1	μA
PWM3, $\overline{OD3}$ OUTPUTS						
Output Voltage		Logic low, I_{SINK} = 400 μA Logic high, I_{SOURCE} = −400 μA	 4.0	10 5.0	500	mV V
THERMAL MONITORING and PROTECTION						
TTSNS Voltage Range (Note 2)			0		5.0	V
TTSNS Threshold		VCC = 5.0 V, TTSNS is falling	2.45	2.5	2.55	V
TTSNS Hysteresis			50	95		mV
TTSNS Bias Current		TTSNS = 2.6 V	−2.0		2.0	μA
VRTT Output Voltage	V_{VRTT}	Logic low, $I_{VRTT(SINK)}$ = 400 μA Logic high, $I_{VRTT(SOURCE)}$ = −400 μA	 4.5	10 5.0	500	mV V
SUPPLY						
Supply Voltage Range	V_{CC}		4.5		5.5	V
Supply Current		EN = high EN = 0 V		7 10	10 50	mA μA
VCC OK Threshold	V_{CCOK}	VCC is rising		4.4	4.5	V
VCC UVLO Threshold	V_{CCUVLO}	VCC is falling	4.0	4.15		V
VCC Hysteresis (Note 2)				250		mV
HIGH−SIDE MOSFET DRIVER						
Pullup Resistance, Sourcing Current (Note 3)		BST = PVCC		1.25	3.3	Ω

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2. Guaranteed by design or bench characterization, not production tested.
3. Based on bench characterization data.
4. Timing is referenced to the 90% and 10% points, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

V_{CC} = PV_{CC} = 5.0 V, FBRTN = PGND = GND = 0 V, H = 5.0 V, L = 0 V, EN = VARFREQ = H, DPRSLP = L, $\overline{PSI}$ = 1.05 V, V_{VID} = V_{DAC} = 1.2000 V, T_A = −40°C to 100°C, unless otherwise noted. (Note 1) Current entering a pin (sink current) has a positive sign.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
HIGH−SIDE MOSFET DRIVER						
Pulldown Resistance, Sinking Current (Note 3)		BST = PVCC		0.8	2.0	Ω
Transition Times	tr_{DRVH} tf_{DRVH}	BST = PVCC, C_L = 3 nF, Figure 2 BST = PVCC, C_L = 3 nF, Figure 2		15 13	35 31	ns
Dead Delay Times	$tpdh_{DRVH}$	BST = PVCC, Figure 2 T = −10°C to 100°C T = −40°C to 100°C	 28	 32	 36 50	ns
BST Quiescent Current		EN = L (Shutdown) EN = H, no switching		1.0 200	10	μA
LOW−SIDE MOSFET DRIVER						
Pullup Resistance, Sourcing Current (Note 3)				0.88	2.8	Ω
Pulldown Resistance, Sinking Current (Note 3)				0.65	1.7	Ω
Transition Times	tr_{DRVL} tf_{DRVL}	C_L = 3 nF, Figure 2 C_L = 3 nF, Figure 2		15 14	35 35	ns
Propagation Delay Times	$tpdh_{DRVL}$	C_L = 3 nF, Figure 2 T = −10°C to 100°C T = −40°C to 100°C	 	 11 12	 30 40	ns
SW Transition Timeout	t_{TOSW}	DRVH = L, SW = 2.5 V T = −10°C to 100°C T = −40°C to 100°C	 85 85	 250 250	 300 450	ns
SW Off Threshold	V_{OFFSW}			1.6		V
PVCC Quiescent Current		EN = L (Shutdown) EN = H, no switching		1.0 170	10	μA
BOOTSTRAP RECTIFIER SWITCH						
On Resistance (Note 3)		EN = L or EN = H and DRVL = H	5.0	7.0	12	Ω

1. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
2. Guaranteed by design or bench characterization, not production tested.
3. Based on bench characterization data.
4. Timing is referenced to the 90% and 10% points, unless otherwise noted.

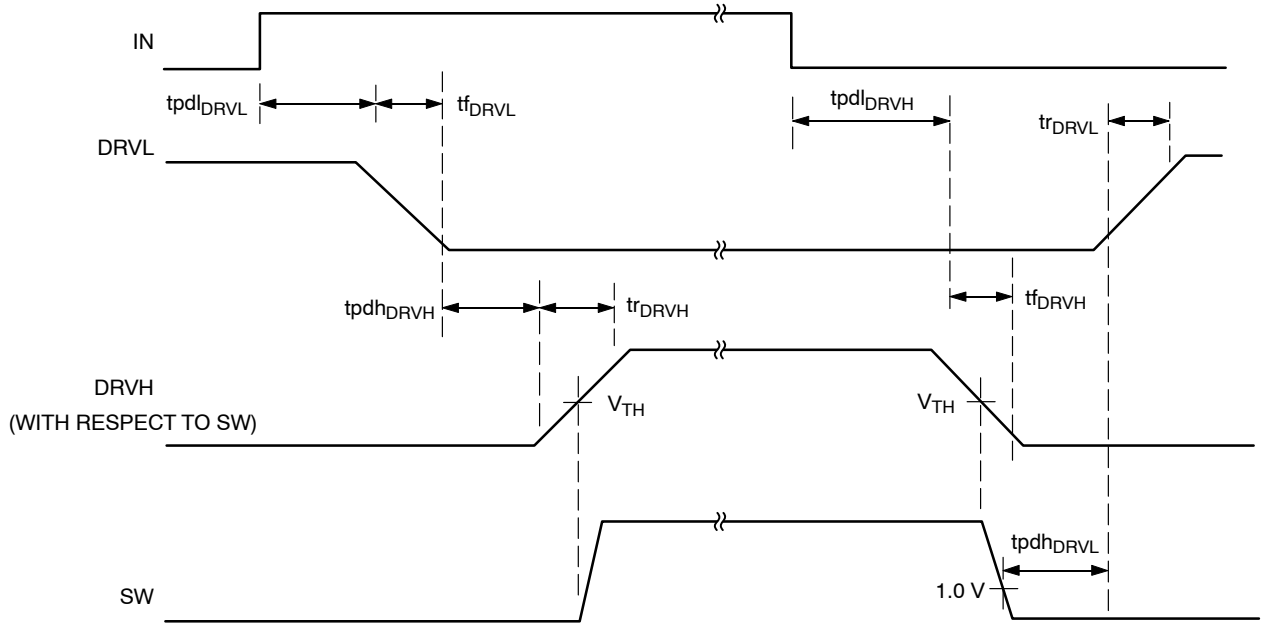


Figure 2. Timing Diagram (Note 4)

TEST CIRCUITS

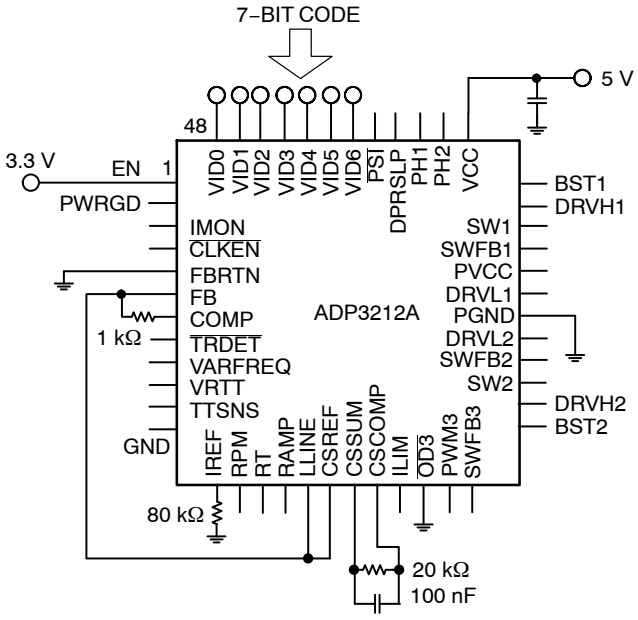


Figure 3. Closed−Loop Output Voltage Accuracy

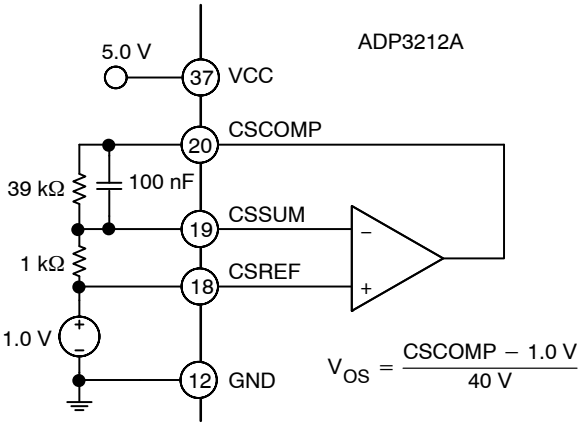


Figure 4. Current Sense Amplifier, V_{OS}

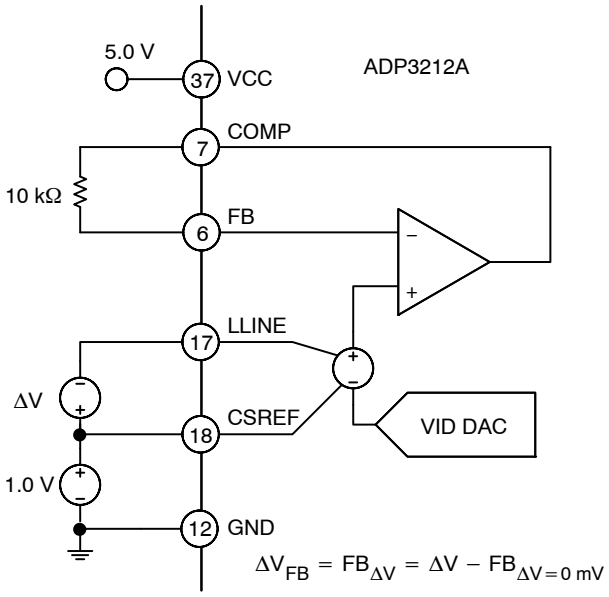


Figure 5. Positioning Accuracy

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

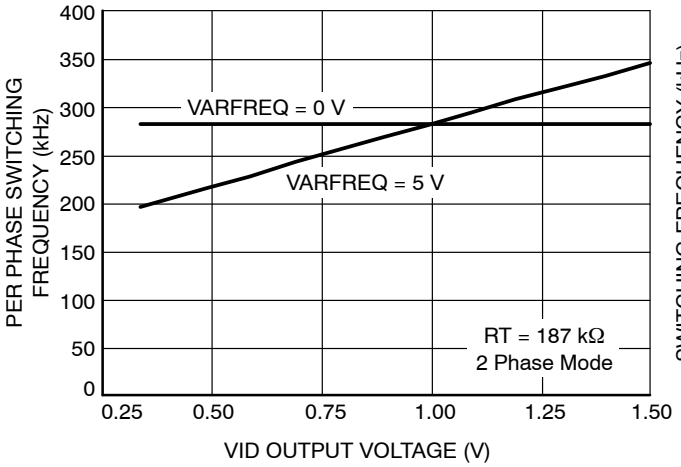


Figure 6. Switching Frequency vs. VID Output Voltage in PWM Mode

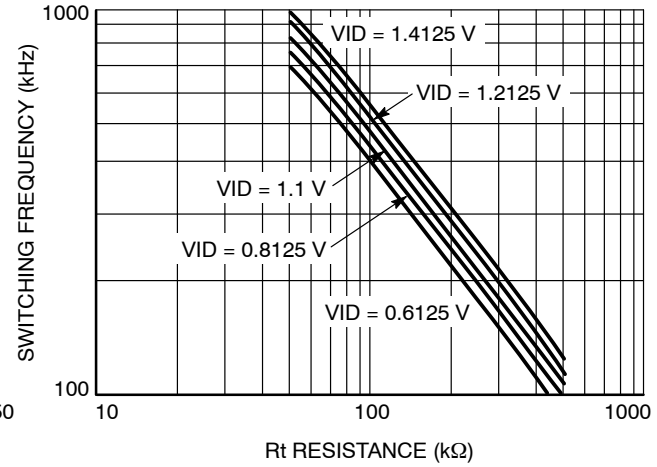


Figure 7. Per Phase Switching Frequency vs. RT Resistance

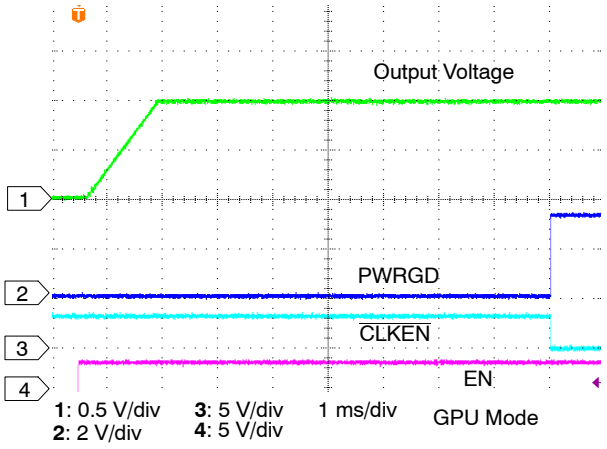


Figure 8. Startup in GPU Mode

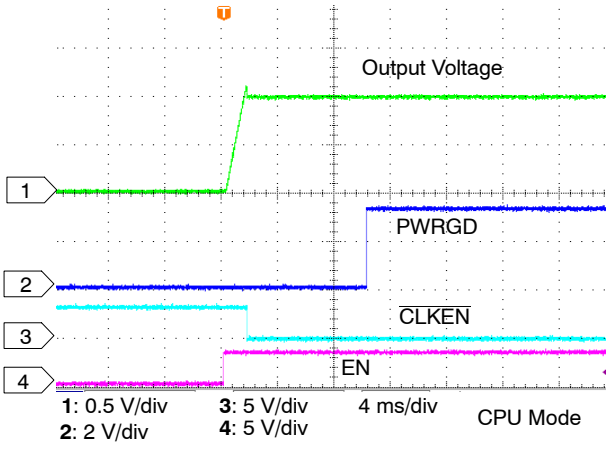


Figure 9. Startup in CPU Mode

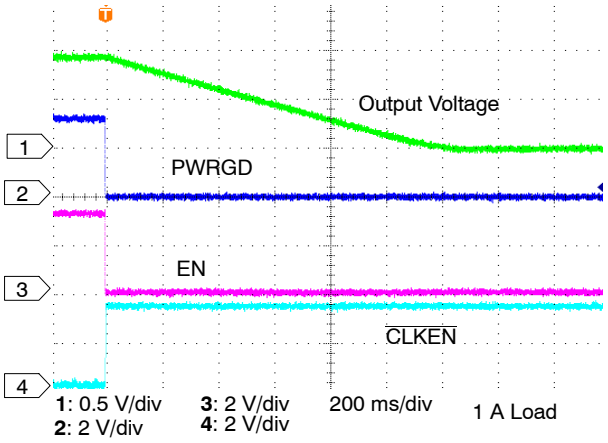


Figure 10. Shutdown

TYPICAL PERFORMANCE CHARACTERISTICS

V_{VID} = 1.5 V, T_A = 20°C to 100°C, unless otherwise noted.

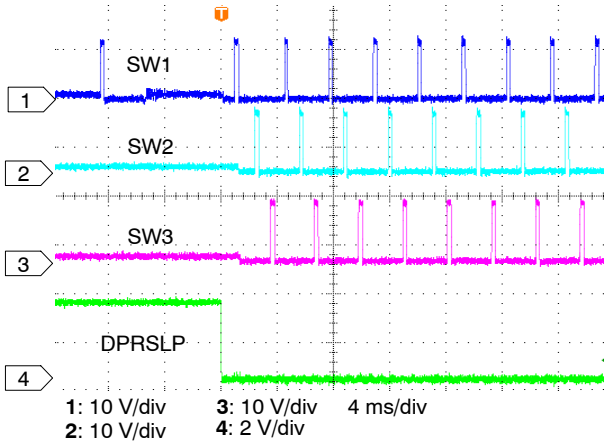


Figure 11. DPRSLP Transition with PSI = High

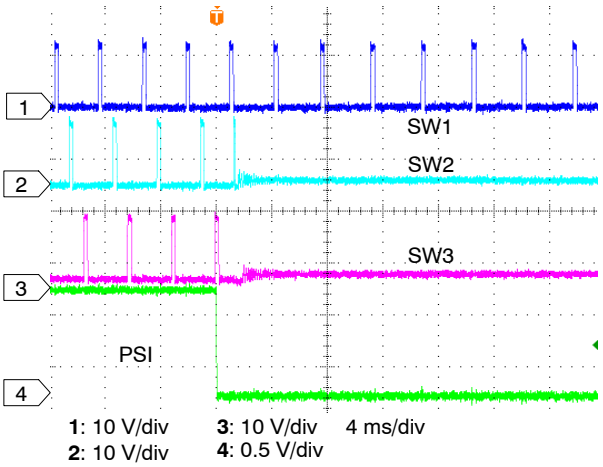


Figure 12. PSI Transition with DPRSLP = Low

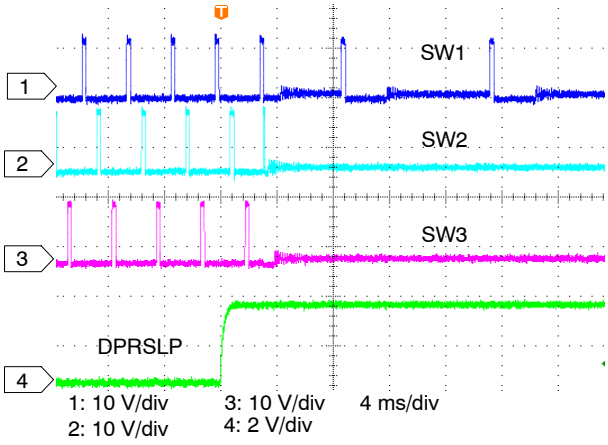


Figure 13. DPRSLP Transition with PSI = High

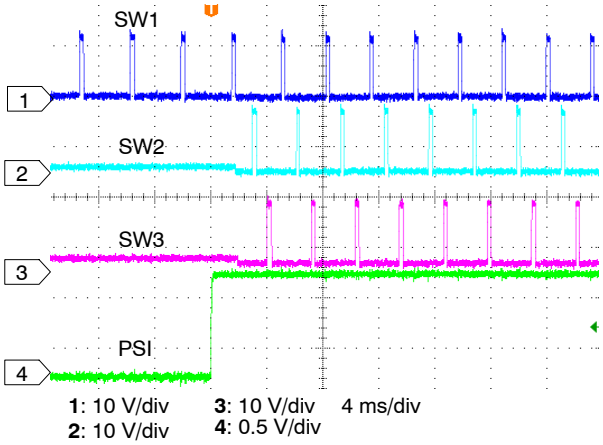


Figure 14. PSI Transition with DPRSLP = Low

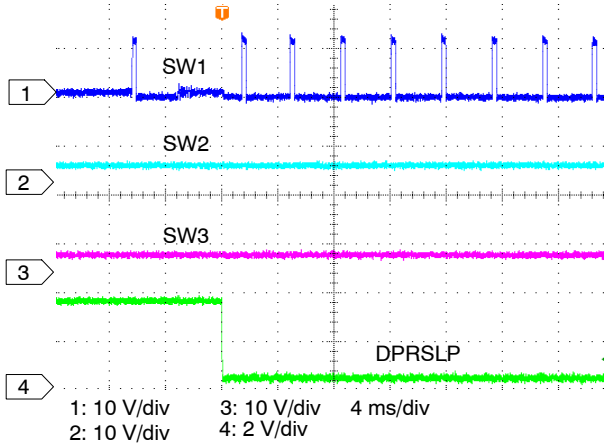


Figure 15. DPRSLP Transition with PSI = Low

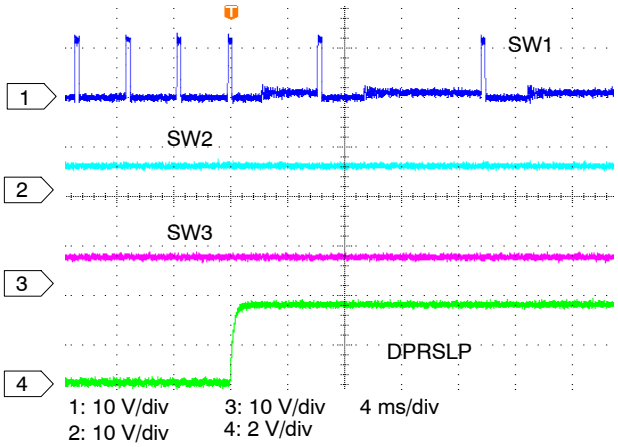


Figure 16. DPRSLP Transition with PSI = Low

Theory of Operation

The APD3212A/NCP3218A combines multi−mode Pulse−Width Modulated (PWM) control and Ramp−Pulse Modulated (RPM) control with multi−phase logic outputs for use in single−, dual−phase, or triple−phase synchronous buck CPU core supply power converters. The internal 7−bit VID DAC conforms to the Intel IMVP−6.5 specifications.

Multi−phase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling high currents in a single−phase converter would put too high of a thermal stress on system components such as the inductors and MOSFETs.

The multimode control of the APD3212A/NCP3218A is a stable, high performance architecture that includes

- Current and thermal balance between phases.
- High speed response at the lowest possible switching frequency and minimal count of output decoupling capacitors.
- Minimized thermal switching losses due to lower frequency operation.
- High accuracy load line regulation.
- High current output by supporting 2−phase or 3−phase operation.
- Reduced output ripple due to multi−phase ripple cancellation.
- High power conversion efficiency with heavy and light loads.
- Increased immunity from noise introduced by PC board layout constraints.
- Ease of use due to independent component selection.
- Flexibility in design by allowing optimization for either low cost or high performance.

Number of Phases

The number of operational phases can be set by the user. Tying the PH1 pin to the GND pin forces the chip into single−phase operation. Tying PH0 to GND and PH1 to VCC forces the chip into 2−phase operation. Tying PH0 and PH1 to VCC forces the chip in 3−phase operation. PH0 and PH1 should be hard wired to VCC or GND. The APD3212A/NCP3218A switches between single phase and multi−phase operation with $\overline{\text{PSI}}$ and DPRSLP to optimize power conversion efficiency. Table 1 summarizes PH0 and PH1.

Table 1. PHASE NUMBER CONFIGURATION

PH0	PH1	Number of Phases Configured
0	0	1
1	0	1 (GPU Mode)
0	1	2
1	1	3

In mulit−phase configuration, the timing relationship between the phases is determined by internal circuitry that monitors the PWM outputs. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be active at a time, permitting overlapping phases.

Operation Modes

The number of phases can be static (see the Number of Phases section) or dynamically controlled by system signals to optimize the power conversion efficiency with heavy and light loads.

If APD3212A/NCP3218A is configured for mulit−phase configuration, during a VID transient or with a heavy load condition (indicated by DPRSLP being low and $\overline{\text{PSI}}$ being high), the APD3212A/NCP3218A runs in multi−phase, interleaved PWM mode to achieve minimal V_{CORE} output voltage ripple and the best transient performance possible. If the load becomes light (indicated by $\overline{\text{PSI}}$ being low or DPRSLP being high), APD3212A/NCP3218A switches to single−phase mode to maximize the power conversion efficiency.

In addition to changing the number of phases, the APD3212A/NCP3218A is also capable of dynamically changing the control method. In dual−phase operation, the APD3212A/NCP3218A runs in PWM mode, where the switching frequency is controlled by the master clock. In single−phase operation (commanded by the DPRSLP high state), the APD3212A/NCP3218A runs in RPM mode, where the switching frequency is controlled by the ripple voltage appearing on the COMP pin. In RPM mode, the DRVH1 pin is driven high each time the COMP pin voltage rises to a voltage limit set by the VID voltage and an external resistor connected between the RPM pin and GND. In RPM mode, the APD3212A/NCP3218A turns off the low−side (synchronous rectifier) MOSFET when the inductor current drops to 0. Turning off the low−side MOSFETs at the zero current crossing prevents reversed inductor current build up and breaks synchronous operation of high− and low−side switches. Due to the asynchronous operation, the switching frequency becomes slower as the load current decreases, resulting in good power conversion efficiency with very light loads.

Table 2 summarizes how the APD3212A/NCP3218A dynamically changes the number of active phases and transitions the operation mode based on system signals and operating conditions.

GPU Mode

The APD3212A/NCP3218A can be used to power IMVP−6.5 GMCH. To configure the APD3212A/NCP3218A in GPU, connect PH1 to VCC and connect PH0 to GND. In GPU mode, the APD3212A/NCP3218A operates in single phase only. In GPU mode, the boot voltage is disabled. During startup, the output voltage ramps up to the programmed VID voltage. There is no other difference between GPU mode and normal CPU mode.

Table 2. PHASE NUMBER AND OPERATION MODES (Note 1)

$\overline{\text{PSI}}$ No.	DPRSLP	VID Transition (Note 2)	Current Limit	No. of Phases Selected by the User	No. of Phases in Operation	Operation Modes (Note 3)
*	*	Yes	*	N [3,2 or 1]	N	PWM, CCM only
1	0	No	*	N [3,2 or 1]	N	PWM, CCM only
0	0	No	No	*	1	RPM, CCM only
0	0	No	Yes	N [3,2 or 1]	N	PWM, CCM only
*	1	No	No	*	1	RPM, automatic CCM/DCM
*	1	No	Yes	*	1	PWM, CCM only

1. * = Don't Care.
2. VID transient period is the time following any VID change, including entry into and exit from deeper sleep mode. The duration of VID transient period is the same as that of PWRGD masking time.
3. CCM stands for continuous current mode, and DCM stands for discontinuous current mode.

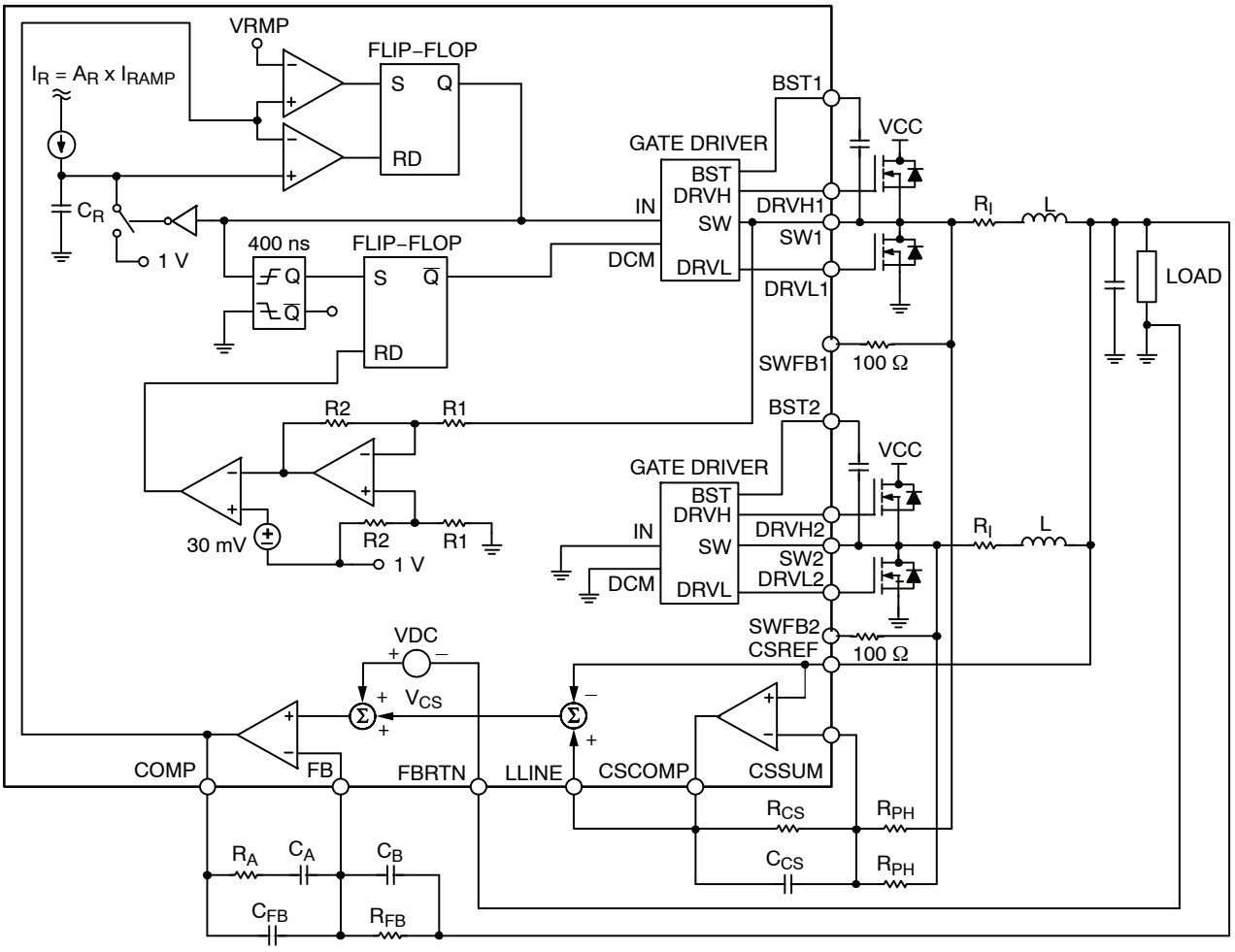


Figure 17. Single−Phase RPM Mode Operation

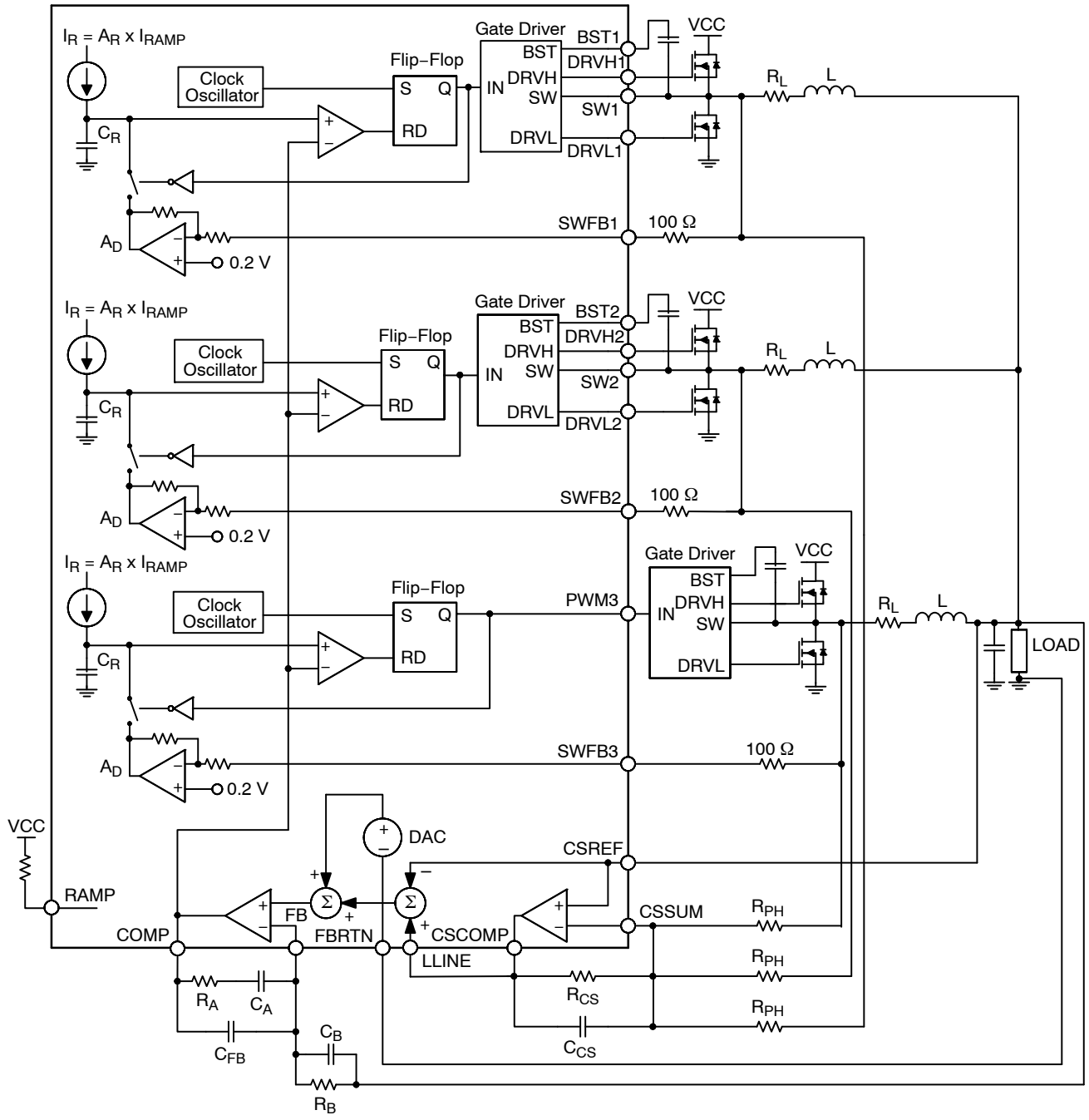


Figure 18. 3−Phase PWM Mode Operation

Setting Switch Frequency

Master Clock Frequency in PWM Mode

When the APD3212A/NCP3218A runs in PWM, the clock frequency is set by an external resistor connected from the RT pin to GND. The frequency is constant at a given VID code but varies with the VID voltage: the lower the VID voltage, the lower the clock frequency. The variation of clock frequency with VID voltage maintains constant V_{CORE} ripple and improves power conversion efficiency at lower VID voltages. Figure 7 shows the relationship between clock frequency and VID voltage, parameterized by RT resistance.

To determine the switching frequency per phase, divide the clock by the number of phases in use.

Switching Frequency in RPM Mode; Single−Phase Operation

In single−phase RPM mode, the switching frequency is controlled by the ripple voltage on the COMP pin, rather than by the master clock. Each time the COMP pin voltage

exceeds the RPM pin voltage threshold level determined by the VID voltage and the external resistor RPM resistor, an internal ramp signal is started and DRVH1 is driven high. The slew rate of the internal ramp is programmed by the current entering the RAMP pin. One−third of the RAMP current charges an internal ramp capacitor (5 pF typical) and creates a ramp. When the internal ramp signal intercepts the COMP voltage, the DRVH1 pin is reset low.

Differential Sensing of Output Voltage

The APD3212A/NCP3218A combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to meet the rigorous accuracy requirement of the Intel IMVP−6.5 specification. In steady−state mode, the combination of the VID DAC and error amplifier maintain the output voltage for a worst−case scenario within ±8 mV of the full operating output voltage and temperature range.

The CPU core output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point; the VCC remote sensing pin of the microprocessor. FBRTN should be connected directly to the negative remote sensing point; the V_{SS} sensing point of the CPU. The internal VID DAC and precision voltage reference are referenced to FBRTN and have a maximum current of 200 μA for guaranteed accurate remote sensing.

Output Current Sensing

The APD3212A/NCP3218A includes a dedicated Current Sense Amplifier (CSA) to monitor the total output current of the converter for proper voltage positioning vs. load current and for over current detection. Sensing the current delivered to the load is an inherently more accurate method than detecting peak current or sampling the current across a sense element, such as the low−side MOSFET. The current sense amplifier can be configured several ways, depending on system optimization objectives, and the current information can be obtained by:

- Output inductor ESR sensing without the use of a thermistor for the lowest cost.
- Output inductor ESR sensing with the use of a thermistor that tracks inductor temperature to improve accuracy.
- Discrete resistor sensing for the highest accuracy.

At the positive input of the CSA, the CSREF pin is connected to the output voltage. At the negative input (that is, the CSSUM pin of the CSA), signals from the sensing element (in the case of inductor DCR sensing, signals from the switch node side of the output inductors) are summed together by series summing resistors. The feedback resistor between the CSCOMP and CSSUM pins sets the gain of the current sense amplifier, and a filter capacitor is placed in parallel with this resistor. The current information is then given as the voltage difference between the CSCOMP and CSREF pins. This signal is used internally as a differential input for the current limit comparator.

An additional resistor divider connected between the CSCOMP and CSREF pins with the midpoint connected to the LLINE pin can be used to set the load line required by the microprocessor specification. The current information to set the load line is then given as the voltage difference between the LLINE and CSREF pins. This configuration allows the load line slope to be set independent from the current limit threshold. If the current limit threshold and load line do not have to be set independently, the resistor divider between the CSCOMP and CSREF pins can be omitted and the CSCOMP pin can be connected directly to LLINE. To disable voltage positioning entirely (that is, to set no load line), LLINE should be tied to CSREF.

To provide the best accuracy for current sensing, the CSA has a low offset input voltage and the sensing gain is set by an external resistor ratio.

Active Impedance Control Mode

To control the dynamic output voltage droop as a function of the output current, the signal that is proportional to the total output current, converted from the voltage difference between LLINE and CSREF, can be scaled to be equal to the required droop voltage. This droop voltage is calculated by multiplying the droop impedance of the regulator by the output current. This value is used as the control voltage of the PWM regulator. The droop voltage is subtracted from the DAC reference output voltage, and the resulting voltage is used as the voltage positioning set point. The arrangement results in an enhanced feed forward response.

Current Control Mode and Thermal Balance

The APD3212A/NCP3218A has individual inputs for monitoring the current of each phase. The phase current information is combined with an internal ramp to create a current−balancing feedback system that is optimized for initial current accuracy and dynamic thermal balance. The current balance information is independent from the total inductor current information used for voltage positioning described in the Active Impedance Control Mode section.

The magnitude of the internal ramp can be set so that the transient response of the system is optimal. The APD3212A/NCP3218A monitors the supply voltage to achieve feed forward control whenever the supply voltage changes. A resistor connected from the power input voltage rail to the RAMP pin determines the slope of the internal PWM ramp. More detail about programming the ramp is provided in the Application Information section.

External resistors are placed in series with the SWFB1, SWFB2, and SWFB3 pins to create an intentional current imbalance. Such a condition can exist when one phase has better cooling and supports higher currents the other phases. Resistors RSWSB1, RSWFB2, and RSWFB3 (see Figure 25) can be used to adjust thermal balance. It is recommended to add these resistors during the initial design to make sure placeholders are provided in the layout.

To increase the current in any given phase, users should make RSWFB for that phase larger (that is, RSWFB = 100 Ω for the hottest phase and do not change it during balance optimization). Increasing RSWFB to 150 Ω makes a substantial increase in phase current. Increase each RSWFB value by small amounts to achieve thermal balance starting with the coolest phase.

If adjusting current balance between phases is not needed, RSWFB should be 100 Ω for all phases.

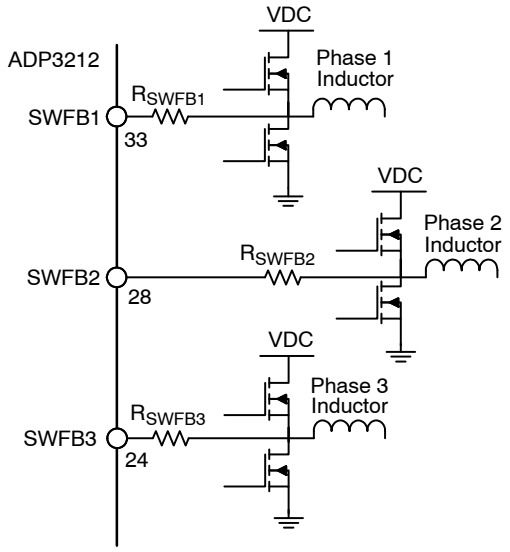


Figure 19. Current Balance Resistors

Voltage Control Mode

A high−gain bandwidth error amplifier is used for the voltage mode control loop. The non−inverting input voltage is set via the 7−bit VID DAC. The VID codes are listed in Table 3. The non−inverting input voltage is offset by the droop voltage as a function of current, commonly known as active voltage positioning. The output of the error amplifier is the COMP pin, which sets the termination voltage of the internal PWM ramps.

At the negative input, the FB pin is tied to the output sense location using R_B, a resistor for sensing and controlling the output voltage at the remote sensing point. The main loop compensation is incorporated in the feedback network connected between the FB and COMP pins.

Power−Good Monitoring

The power−good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output that can be pulled up through an external resistor to a voltage rail; not necessarily the same VCC voltage rail that is running the controller. A logic high level indicates that the output voltage is within the voltage limits defined by a range around the VID voltage setting. PWRGD goes low when the output voltage is outside of this range.

Following the IMVP−6.5 specification, the PWRGD range is defined to be 300 mV less than and 200 mV greater than the actual VID DAC output voltage. For any DAC voltage less than 300 mV, only the upper limit of the PWRGD range is monitored. To prevent a false alarm, the power−good circuit is masked during various system transitions, including a VID change and entrance into or exit out of deeper sleep. The duration of the PWRGD mask is set to approximately 130 μs by an internal timer. If the voltage drop is greater than 200 mV during deeper sleep entry or slow deeper sleep exit, the duration of PWRGD masking is extended by the internal logic circuit.

Powerup Sequence and Soft−Start

The power−on ramp−up time of the output voltage is set internally. The APD3212A/NCP3218A steps sequentially through each VID code until it reaches the boot voltage. The powerup sequence, including the soft−start is illustrated in Figure 20.

After EN is asserted high, the soft−start sequence starts. The core voltage ramps up linearly to the boot voltage. The APD3212A/NCP3218A regulates at the boot voltage for approximately 90 μs. After the boot time is over, $\overline{\text{CLKEN}}$ is asserted low. Before $\overline{\text{CLKEN}}$ is asserted low, the VID pins are ignored. 9 ms after $\overline{\text{CLKEN}}$ is asserted low, PWRGD is asserted high.

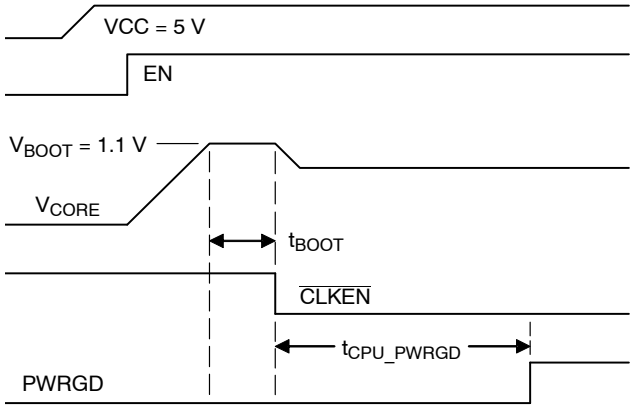


Figure 20. Powerup Sequence of APD3212A/NCP3218A

Current Limit

The APD3212A/NCP3218A compares the differential output of a current sense amplifier to a programmable current limit set point to provide the current limiting function. The current limit threshold is set by the user with a resistor connected from the ILIM pin to CSCOMP.

Changing VID On−The−Fly (OTF)

The APD3212A/NCP3218A is designed to track dynamically changing VID code. As a consequence, the CPU VCC voltage can change without the need to reset the controller or the CPU. This concept is commonly referred to as VID OTF transient. A VID OTF can occur with either light or heavy load conditions. The processor alerts the controller that a VID change is occurring by changing the VID inputs in LSB incremental steps from the start code to the finish code. The change can be either upwards or downwards steps.

When a VID input changes, the APD3212A/NCP3218A detects the change but ignores new code for a minimum of 400 ns. This delay is required to prevent the device from reacting to digital signal skew while the 7−bit VID input code is in transition. Additionally, the VID change triggers a PWRGD masking timer to prevent a PWRGD failure. Each VID change resets and retriggers the internal PWRGD masking timer.

As listed in Table 3, during a VID transient, the APD3212A/NCP3218A forces PWM mode regardless of the state of the system input signals. For example, this means that if the chip is configured as a dual−phase controller but is running in single−phase mode due to a light load condition, a current overload event causes the chip to switch to dual−phase mode to share the excessive load until the delayed current limit latchoff cycle terminates.

In user−set single−phase mode, the APD3212A/NCP3218A usually runs in RPM mode. When a VID transition occurs, however, the APD3212A/NCP3218A switches to dual−phase PWM mode.

Light Load RPM DCM Operation

In single−phase normal mode, DPRSLP is pulled low and the APD3208 operates in Continuous Conduction Mode (CCM) over the entire load range. The upper and lower MOSFETs run synchronously and in complementary phase. See Figure 21 for the typical waveforms of the APD3212A/NCP3218A running in CCM with a 7 A load current.

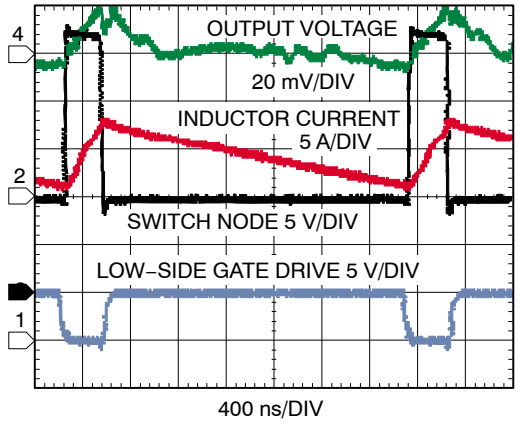


Figure 21. Single−Phase Waveforms in CCM

If DPRSLP is pulled high, the APD3212A/NCP3218A operates in RPM mode. If the load condition is light, the chip enters Discontinuous Conduction Mode (DCM). Figure 22 shows a typical single−phase buck with one upper FET, one lower FET, an output inductor, an output capacitor, and a load resistor. Figure 23 shows the path of the inductor current with the upper FET on and the lower FET off. In Figure 24, the high−side FET is off and the low−side FET is on. In CCM, if one FET is on, its complementary FET must be off; however, in DCM, both high− and low−side FETs are off and no current flows into the inductor (see Figure 25). Figure 26 shows the inductor current and switch node voltage in DCM.

In DCM with a light load, the APD3212A/NCP3218A monitors the switch node voltage to determine when to turn off the low−side FET. Figure 27 shows a typical waveform in DCM with a 1 A load current. Between t_1 and t_2, the inductor current ramps down. The current flows through the source drain of the low−side FET and creates a voltage drop across the FET with a slightly negative switch node. As the inductor current ramps down to 0 A, the switch voltage approaches 0 V, as seen just before t_2. When the switch voltage is approximately −6 mV, the low−side FET is turned off.

Figure 26 shows a small, dampened ringing at t_2. This is caused by the LC created from capacitance on the switch node, including the C_{DS} of the FETs and the output inductor. This ringing is normal.

The APD3212A/NCP3218A automatically goes into DCM with a light load. Figure 27 shows the typical DCM waveform of the APD3212A/NCP3218A. As the load increases, the APD3212A/NCP3218A enters into CCM. In DCM, frequency decreases with load current. Figure 28 shows switching frequency vs. load current for a typical design. In DCM, switching frequency is a function of the inductor, load current, input voltage, and output voltage.

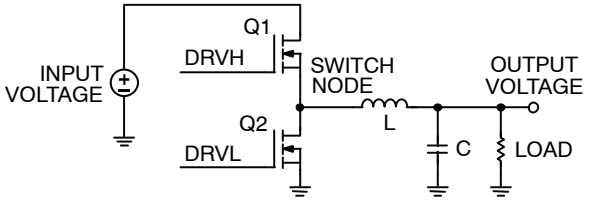


Figure 22. Buck Topology

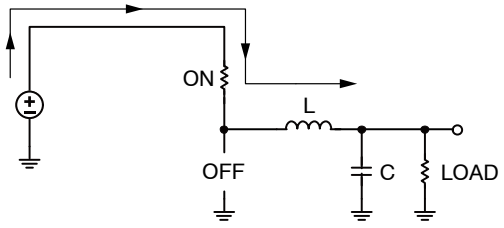


Figure 23. Buck Topology Inductor Current During t_0 and t_1

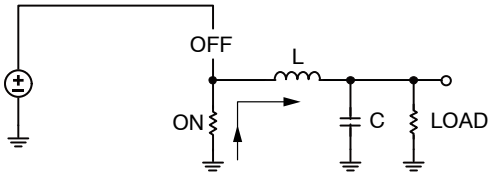


Figure 24. Buck Topology Inductor Current During t_1 and t_2

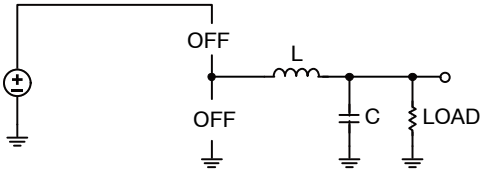


Figure 25. Buck Topology Inductor Current During t_2 and t_3

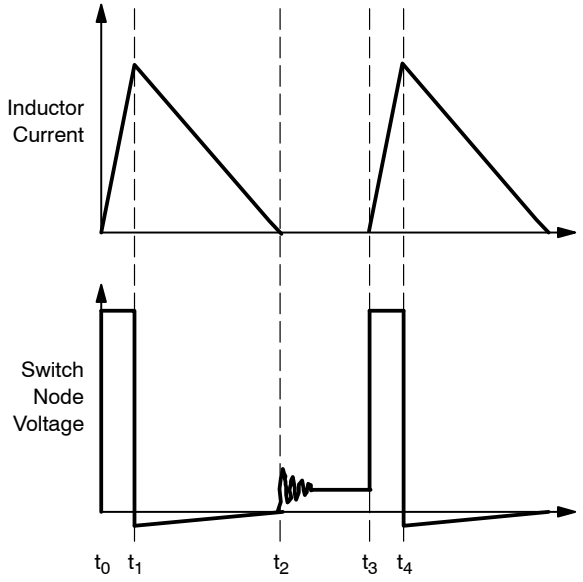


Figure 26. Inductor Current and Switch Node in DCM

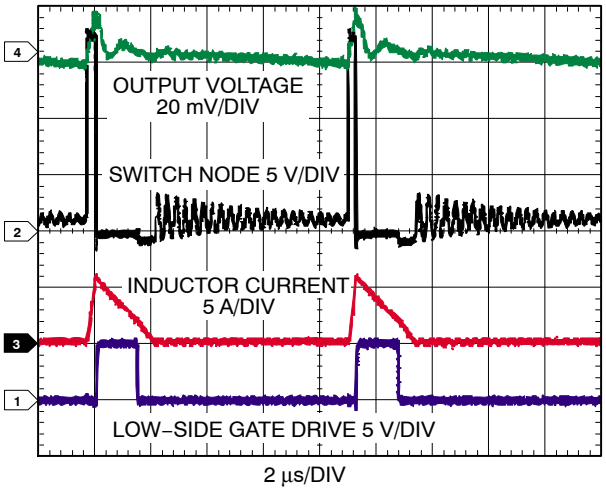


Figure 27. Single−Phase Waveforms in DCM with 1 A Load Current

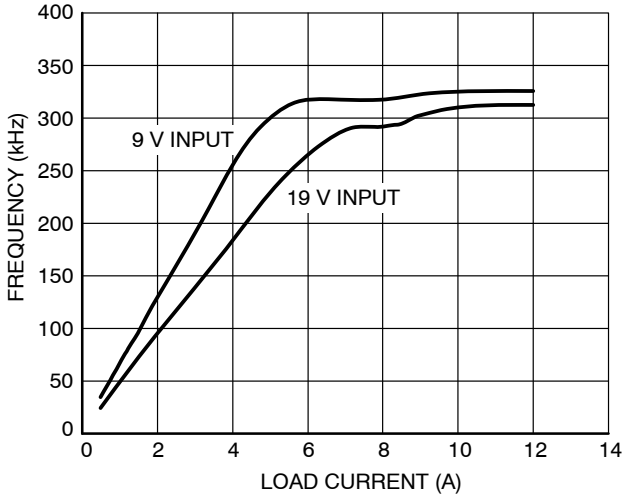


Figure 28. Single−Phase CCM/DCM Frequency vs. Load Current

Output Crowbar

To prevent the CPU and other external components from damage due to overvoltage, the APD3212A/NCP3218A turns off the DRVH1 and DRVH2 outputs and turns on the DRVL1 and DRVL2 outputs when the output voltage exceeds the OVP threshold (1.55 V typical).

Turning on the low−side MOSFETs forces the output capacitor to discharge and the current to reverse due to current build up in the inductors. If the output overvoltage is due to a drain−source short of the high−side MOSFET, turning on the low−side MOSFET results in a crowbar across the input voltage rail. The crowbar action blows the fuse of the input rail, breaking the circuit and thus protecting the microprocessor from destruction.

When the OVP feature is triggered, the APD3212A/NCP3218A is latched off. The latchoff function can be reset by removing and reapplying VCC to the APD3212A/NCP3218A or by briefly pulling the EN pin low.

Pulling TTSNS to less than 1.0 V disables the overvoltage protection function. In this configuration, VRTT should be tied to ground.

Reverse Voltage Protection

Very large reverse current in inductors can cause negative V_{CORE} voltage, which is harmful to the CPU and other output components. The APD3212A/NCP3218A provides a Reverse Voltage Protection (RVP) function without additional system cost. The V_{CORE} voltage is monitored through the CSREF pin. When the CSREF pin voltage drops to less than −300 mV, the APD3212A/NCP3218A triggers the RVP function by disabling all PWM outputs and driving DRVL1 and DRVL2 low, thus turning off all MOSFETs. The reverse inductor currents can be quickly reset to 0 by discharging the built−up energy in the inductor into the input dc voltage source via the forward−biased body diode of the high−side MOSFETs. The RVP function is terminated when the CSREF pin voltage returns to greater than −100 mV.

Sometimes the crowbar feature inadvertently causes output reverse voltage because turning on the low−side MOSFETs results in a very large reverse inductor current. To prevent damage to the CPU caused from negative voltage, the APD3212A/NCP3218A maintains its RVP monitoring function even after OVP latchoff. During OVP latchoff, if the CSREF pin voltage drops to less than −300 mV, the low−side MOSFETs is turned off. DRVL outputs are allowed to turn back on when the CSREF voltage recovers to greater than −100 mV.

Output Enable and UVLO

For the APD3212A/NCP3218A to begin switching, the VCC supply voltage to the controller must be greater than the V_{CCOK} threshold and the EN pin must be driven high. If the VCC voltage is less than the V_{CCUVLO} threshold or the EN pin is a logic low, the APD3212A/NCP3218A shuts off. In shutdown mode, the controller holds the PWM outputs low, shorts the capacitors of the SS and PGDELAY pins to ground, and drives the DRVH and DRVL outputs low.

The user must adhere to proper power−supply sequencing during startup and shutdown of the APD3212A/NCP3218A. All input pins must be at ground prior to removing or applying VCC, and all output pins should be left in high impedance state while VCC is off.

Thermal Throttling Control

The APD3212A/NCP3218A includes a thermal monitoring circuit to detect whether the temperature of the VR has exceeded a user−defined thermal throttling threshold. The thermal monitoring circuit requires an external resistor divider connected between the VCC pin and GND. The divider consists of an NTC thermistor and a resistor. To generate a voltage that is proportional to temperature, the midpoint of the divider is connected to the TTSNS pin. An internal comparator circuit compares the TTSNS voltage to half the VCC threshold and outputs a logic level signal at the VRTT output when the temperature trips the user−set alarm threshold. The VRTT output is designed to drive an external transistor that in turn provides the high current, open−drain VRTT signal required by the IMVP−6.5 specification. The internal VRTT comparator has a hysteresis of approximately 100 mV to prevent high frequency oscillation of VRTT when the temperature approaches the set alarm point.

Output Current Monitor

The APD3212A/NCP3218A has an output current monitor. The IMON pin sources a current proportional to the inductor current. A resistor from IMON pin to FBRTN sets the gain. A 0.1 μF is added in parallel with R_{MON} to filter the inductor ripple. The IMON pin is clamped to prevent it from going above 1.15 V.

Table 3. VID CODE TABLE

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	0	0	0	0	0	0	1.5000 V
0	0	0	0	0	0	0	1.5000 V
0	0	0	0	0	0	1	1.4875 V
0	0	0	0	0	1	0	1.4750 V
0	0	0	0	0	1	1	1.4625 V
0	0	0	0	1	0	0	1.4500 V
0	0	0	0	1	0	1	1.4375 V
0	0	0	0	1	1	0	1.4250 V
0	0	0	0	1	1	1	1.4125 V
0	0	0	1	0	0	0	1.4000 V
0	0	0	1	0	0	1	1.3875 V
0	0	0	1	0	1	0	1.3750 V
0	0	0	1	0	1	1	1.3625 V
0	0	0	1	1	0	0	1.3500 V
0	0	0	1	1	0	1	1.3375 V
0	0	0	1	1	1	0	1.3250 V
0	0	0	1	1	1	1	1.3125 V
0	0	1	0	0	0	0	1.3000 V
0	0	1	0	0	0	1	1.2875 V
0	0	1	0	0	1	0	1.2750 V
0	0	1	0	0	1	1	1.2625 V
0	0	1	0	1	0	0	1.2500 V
0	0	1	0	1	0	1	1.2375 V
0	0	1	0	1	1	0	1.2250 V
0	0	1	0	1	1	1	1.2125 V
0	0	1	1	0	0	0	1.2000 V
0	0	1	1	0	0	1	1.1875 V
0	0	1	1	0	1	0	1.1750 V
0	0	1	1	0	1	1	1.1625 V
0	0	1	1	1	0	0	1.1500 V
0	0	1	1	1	0	1	1.1375 V
0	0	1	1	1	1	0	1.1250 V
0	0	1	1	1	1	1	1.1125 V

Table 3. VID CODE TABLE (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	0	0	0	0	1.1000 V
0	1	0	0	0	0	1	1.0875 V
0	1	0	0	0	1	0	1.0750 V
0	1	0	0	0	1	1	1.0625 V
0	1	0	0	1	0	0	1.0500 V
0	1	0	0	1	0	1	1.0375 V
0	1	0	0	1	1	0	1.0250 V
0	1	0	0	1	1	1	1.0125 V
0	1	0	1	0	0	0	1.0000 V
0	1	0	1	0	0	1	0.9875 V
0	1	0	1	0	1	0	0.9750 V
0	1	0	1	0	1	1	0.9625 V
0	1	0	1	1	0	0	0.9500 V
0	1	0	1	1	0	1	0.9375 V
0	1	0	1	1	1	0	0.9250 V
0	1	0	1	1	1	1	0.9125 V
0	1	1	0	0	0	0	0.9000 V
0	1	1	0	0	0	1	0.8875 V
0	1	1	0	0	1	0	0.8750 V
0	1	1	0	0	1	1	0.8625 V
0	1	1	0	1	0	0	0.8500 V
0	1	1	0	1	0	1	0.8375 V
0	1	1	0	1	1	0	0.8250 V
0	1	1	0	1	1	1	0.8125 V
0	1	1	1	0	0	0	0.8000 V
0	1	1	1	0	0	1	0.7875 V
0	1	1	1	0	1	0	0.7750 V
0	1	1	1	0	1	1	0.7625 V
0	1	1	1	1	0	0	0.7500 V
0	1	1	1	1	0	1	0.7375 V
0	1	1	1	1	1	0	0.7250 V
0	1	1	1	1	1	1	0.7125 V
1	0	0	0	0	0	0	0.7000 V
1	0	0	0	0	0	1	0.6875 V
1	0	0	0	0	1	0	0.6750 V
1	0	0	0	0	1	1	0.6625 V
1	0	0	0	1	0	0	0.6500 V
1	0	0	0	1	0	1	0.6375 V
1	0	0	0	1	1	0	0.6250 V
1	0	0	0	1	1	1	0.6125 V
1	0	0	1	0	0	0	0.6000 V
1	0	0	1	0	0	1	0.5875 V
1	0	0	1	0	1	0	0.5750 V
1	0	0	1	0	1	1	0.5625 V
1	0	0	1	1	0	0	0.5500 V
1	0	0	1	1	0	1	0.5375 V
1	0	0	1	1	1	0	0.5250 V
1	0	0	1	1	1	1	0.5125 V
1	0	1	0	0	0	0	0.5000 V

Table 3. VID CODE TABLE (continued)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
1	0	1	0	0	0	1	0.4875 V
1	0	1	0	0	1	0	0.4750 V
1	0	1	0	0	1	1	0.4625 V
1	0	1	0	1	0	0	0.4500 V
1	0	1	0	1	0	1	0.4375 V
1	0	1	0	1	1	0	0.4250 V
1	0	1	0	1	1	1	0.4125 V
1	0	1	1	0	0	0	0.4000 V
1	0	1	1	0	0	1	0.3875 V
1	0	1	1	0	1	0	0.3750 V
1	0	1	1	0	1	1	0.3625 V
1	0	1	1	1	0	0	0.3500 V
1	0	1	1	1	0	1	0.3375 V
1	0	1	1	1	1	0	0.3250 V
1	0	1	1	1	1	1	0.3125 V
1	1	0	0	0	0	0	0.3000 V
1	1	0	0	0	0	1	0.2875 V
1	1	0	0	0	1	0	0.2750 V
1	1	0	0	0	1	1	0.2625 V
1	1	0	0	1	0	0	0.2500 V
1	1	0	0	1	0	1	0.2375 V
1	1	0	0	1	1	0	0.2250 V
1	1	0	0	1	1	1	0.2125 V
1	1	0	1	0	0	0	0.2000 V
1	1	0	1	0	0	1	0.1875 V
1	1	0	1	0	1	0	0.1750 V
1	1	0	1	0	1	1	0.1625 V
1	1	0	1	1	0	0	0.1500 V
1	1	0	1	1	0	1	0.1375 V
1	1	0	1	1	1	0	0.1250 V
1	1	0	1	1	1	1	0.1125 V
1	1	1	0	0	0	0	0.1000 V
1	1	1	0	0	0	1	0.0875 V
1	1	1	0	0	1	0	0.0750 V
1	1	1	0	0	1	1	0.0625 V
1	1	1	0	1	0	0	0.0500 V
1	1	1	0	1	0	1	0.0375 V
1	1	1	0	1	1	0	0.0250 V
1	1	1	0	1	1	1	0.0125 V
1	1	1	1	0	0	0	0.0000 V
1	1	1	1	0	0	1	0.0000 V
1	1	1	1	0	1	0	0.0000 V
1	1	1	1	0	1	1	0.0000 V
1	1	1	1	1	0	0	0.0000 V
1	1	1	1	1	0	1	0.0000 V
1	1	1	1	1	1	0	0.0000 V
1	1	1	1	1	1	1	0.0000 V

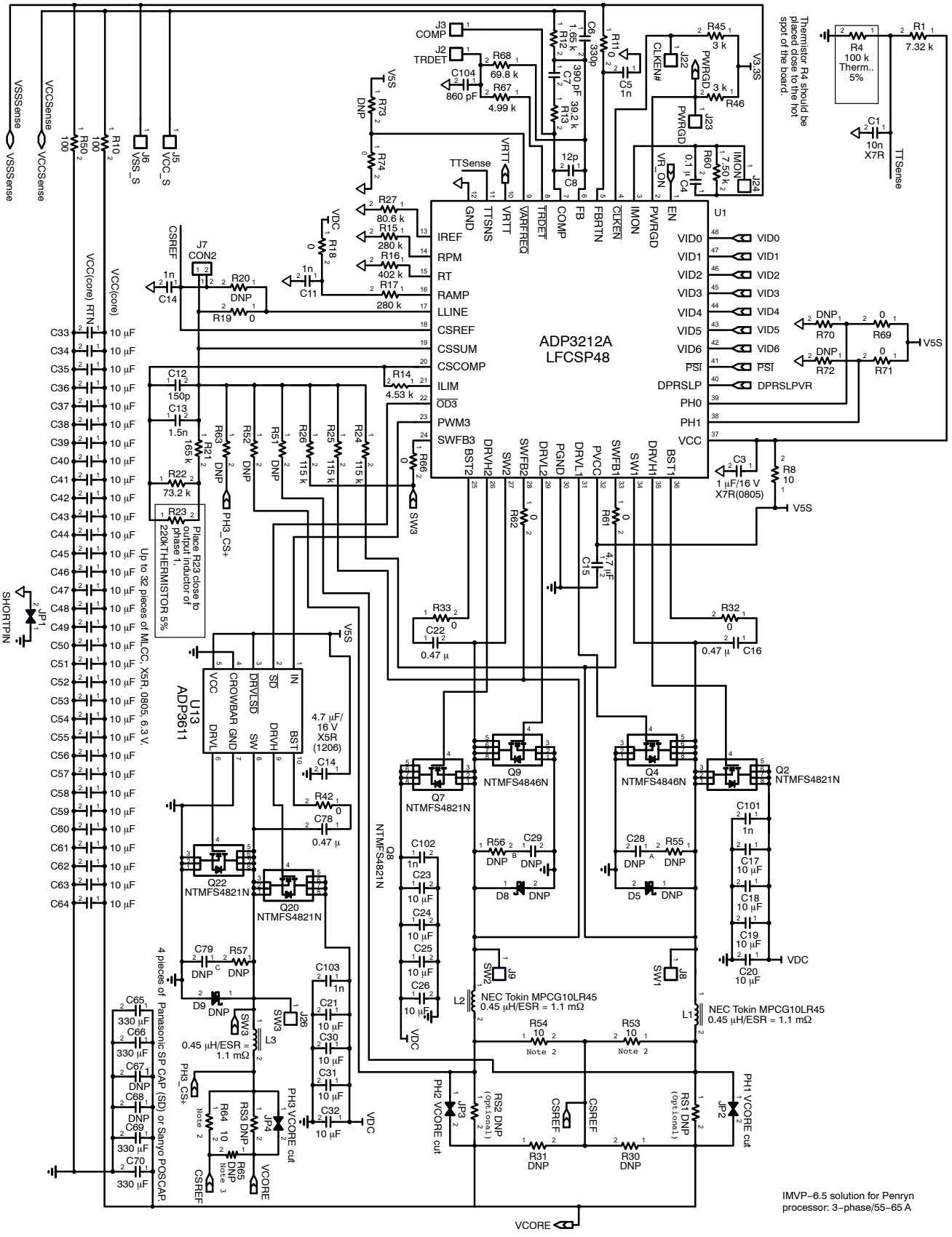


Figure 29. Typical Dual−Phase Application Circuit

Application Information

The design parameters for a typical IMVP−6.5−compliant CPU core VR application are as follows:

- Maximum input voltage (V_{INMAX}) = 19 V
- Minimum input voltage (V_{INMIN}) = 8.0 V
- Output voltage by VID setting (V_{VID}) = 1.05 V
- Maximum output current (I_O) = 52 A
- Droop resistance (R_O) = 1.9 mΩ
- Nominal output voltage at 40 A load (V_{OFL}) = 0.9512 V
- Static output voltage drop from no load to full load (ΔV) = $V_{ONL} - V_{OFL}$ = 1.05 V − 0.9512 V = 98 mV
- Maximum output current step (ΔI_O) = 52 A
- Number of phases (n) = 2
- Switching frequency per phase (f_{SW}) = 300 kHz
- Duty cycle at maximum input voltage (D_{MAX}) = 0.13 V
- Duty cycle at minimum input voltage (D_{MIN}) = 0.055 V

Setting the Clock Frequency for PWM

In PWM operation, the APD3212A/NCP3218A uses a fixed−frequency control architecture. The frequency is set by an external timing resistor (RT). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to the switching losses and the sizes of the inductors and input and output capacitors. For a dual−phase design, a clock frequency of 600 kHz sets the switching frequency to 300 kHz per phase. This selection represents the trade−off between the switching losses and the minimum sizes of the output filter components. To achieve a 600 kHz oscillator frequency at a VID voltage of 1.2 V, RT must be 181 kΩ. Alternatively, the value for RT can be calculated by using the following equation:

$$R_T = \frac{V_{VID} + 1.0\ V}{2 \times n \times f_{SW} \times 9\ pF} - 16\ k\Omega \qquad \text{(eq. 1)}$$

where:

9 pF and 16 kΩ are internal IC component values.
V_{VID} is the VID voltage in volts.
n is the number of phases.
f_{SW} is the switching frequency in hertz for each phase.

For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

When VARFREQ pin is connected to ground, the switching frequency does not change with VID. The value for RT can be calculated by using the following equation.

$$R_T = \frac{1.0\ V}{n \times 2 \times f_{SW} \times 9\ pF} - 16\ k\Omega \qquad \text{(eq. 2)}$$

Setting the Switching Frequency for RPM Operation of Phase 1

During the RPM operation of Phase 1, the APD3212A/NCP3218A runs in pseudoconstant frequency if the load current is high enough for continuous current mode. While in DCM, the switching frequency is reduced with the load current in a linear manner.

To save power with light loads, lower switching frequency is usually preferred during RPM operation. However, the V_{CORE} ripple specification of IMVP−6.5 sets a limitation for the lowest switching frequency. Therefore, depending on the inductor and output capacitors, the switching frequency in RPM can be equal to, greater than, or less than its counterpart in PWM.

A resistor from RPM to GND sets the pseudo constant frequency as following:

$$R_{RPM} = \frac{2 \times R_T}{V_{VID} + 1.0\ V} \times \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} - 0.5\ k\Omega \qquad \text{(eq. 3)}$$

where:

A_R is the internal ramp amplifier gain.
C_R is the internal ramp capacitor value.
R_R is an external resistor on the RAMPADJ pin to set the internal ramp magnitude.

Soft−Start and Current Limit Latchoff Delay Times Inductor Selection

The choice of inductance determines the ripple current of the inductor. Less inductance results in more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs. However, this allows the use of smaller−size inductors, and for a specified peak−to−peak transient deviation, it allows less total output capacitance. Conversely, a higher inductance results in lower ripple current and reduced conduction losses, but it requires larger−size inductors and more output capacitance for the same peak−to−peak transient deviation. For a multi−phase converter, the practical value for peak−to−peak inductor ripple current is less than 50% of the maximum dc current of that inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak−to−peak ripple current. Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{VID} \times (1 - D_{MIN})}{f_{SW} \times L} \qquad \text{(eq. 4)}$$

$$L \geq \frac{V_{VID} \times R_O \times \left(1 - (n \times D_{MIN})\right)}{f_{SW} \times V_{RIPPLE}} \qquad \text{(eq. 5)}$$

Solving Equation 5 for a 16 mV peak−to−peak output ripple voltage yields:

$$L \geq \frac{1.05\ V \times 1.9\ m\Omega \times (1 - 2 \times 0.055)}{300\ kHz \times 16\ mV} = 528\ nH$$

If the resultant ripple voltage is less than the initially selected value, the inductor can be changed to a smaller value until the ripple value is met. This iteration allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 490 nH inductor is a good choice for a starting point, and it provides a calculated ripple current of 9.0 A. The inductor should not saturate at the peak current of 24.5 A, and it should be able to handle the sum of the power dissipation caused by the

winding's average current (20 A) plus the ac core loss. In this example, 330 nH is used.

Another important factor in the inductor design is the DCR, which is used for measuring the phase currents. Too large of a DCR causes excessive power losses, whereas too small of a value leads to increased measurement error. For this example, an inductor with a DCR of 0.8 mΩ is used.

Selecting a Standard Inductor

After the inductance and DCR are known, select a standard inductor that best meets the overall design goals. It is also important to specify the inductance and DCR tolerance to maintain the accuracy of the system. Using 20% tolerance for the inductance and 15% for the DCR at room temperature are reasonable values that most manufacturers can meet.

Power Inductor Manufacturers

The following companies provide surface−mount power inductors optimized for high power applications upon request:

- Vishay Dale Electronics, Inc.
  (605) 665−9301
- Panasonic
  (714) 373−7334
- Sumida Electric Company
  (847) 545−6700
- NEC Tokin Corporation
  (510) 324−4110

Output Droop Resistance

The design requires that the regulator output voltage measured at the CPU pins decreases when the output current increases. The specified voltage drop corresponds to the droop resistance (R_O).

The output current is measured by summing the currents of the resistors monitoring the voltage across each inductor and by passing the signal through a low−pass filter. The summing is implemented by the CS amplifier that is configured with resistor $R_{PH(x)}$ (summer) and resistors R_{CS} and C_{CS} (filters). The output resistance of the regulator is set by the following equations:

$$R_O = \frac{R_{CS}}{R_{PH(x)}} \times R_{SENSE} \quad \text{(eq. 6)}$$

$$C_{CS} = \frac{L}{R_{SENSE} \times R_{CS}} \quad \text{(eq. 7)}$$

where R_{SENSE} is the DCR of the output inductors.

Either R_{CS} or $R_{PH(x)}$ can be chosen for added flexibility. Due to the current drive ability of the CSCOMP pin, the R_{CS} resistance should be greater than 100 kΩ. For example, initially select R_{CS} to be equal to 200 kΩ, and then use Equation 7 to solve for C_{CS}:

$$C_{CS} = \frac{330\ \text{nH}}{0.8\ \text{m}\Omega \times 200\ \text{k}\Omega} = 2.1\ \text{nF}$$

If C_{CS} is not a standard capacitance, R_{CS} can be tuned. For example, if the optimal C_{CS} capacitance is 1.5 nF, adjust R_{CS} to 280 kΩ. For best accuracy, C_{CS} should be a 5% NPO capacitor. In this example, a 220 kΩ is used for R_{CS} to achieve optimal results.

Next, solve for $R_{PH(x)}$ by rearranging Equation 6 as follows:

$$R_{PH(x)} \geq \frac{0.8\ \text{m}\Omega}{2.1\ \text{m}\Omega} \times 220\ \text{k}\Omega = 83.8\ \text{k}\Omega$$

The standard 1% resistor for $R_{PH(x)}$ is 86.6 kΩ.

Inductor DCR Temperature Correction

If the DCR of the inductor is used as a sense element and copper wire is the source of the DCR, the temperature changes associated with the inductor's winding must be compensated for. Fortunately, copper has a well−known Temperature Coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite but equal percentage of change in resistance, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, series resistors R_{CS1} and R_{CS2} (see Figure 30) are needed to linearize the NTC and produce the desired temperature coefficient tracking.

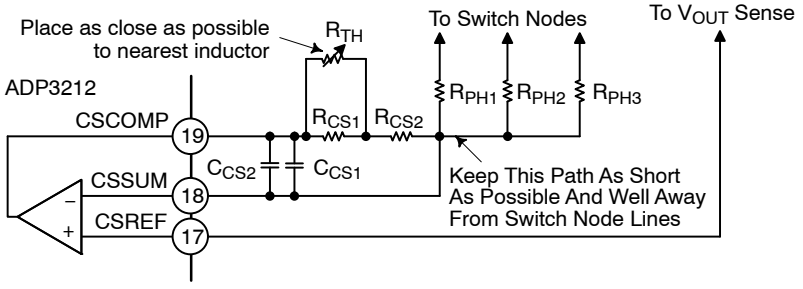


Figure 30. Temperature−Compensation Circuit Values

The following procedure and expressions yield values for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC to be used based on its type and value. Because the value needed is not yet determined, start with a thermistor with a value close to R_{CS} and an NTC with an initial tolerance of better than 5%.
2. Find the relative resistance value of the NTC at two temperatures. The appropriate temperatures will depend on the type of NTC, but 50°C and 90°C have been shown to work well for most types of NTCs. The resistance values are called A (A is $R_{TH}(50°C)/R_{TH}(25°C)$) and B (B is $R_{TH}(90°C)/R_{TH}(25°C)$). Note that the relative value of the NTC is always 1 at 25°C.
3. Find the relative value of R_{CS} required for each of the two temperatures. The relative value of R_{CS} is based on the percentage of change needed, which is initially assumed to be 0.39%/°C in this example.
   The relative values are called r_1 (r_1 is $1/(1+ TC \times (T_1 - 25))$) and r_2 (r_2 is $1/(1 + TC \times (T_2 - 25))$), where TC is 0.0039, T_1 is 50°C, and T_2 is 90°C.
4. Compute the relative values for r_{CS1}, r_{CS2}, and r_{TH} by using the following equations:

$$r_{CS2} = \frac{(A-B) \times r_1 \times r_2 - A \times (1-B) \times r_2 + B \times (1-A) \times r_1}{A \times (1 - B) \times r_1 - B \times (1 - A) \times r_2 - (A - B)}$$

$$r_{CS1} = \frac{(1 - A)}{\frac{1}{1-r_{CS2}} - \frac{A}{r_1 - r_{CS2}}} \quad \text{(eq. 8)}$$

$$r_{TH} = \frac{1}{\frac{1}{1-r_{CS2}} - \frac{1}{r_{CS1}}}$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, and then select a thermistor of the closest value available. In addition, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad \text{(eq. 9)}$$

6. Calculate values for R_{CS1} and R_{CS2} by using the following equations:

$$R_{CS1} = R_{CS} \times k \times r_{CS1}$$
$$R_{CS2} = R_{CS} \times \left((1 - k) + (k \times r_{CS2})\right) \quad \text{(eq. 10)}$$

For example, if a thermistor value of 100 kΩ is selected in Step 1, an available 0603−size thermistor with a value close to R_{CS} is the Vishay NTHS0603N04 NTC thermistor, which has resistance values of A = 0.3359 and B = 0.0771. Using the equations in Step 4, r_{CS1} is 0.359, r_{CS2} is 0.729, and r_{TH} is 1.094. Solving for r_{TH} yields 241 kΩ, so a thermistor of 220 kΩ would be a reasonable selection, making k equal to 0.913. Finally, R_{CS1} and R_{CS2} are found to be 72.1 kΩ and 166 kΩ. Choosing the closest 1% resistor for R_{CS2} yields 165 kΩ. To correct for this approximation, 73.3 kΩ is used for R_{CS1}.

C_{OUT} Selection

The required output decoupling for processors and platforms is typically recommended by Intel. For systems containing both bulk and ceramic capacitors, however, the following guidelines can be a helpful supplement.

Select the number of ceramics and determine the total ceramic capacitance (C_Z). This is based on the number and type of capacitors used. Keep in mind that the best location to place ceramic capacitors is inside the socket; however, the physical limit is twenty 0805−size pieces inside the socket. Additional ceramic capacitors can be placed along the outer edge of the socket. A combined ceramic capacitor value of 200 μF to 300 μF is recommended and is usually composed of multiple 10 μF or 22 μF capacitors.

Ensure that the total amount of bulk capacitance (C_X) is within its limits. The upper limit is dependent on the VID OTF output voltage stepping (voltage step, V_V, in time, t_V, with error of V_{ERR}); the lower limit is based on meeting the critical capacitance for load release at a given maximum load step, ΔI_O. The current version of the IMVP−6.5 specification allows a maximum V_{CORE} overshoot (V_{OSMAX}) of 10 mV more than the VID voltage for a step−off load current.

$$C_{X(MIN)} \geq \left[\frac{L \times \Delta I_O}{n \times \left(R_O + \frac{V_{OSMAX}}{\Delta I_O} \right) \times V_{VID}} - C_Z \right] \quad \text{(eq. 11)}$$

$$C_{X(MAX)} \leq \frac{L}{n \times k^2 \times R_O{}^2} \times \frac{V_V}{V_{VID}} \times \left[\sqrt{1 + \left(t_v \frac{V_{VID}}{V_V} \times \frac{n \times k \times R_O}{L} \right)^2} - 1 \right] - C_Z$$

$$\text{where } k = -\ln\left(\frac{V_{ERR}}{V_V}\right) \quad \text{(eq. 12)}$$

To meet the conditions of these expressions and the transient response, the ESR of the bulk capacitor bank (R_X) should be less than two times the droop resistance, R_O. If the $C_{X(MIN)}$ is greater than $C_{X(MAX)}$, the system does not meet the VID OTF and/or the deeper sleep exit specifications and may require less inductance or more phases. In addition, the switching frequency may have to be increased to maintain the output ripple.

For example, if 30 pieces of 10 μF, 0805−size MLC capacitors (C_Z = 300 μF) are used, the fastest VID voltage change is when the device exits deeper sleep, during which the V_{CORE} change is 220 mV in 22 μs with a setting error of 10 mV. If k = 3.1, solving for the bulk capacitance yields

$$C_{X(MIN)} \geq \left(\frac{330\ \text{nH} \times 27.9\ \text{A}}{2 \times \left(2.1\ \text{m}\Omega + \frac{10\ \text{mV}}{27.9\ \text{A}}\right) \times 1.4375\ \text{V}} - 300\ \mu\text{F} \right) = 1.0\ \text{mF}$$

$$C_{X(MAX)} \leq \frac{330\ \text{nH} \times 220\ \text{mV}}{2 \times 3.1^2 \times (2.1\ \text{m}\Omega)^2 \times 1.4375\ \text{V}} \times \left(\sqrt{1 + \left(\frac{22\mu\text{s} \times 1.4375\text{V} \times 2 \times 3.1 \times 2.1\text{m}\Omega}{220\ \text{mV} \times 490\ \text{nH}} \right)^2} - 1 \right) - 300\ \mu\text{F}$$

$$= 21\ \text{mF}$$

Using six 330 μF Panasonic SP capacitors with a typical ESR of 7 mΩ each yields C_X = 1.98 mF and R_X = 1.2 mΩ.

Ensure that the ESL of the bulk capacitors (L_X) is low enough to limit the high frequency ringing during a load change. This is tested using:

$$L_X \leq C_Z \times {R_O}^2 \times Q^2$$
$$L_X \leq 300\ \mu\text{F} \times (2.1\ \text{m}\Omega)^2 \times 2 = 2\ \text{nH} \quad \text{(eq. 13)}$$

where:

Q is limited to the square root of 2 to ensure a critically damped system.

L_X is about 150 pH for the six SP capacitors, which is low enough to avoid ringing during a load change. If the L_X of the chosen bulk capacitor bank is too large, the number of ceramic capacitors may need to be increased to prevent excessive ringing.

For this multimode control technique, an all ceramic capacitor design can be used if the conditions of Equations 11, 12, and 13 are satisfied.

Power MOSFETs

For typical 20 A per phase applications, the N−channel power MOSFETs are selected for two high−side switches and two or three low−side switches per phase. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. Because the voltage of the gate driver is 5.0 V, logic−level threshold MOSFETs must be used.

The maximum output current, I_O, determines the $R_{DS(ON)}$ requirement for the low−side (synchronous) MOSFETs. In the APD3212A/NCP3218A, currents are balanced between phases; the current in each low−side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following expression shows the total power that is dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and the average total output current (I_O):

$$P_{SF} = (1-D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad \text{(eq. 14)}$$

where:

D is the duty cycle and is approximately the output voltage divided by the input voltage.

I_R is the inductor peak−to−peak ripple current and is approximately

$$I_R = \frac{(1 - D) \times V_{OUT}}{L \times f_{SW}}$$

Knowing the maximum output current and the maximum allowed power dissipation, the user can calculate the required $R_{DS(ON)}$ for the MOSFET. For 8−lead SOIC or 8−lead SOIC compatible MOSFETs, the junction−to−ambient (PCB) thermal impedance is 50°C/W. In the worst case, the PCB temperature is 70°C to 80°C during heavy load operation of the notebook, and a safe limit for P_{SF} is about 0.8 W to 1.0 W at 120°C junction temperature. Therefore, for this example (40 A maximum), the $R_{DS(SF)}$ per MOSFET is less than 8.5 mΩ for two pieces of low−side MOSFETs. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C; therefore, the $R_{DS(SF)}$ per MOSFET should be less than 6 mΩ at room temperature, or 8.5 mΩ at high temperature.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input must be small (less than 10% is recommended) to prevent accidentally turning on the synchronous MOSFETs when the switch node goes high.

The high−side (main) MOSFET must be able to handle two main power dissipation components: conduction losses and switching losses. Switching loss is related to the time for the main MOSFET to turn on and off and to the current and voltage that are being switched. Basing the switching speed on the rise and fall times of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{DC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \quad \text{(eq. 15)}$$

where:

n_{MF} is the total number of main MOSFETs.

R_G is the total gate resistance.

C_{ISS} is the input capacitance of the main MOSFET.

The most effective way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad \text{(eq. 16)}$$

where $R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, a user wants the highest speed (low C_{ISS}) device for a main MOSFET, but such a device usually has higher on resistance. Therefore, the user must select a device that meets the total power dissipation (about 0.8 W to 1.0 W for an 8−lead SOIC) when combining the switching and conduction losses.

For example, an IRF7821 device can be selected as the main MOSFET (four in total; that is, n_{MF} = 4), with approximately
C_{ISS} = 1010 pF (maximum) and $R_{DS(MF)}$ = 18 mΩ (maximum at T_J = 120°C), and an IR7832 device can be selected as the synchronous MOSFET (four in total; that is, n_{SF} = 4), with
$R_{DS(SF)}$ = 6.7 mΩ (maximum at T_J = 120°C). Solving for the power dissipation per MOSFET at I_O = 40 A and I_R = 9.0 A yields 630 mW for each synchronous MOSFET and 590 mW for each main MOSFET. A third synchronous MOSFET is an option to further increase the conversion efficiency and reduce thermal stress.

Finally, consider the power dissipation in the driver for each phase. This is best described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}) + I_{CC} \right] \times VCC \quad \text{(eq. 17)}$$

where Q_{GMF} is the total gate charge for each main MOSFET, and Q_{GSF} is the total gate charge for each synchronous MOSFET.

The previous equation also shows the standby dissipation (I_{CC} times the VCC) of the driver.

Ramp Resistor Selection

The ramp resistor (R_R) is used to set the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. Use the following expression to determine a starting value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R} \quad \text{(eq. 18)}$$

$$R_R = \frac{0.5 \times 360\ \text{nH}}{3 \times 5 \times 5.2\ \text{m}\Omega \times 5\ \text{pF}} = 462\ \text{k}\Omega$$

where:

A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
R_{DS} is the total low−side MOSFET on resistance.
C_R is the internal ramp capacitor value.

Another consideration in the selection of R_R is the size of the internal ramp voltage (see Equation 19). For stability and noise immunity, keep the ramp size larger than 0.5 V. Taking this into consideration, the value of R_R in this example is selected as 280 kΩ.

The internal ramp voltage magnitude can be calculated as follows:

$$V_R = \frac{A_R \times (1 - D) \times V_{VID}}{R_R \times C_R \times f_{SW}} \quad \text{(eq. 19)}$$

$$V_R = \frac{0.5 \times (1 - 0.061) \times 1.150\ \text{V}}{462\ \text{k}\Omega \times 5\ \text{pF} \times 280\ \text{kHz}} = 0.83\ \text{V}$$

The size of the internal ramp can be increased or decreased. If it is increased, stability and transient response improves but thermal balance degrades. Conversely, if the ramp size is decreased, thermal balance improves but stability and transient response degrade. In the denominator of Equation 18, the factor of 3 sets the minimum ramp size that produces an optimal combination of good stability, transient response, and thermal balance.

Current Limit Setpoint

To select the current limit setpoint, the resistor value for R_{CLIM} must be determined. The current limit threshold for the APD3212A/NCP3218A is set with R_{CLIM}. R_{CLIM} can be found using the following equation:

$$R_{LIM} = \frac{I_{LIM} \times R_O}{60\ \mu\text{A}} \quad \text{(eq. 20)}$$

where:

R_{LIM} is the current limit resistor.
R_O is the output load line.
I_{LIM} is the current limit setpoint.

When the APD3212A/NCP3218A is configured for 3 phase operation, the equation above is used to set the current limit. When the APD3212A/NCP3218A switches from 3 phase to 1 phase operation by $\overline{\text{PSI}}$ or DPRSLP signal, the current is single phase is one third of the current limit in 3 phase.

When the APD3212A/NCP3218A is configured for 2 phase operation, the equation above is used to set the current limit. When the APD3212A/NCP3218A switches from 2 phase to 1 phase operation by $\overline{\text{PSI}}$ or DPRSLP signal, the current is single phase is one half of the current limit in 2 phase.

When the APD3212A/NCP3218A is configured for 1 phase operation, the equation above is used to set the current limit.

Current Monitor

The APD3212A/NCP3218A has output current monitor. The IMON pin sources a current proportional to the total inductor current. A resistor, R_{MON}, from IMON to FBRTN sets the gain of the output current monitor. A 0.1 μF is placed in parallel with R_{MON} to filter the inductor current ripple and

high frequency load transients. Since the IMON pin is connected directly to the CPU, it is clamped to prevent it from going above 1.15 V.

The IMON pin current is equal to the R_{LIM} times a fixed gain of 4. R_{MON} can be found using the following equation:

$$R_{MON} = \frac{1.15\ V \times R_{LIM}}{4 \times R_O \times I_{FS}} \quad \text{(eq. 21)}$$

where:

R_{MON} is the current monitor resistor. R_{MON} is connected from IMON pin to FBRTN.
R_{LIM} is the current limit resistor.
R_O is the output load line resistance.
I_{FS} is the output current when the voltage on IMON is at full scale.

Feedback Loop Compensation Design

Optimized compensation of the APD3212A/NCP3218A allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc, and that is equal to the droop resistance (R_O). With the resistive output impedance, the output voltage droops in proportion with the load current at any load current slew rate, ensuring the optimal position and allowing the minimization of the output decoupling.

With the multimode feedback structure of the APD3212A/NCP3218A, it is necessary to set the feedback compensation so that the converter's output impedance works in parallel with the output decoupling. In addition, it is necessary to compensate for the several poles and zeros created by the output inductor and decoupling capacitors (output filter).

A Type III compensator on the voltage feedback is adequate for proper compensation of the output filter. Figure 31 shows the Type III amplifier used in the APD3212A/NCP3218A. Figure 32 shows the locations of the two poles and two zeros created by this amplifier.

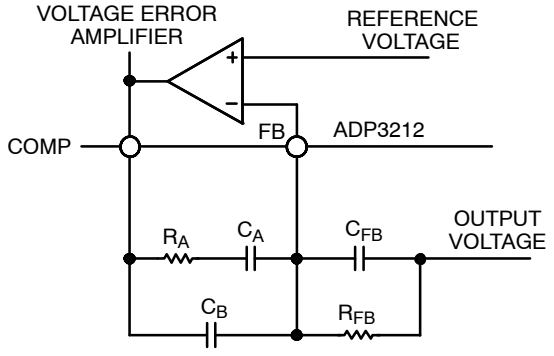


Figure 31. Voltage Error Amplifier

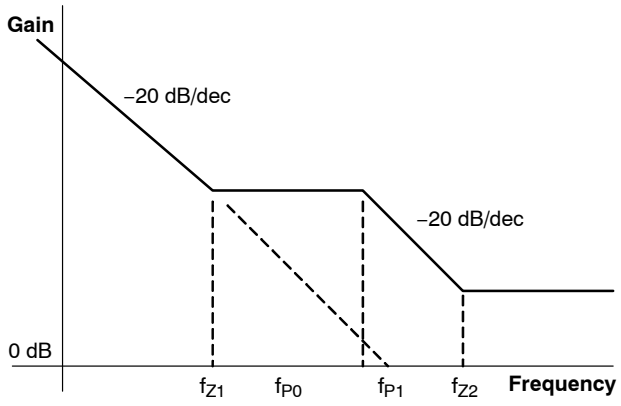


Figure 32. Poles and Zeros of Voltage Error Amplifier

The following equations give the locations of the poles and zeros shown in Figure 32:

$$f_{Z1} = \frac{1}{2\pi \times C_A \times R_A} \quad \text{(eq. 22)}$$

$$f_{Z2} = \frac{1}{2\pi \times C_{FB} \times R_{FB}} \quad \text{(eq. 23)}$$

$$f_{P0} = \frac{1}{2\pi \times (C_A + C_B) \times R_{FB}} \quad \text{(eq. 24)}$$

$$f_{P1} = \frac{C_A + C_B}{2\pi \times R_A \times C_B \times C_A} \quad \text{(eq. 25)}$$

The expressions that follow compute the time constants for the poles and zeros in the system and are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects (see the Tuning Procedure for 12 section):

$$R_E = n \times R_O + A_D \times R_{DS} + \frac{R_L \times V_{RT}}{V_{VID}} + \frac{2 \times L \times (1 - (n \times D)) \times V_{RT}}{n \times C_X \times R_O \times V_{VID}} \quad \text{(eq. 26)}$$

$$T_A = C_X \times (R_O - R') + \frac{L_X}{R_O} \times \frac{R_O - R'}{R_X} \quad \text{(eq. 27)}$$

$$T_B = (R_X + R' - R_O) \times C_X \quad \text{(eq. 28)}$$

$$T_C = \frac{V_{RT} \times \left(L - \frac{A_D \times R_{DS}}{2 \times f_{SW}}\right)}{V_{VID} \times R_E} \quad \text{(eq. 29)}$$

$$T_D = \frac{C_X \times C_Z \times R_O{}^2}{C_X \times (R_O - R') + C_Z \times R_O} \quad \text{(eq. 30)}$$

where:

R' is the PCB resistance from the bulk capacitors to the ceramics and is approximately 0.4 mΩ (assuming an 8−layer motherboard).
R_{DS} is the total low−side MOSFET for on resistance per phase.
A_D is 5.
V_{RT} is 1.25 V.
L_X is 150 pH for the six Panasonic SP capacitors.

The compensation values can be calculated as follows:

$$C_A = \frac{n \times R_O \times T_A}{R_E \times R_B} \quad \text{(eq. 31)}$$

$$R_A = \frac{T_C}{C_A} \quad \text{(eq. 32)}$$

$$C_B = \frac{T_B}{R_B} \quad \text{(eq. 33)}$$

$$C_{FB} = \frac{T_D}{R_A} \quad \text{(eq. 34)}$$

The standard values for these components are subject to the tuning procedure described in the Tuning Procedure for 12 section.

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor−current mode, the source current of the high−side MOSFET is approximately a square wave with a duty ratio equal to $n \times V_{OUT}/V_{IN}$ and an amplitude that is one−n^{th} of the maximum output current. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum rms current. The maximum rms capacitor current occurs at the lowest input voltage and is given by:

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{n \times D} - 1} \quad \text{(eq. 35)}$$

$$I_{CRMS} = 0.18 \times 40\ A \times \sqrt{\frac{1}{2 \times 0.18} - 1} = 9.6\ A$$

where I_O is the output current.

In a typical notebook system, the battery rail decoupling is achieved by using MLC capacitors or a mixture of MLC capacitors and bulk capacitors. In this example, the input capacitor bank is formed by eight pieces of 10 μF, 25 V MLC capacitors, with a ripple current rating of about 1.5 A each.

RC Snubber

It is important in any buck topology to use a resistor−capacitor snubber across the low side power MOSFET. The RC snubber dampens ringing on the switch node when the high side MOSFET turns on. The switch node ringing could cause EMI system failures and increased stress on the power components and controller. The RC snubber should be placed as close as possible to the low side MOSFET. Typical values for the resistor range from 1 Ω to 10 Ω. Typical values for the capacitor range from 330 pF to 4.7 nF. The exact value of the RC snubber depends on the PCB layout and MOSFET selection. Some fine tuning must be done to find the best values. The equation below is used to find the starting values for the RC subber.

$$R_{Snubber} = \frac{1}{2 \times \pi \times f_{Ringing} \times C_{OSS}} \quad \text{(eq. 36)}$$

$$C_{Snubber} = \frac{1}{\pi \times f_{Ringing} \times R_{Snubber}} \quad \text{(eq. 37)}$$

$$P_{Snubber} = C_{Snubber} \times V_{Input}{}^2 \times f_{Switching} \quad \text{(eq. 38)}$$

Where $R_{Snubber}$ is the snubber resistor.
$C_{Snubber}$ is the snubber capacitor.
$f_{Rininging}$ is the frequency of the ringing on the switch node when the high side MOSFET turns on.
C_{OSS} is the low side MOSFET output capacitance at V_{Input}. This is taken from the low side MOSFET data sheet.
V_{input} is the input voltage.
$f_{Switching}$ is the switching frequency.
$P_{Snubber}$ is the power dissipated in $R_{Snubber}$.

Selecting Thermal Monitor Components

To monitor the temperature of a single−point hot spot, set R_{TTSET1} equal to the NTC thermistor's resistance at the alarm temperature. For example, if the alarm temperature for VRTT is 100°C and a Vishey thermistor (NTHS−0603N011003J) with a resistance of 100 kΩ at 25°C, or 6.8 kΩ at 100°C, is used, the user can set R_{TTSET1} equal to 6.8 kΩ (the R_{TH1} at 100°C).

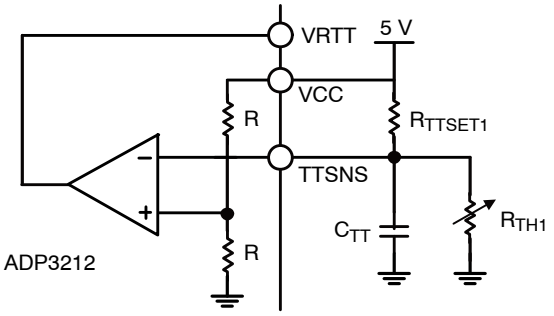


Figure 33. Single−Point Thermal Monitoring

To monitor the temperature of multiple−point hot spots, use the configuration shown in Figure 34. If any of the monitored hot spots reaches the alarm temperature, the VRTT signal is asserted. The following calculation sets the alarm temperature:

$$R_{TTSET1} = \frac{1/2 + \frac{V_{FD}}{V_{REF}}}{1/2 - \frac{V_{FD}}{V_{REF}}} \times R_{TH1AlarmTemperature} \quad \text{(eq. 39)}$$

where V_{FD} is the forward drop voltage of the parallel diode.

Because the forward current is very small, the forward drop voltage is very low, that is, less than 100 mV. Assuming the same conditions used for the single−point thermal monitoring example—that is, an alarm temperature of 100°C and use of an NTHS−0603N011003J Vishay thermistor—solving Equation 39 gives a R_{TTSET} of 7.37 kΩ, and the closest standard resistor is 7.32 kΩ (1%).

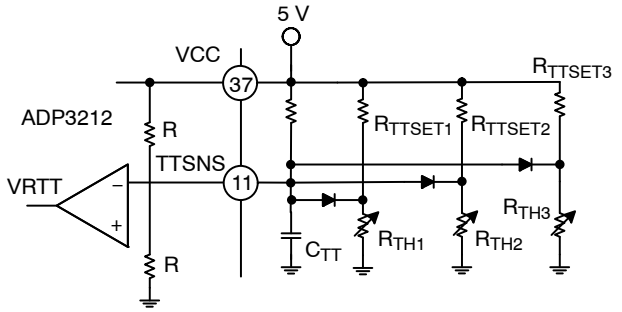


Figure 34. Multiple−Point Thermal Monitoring

The number of hot spots monitored is not limited. The alarm temperature of each hot spot can be individually set by using different values for R_{TTSET1}, R_{TTSET2}, ... R_{TTSETn}.

Tuning Procedure for APD3212A/NCP3218A

Set Up and Test the Circuit

1. Build a circuit based on the compensation values computed from the design spreadsheet.
2. Connect a dc load to the circuit.
3. Turn on the APD3212A/NCP3218A and verify that it operates properly.
4. Check for jitter with no load and full load conditions.

Set the DC Load Line

1. Measure the output voltage with no load (V_{NL}) and verify that this voltage is within the specified tolerance range.
2. Measure the output voltage with a full load when the device is cold (V_{FLCOLD}). Allow the board to run for ~10 minutes with a full load and then measure the output when the device is hot (V_{FLHOT}). If the difference between the two measured voltages is more than a few millivolts, adjust R_{CS2} using Equation 40.

$$R_{CS2(NEW)} = R_{CS2(OLD)} \times \frac{V_{NL} - V_{FLCOLD}}{V_{NL} - V_{FLHOT}} \quad \text{(eq. 40)}$$

3. Repeat Step 2 until no adjustment of R_{CS2} is needed.
4. Compare the output voltage with no load to that with a full load using 5 A steps. Compute the load line slope for each change and then find the average to determine the overall load line slope (R_{OMEAS}).
5. If the difference between R_{OMEAS} and R_O is more than 0.05 mΩ, use the following equation to adjust the R_{PH} values:

$$R_{PH(NEW)} = R_{PH(OLD)} \times \frac{R_{OMEAS}}{R_O} \quad \text{(eq. 41)}$$

6. Repeat Steps 4 and 5 until no adjustment of R_{PH} is needed. Once this is achieved, do not change R_{PH}, R_{CS1}, R_{CS2}, or R_{TH} for the rest of the procedure.
7. Measure the output ripple with no load and with a full load with scope, making sure both are within the specifications.

Set the AC Load Line

1. Remove the dc load from the circuit and connect a dynamic load.
2. Connect the scope to the output voltage and set it to dc coupling mode with a time scale of 100 μs/div.
3. Set the dynamic load for a transient step of about 40 A at 1 kHz with 50% duty cycle.
4. Measure the output waveform (note that use of a dc offset on the scope may be necessary to see the waveform). Try to use a vertical scale of 100 mV/div or finer.
5. The resulting waveform will be similar to that shown in Figure 35. Use the horizontal cursors to measure V_{ACDRP} and V_{DCDRP}, as shown in Figure 35. Do not measure the undershoot or overshoot that occurs immediately after the step.

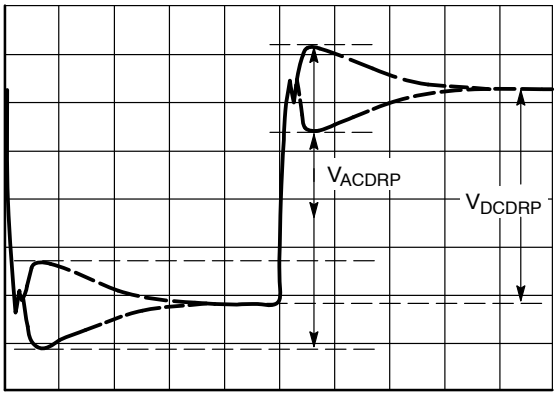


Figure 35. AC Load Line Waveform

6. If the difference between V_{ACDRP} and V_{DCDRP} is more than a couple of millivolts, use Equation 42 to adjust C_{CS}. It may be necessary to try several parallel values to obtain an adequate one because there are limited standard capacitor values available (it is a good idea to have locations for two capacitors in the layout for this reason).

$$C_{CS(NEW)} = C_{CS(OLD)} \times \frac{V_{ACDRP}}{V_{DCDRP}} \quad \text{(eq. 42)}$$

7. Repeat Steps 5 and 6 until no adjustment of C_{CS} is needed. Once this is achieved, do not change C_{CS} for the rest of the procedure.
8. Set the dynamic load step to its maximum step size (but do not use a step size that is larger than needed) and verify that the output waveform is square, meaning V_{ACDRP} and V_{DCDRP} are equal.
9. Ensure that the load step slew rate and the powerup slew rate are set to ~150 A/μs to 250 A/μs (for example, a load step of 50 A should

take 200 ns to 300 ns) with no overshoot. Some dynamic loads have an excessive overshoot at powerup if a minimum current is incorrectly set (this is an issue if a VTT tool is in use).

Set the Initial Transient

1. With the dynamic load set at its maximum step size, expand the scope time scale to 2 μs/div to 5 μs/div. This results in a waveform that may have two overshoots and one minor undershoot before achieving the final desired value after V_{DROOP} (see Figure 36).

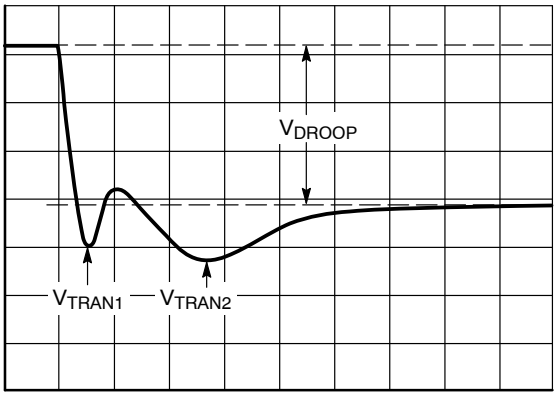


Figure 36. Transient Setting Waveform, Load Step

2. If both overshoots are larger than desired, try the following adjustments in the order shown.

a. Increase the resistance of the ramp resistor (R_{RAMP}) by 25%.

b. For V_{TRAN1}, increase C_B or increase the switching frequency.

c. For V_{TRAN2}, increase R_A by 25% and decrease C_A by 25%.

If these adjustments do not change the response, it is because the system is limited by the output decoupling. Check the output response and the switching nodes each time a change is made to ensure that the output decoupling is stable.

3. For load release (see Figure 37), if $V_{TRANREL}$ is larger than the value specified by IMVP−6.5, a greater percentage of output capacitance is needed. Either increase the capacitance directly or decrease the inductor values. (If inductors are changed, however, it will be necessary to redesign the circuit using the information from the spreadsheet and to repeat all tuning guide procedures).

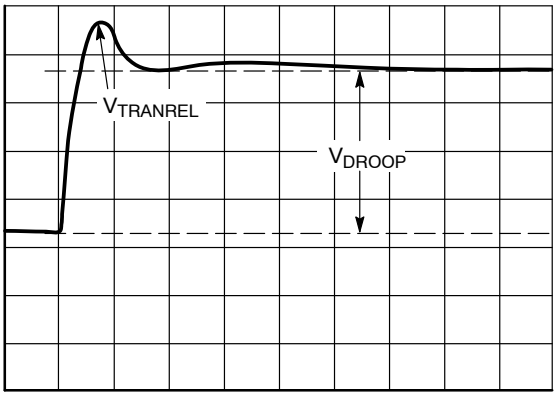


Figure 37. Transient Setting Waveform, Load Release

Layout and Component Placement

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

1. For best results, use a PCB of four or more layers. This should provide the needed versatility for control circuitry interconnections with optimal placement; power planes for ground, input, and output; and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 oz copper trace has a resistance of ~0.53 mΩ at room temperature.
2. When high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the output voltage sense lines of the APD3212A/NCP3218A) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of increasing signal ground noise.
4. An analog ground plane should be used around and under the APD3212A/NCP3218A for referencing the components associated with the controller. This plane should be tied to the nearest ground of the output decoupling capacitor, but should not be tied to any other power circuitry to prevent power currents from flowing into the plane.

5. The components around the APD3212A/NCP3218A should be located close to the controller with short traces. The most important traces to keep short and away from other traces are those to the FB and CSSUM pins. Refer to Figure 30 for more details on the layout for the CSSUM node.
6. The output capacitors should be connected as close as possible to the load (or connector) that receives the power (for example, a microprocessor core). If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
7. Avoid crossing signal lines over the switching power path loop, as described in the Power Circuitry section.
8. Connect a 1 μF decoupling ceramic capacitor from VCC to GND. Place this capacitor as close as possible to the controller. Connect a 4.7 μF decoupling ceramic capacitor from PVCC to PGND. Place capacitor as close as possible to the controller.

Power Circuitry

1. The switching power path on the PCB should be routed to encompass the shortest possible length to minimize radiated switching noise energy (that is, EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise−related operational problems in the power−converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. The use of short, wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.
2. When a power−dissipating component (for example, a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer heat to the surrounding air. To achieve optimal thermal dissipation, mirror the pad configurations used to heat sink the MOSFETs on the opposite side of the PCB. In addition, improvements in thermal performance can be obtained using the largest possible pad area.
3. The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.
4. For best EMI containment, a solid power ground plane should be used as one of the inner layers and extended under all power components.

Signal Circuitry

1. The output voltage is sensed and regulated between the FB and FBRTN pins, and the traces of these pins should be connected to the signal ground of the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be as small as possible. Therefore, the FB and FBRTN traces should be routed adjacent to each other, atop the power ground plane, and back to the controller.
2. The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be Kelvin connected to the center point of the copper bar, which is the V_{CORE} common node for the inductors of all the phases.
3. On the back of the APD3212A/NCP3218A package, there is a metal pad that can be used to heat sink the device. Therefore, running vias under the APD3212A/NCP3218A is not recommended because the metal pad may cause shorting between vias.

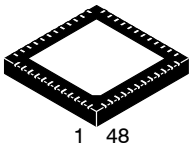
ORDERING INFORMATION

Device Number*	Temperature Range	Package	Package Option	Shipping†
ADP3212AMNR2G	−40°C to 100°C	48−Lead Frame Chip Scale Pkg [QFN_VQ] 7x7 mm, 0.5 mm pitch	CP−48−1	2500 / Tape & Reel
NCP3218AMNR2G	−40°C to 100°C	48−Lead Frame Chip Scale Pkg [QFN_VQ] 6x6 mm, 0.4 mm pitch	CP−48−1	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
*The “G” suffix indicates Pb−Free package.

QFN48 7x7, 0.5P
CASE 485AJ−01
ISSUE O

DATE 27 APR 2007



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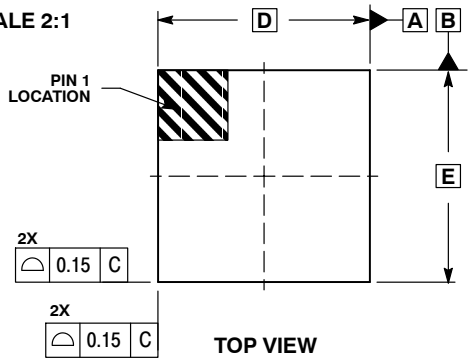
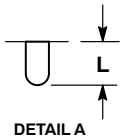


TOP VIEW



DETAIL A
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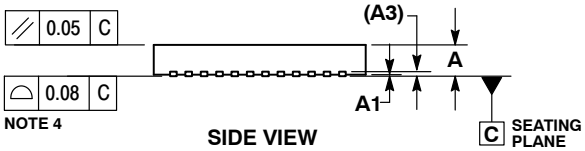
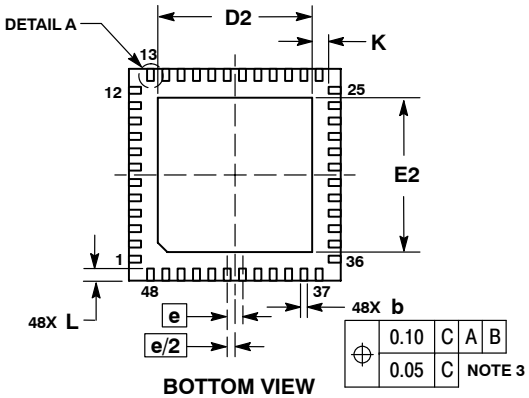
2X SCALE



SIDE VIEW

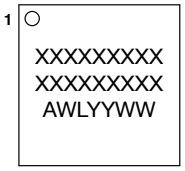


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	7.00 BSC	
D2	5.00	5.20
E	7.00 BSC	
E2	5.00	5.20
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

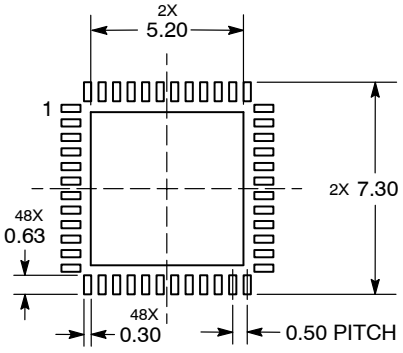
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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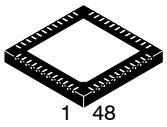
QFN48 6x6, 0.4P
CASE 485BA
ISSUE A

DATE 16 FEB 2010



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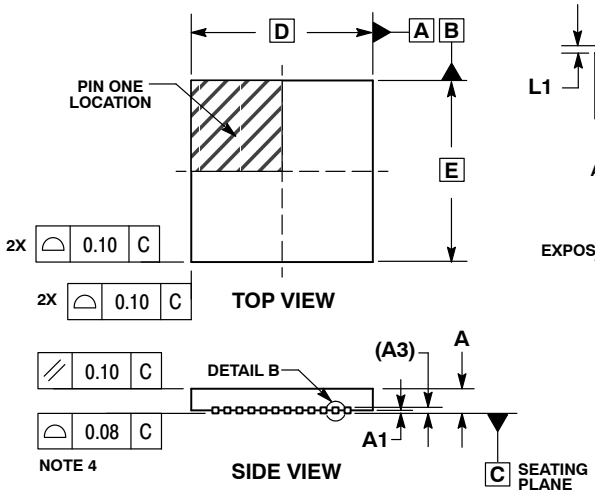

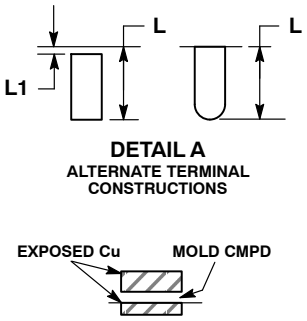

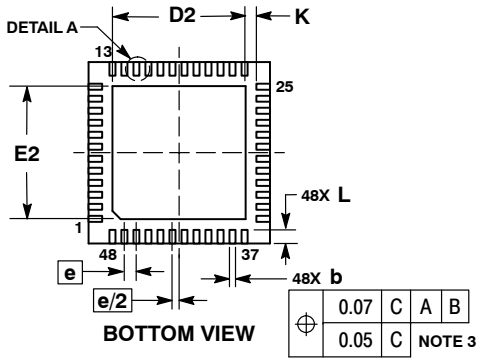

NOTES:
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	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.40	4.60
E	6.00 BSC	
E2	4.40	4.60
e	0.40 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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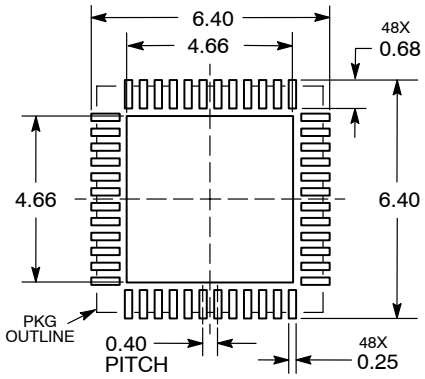

DIMENSIONS: MILLIMETERS

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